(Received 27 September 2024, Accepted 12 December 2024, Scheduled 27 December 2024)

Wideband RF GaN Power Amplifiers

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ABSTRACT: In this paper, 5G communication system requires high broadband, high efficiency, low distortion, and good heat dissipation for RF power amplifier. A GaN RF power amplifier working in broadband is designed. The input and output matching is processed on the Al_2O_3 ceramic substrate with bond wire, and the tube shell is packaged with CuMoCu copper alloy shell. Because the power loss of the power amplifier will produce a lot of heat, the heat dissipation problem becomes a factor that cannot be ignored in the design. Using the finite element thermal simulation analysis method, the maximum temperature of the power amplifier chip under long time operation is 85°, which meets the heat dissipation demand. Under the continuous wave test conditions, the drain voltage is 30 V; the operating frequency band is 2 ∼ 6 GHz; the saturation output power is 42 dBm; the power gain is more than 45 dB; and the power added efficiency is 40%. The test results meet the actual demand.

1. INTRODUCTION

As one of the key components of the 5G communication system, RF power amplifier not only ensures the stability and coverage of signal transmission, but also puts forward higher requirements for system performance and power consumption, especially in the aspects of frequency band expansion, spectrum efficiency improvement, and power consumption optimization [1–7]. GaN semiconductors are ideal for next-generation RF power amplifiers due to their excellent high-frequency characteristics, high power density, and high-temperature stability. Especially in the field of 5G communication, GaN RF power amplifiers show great potential [8–13].

In this paper, a wideband GaN RF power amplifier is designed and implemented, focusing on its application in 5G communication systems. A GaN power chip with a thickness of 0.10 mm is used and combined with a low-loss high-frequency plate RO4350C as the substrate. The tube shell is made of CuMoCu copper alloy shell with low loss and high thermal conductivity. The microwave performance test results show that all parameters meet the design indicators. In order to evaluate the heat dissipation performance of the power amplifier, a fin-shaped heat dissipation upper cover was designed, and the thermal simulation analysis was carried out by finite element software, and the temperature distribution of the chip was simulated through the comparative analysis of the thermal simulation results, which verified the accuracy of the heat dissipation design. The purpose of this study is to provide new ideas and methods for the design and optimization of RF power amplifiers in 5G communication systems, so as to promote the further development and application of 5G communication technology [14–17].

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2. STRUCTURAL DESIGN OF POWER AMPLIFIER

2.1. Structural Layout

The design of GaN power amplifier circuit is divided into two parts: GaAs drive amplifier circuit and GaN main power amplifier circuit. In the design, we selected Rogers' 0.254 mm thick RO4350C high-frequency plate with low loss and low dielectric constant as the substrate. The carrier of the power amplifier circuit adopts CuMoCu with thermal conductivity and expansion rate that meet the requirements of the industry. The chip uses a domestic broadband high-power amplifier chip. In terms of capacitance, general-purpose microwave chip capacitors were selected. According to the requirements of the power amplifier chip for the feed combination filter capacitor and the power supply filter capacitor in the protection circuit, the peripheral filter capacitor is reasonably arranged as close to the chip as possible, so that the stability and performance of the circuit can reach the best state. Due to the gold plating on the surface of the capacitor, it is ideal for gold wire bonding and also reduces the risk of short circuits during assembly.

Due to the high power consumption and large amount of heat dissipation of the device, an appropriate assembly process is required to handle the amplifier chip in order to ensure that the junction temperature of the device is below the limit value to maintain stable operation. Firstly, the substrate is sintered on top of the cavity with low-temperature solder, and then the CuMoCu copper alloy is used as the carrier of the power amplifier chip, and the power amplifier chip and chip capacitor are sintered on the carrier by using high-temperature solder, then the carrier is fixed in the corresponding position in the module cavity. After these operations are completed, the connection between the pads is completed by means of a bond alloy wire. The overall layout of the power amplifier is shown in Fig. 1.

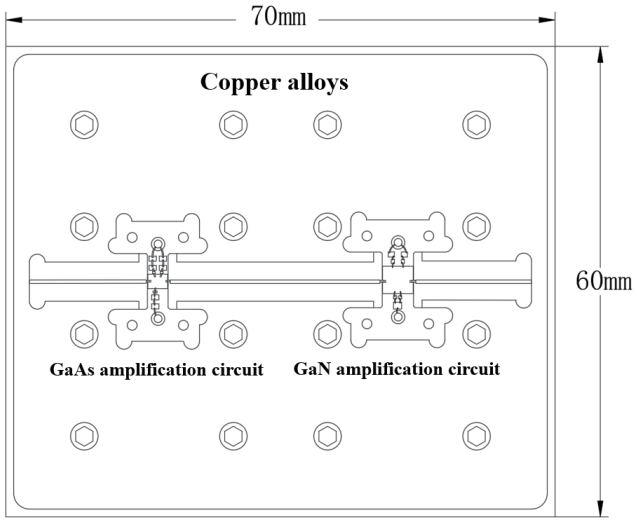

FIGURE 1. The overall assembly layout of the GaN power amplifier.

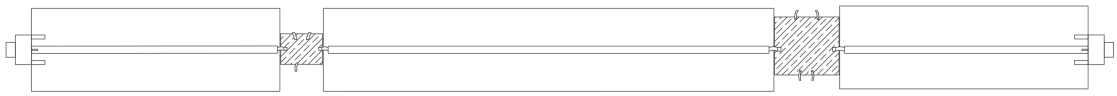

FIGURE 2. Schematic diagram of gold wire & microstrip RF loss simulation.

2.2. Power Amplification Circuit Design

The GaN power amplifier chip is based on GaN HEMT technology and uses a two-stage amplification circuit. The GaN chip is made using a 0.25 μm GaN monolithic microwave integrated circuit (MMIC) process, which is a broadband high-power amplifier chip that is grounded through a metal through a hole on the back. The circuit schematic diagram of the power amplifier design is shown in Fig. 4. VD_1 is the drain power supply port of the GaAs power amplifier; VD1 generates the gate voltage VG_1 of the GaAs power amplification circuit through the voltage conversion circuit; and the conversion circuit is also the protection circuit of the power amplifier. VD_2 is the drain power port of the GaN power amplifier, and the gate voltage of the GaN power amplification circuit is generated through the protection circuit. Both GaAS and GaN power amplification circuits are designed with protection circuits, and there is no requirement for the power-up timing of the drains of both at power-up.

In the circuit matching design, the power amplifier selected the INPA-0108-P40A GaN chip; the chip has been biased; and its own impedance matching reached 50 Ω. However, considering that the length and width of the gold wire will affect the RF loss of the power amplifier, it is concluded from the simulation diagram in Fig. 2 that the 50 μm double gold wire bonding is used, and the length is 400 μm. The gap between the microwave port of the chip and the substrate is not more than 0.05 mm [1]. It meets the requirements of 50 Ω matching circuit and has minimum RF loss. In addition, the SMA connector and transmission line will also affect the output impedance of the amplifier in practical use. In order to optimize the loss of the whole circuit, the microstrip line width [2] is optimized by simulation, and the RF loss of SMA joint is taken into account. After simulation optimization, the RF loss of the whole circuit is reduced. The simulation diagram of RF loss of the optimized RF amplifier circuit is shown in Fig. 2. The simulation results in Fig. 3 show that $S_{21} < 0$. In fact, the RF loss in the frequency band of $2 \sim 4$ GHz is negligible. As the frequency rises, there are $S_{21} \approx -1.8$ in the 5 to 6 GHz frequency band.

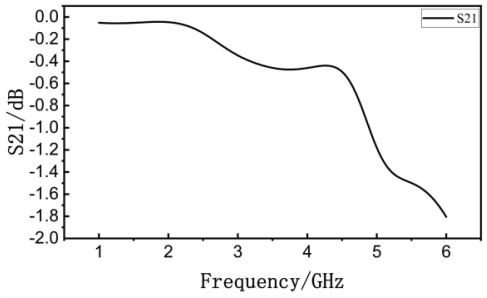

FIGURE 3. RF insertion loss S_{21} of passive structure of the power amplifier.

2.3. Power Management Module Design

The power management module of power amplifier has two main functions:

- The gate voltage required by the gate of GaN/GaAs power amplifier circuit is generated by the circuit conversion.
- Playing a role in the protection of the power amplifier chip will not be due to the power on timing error and power er-

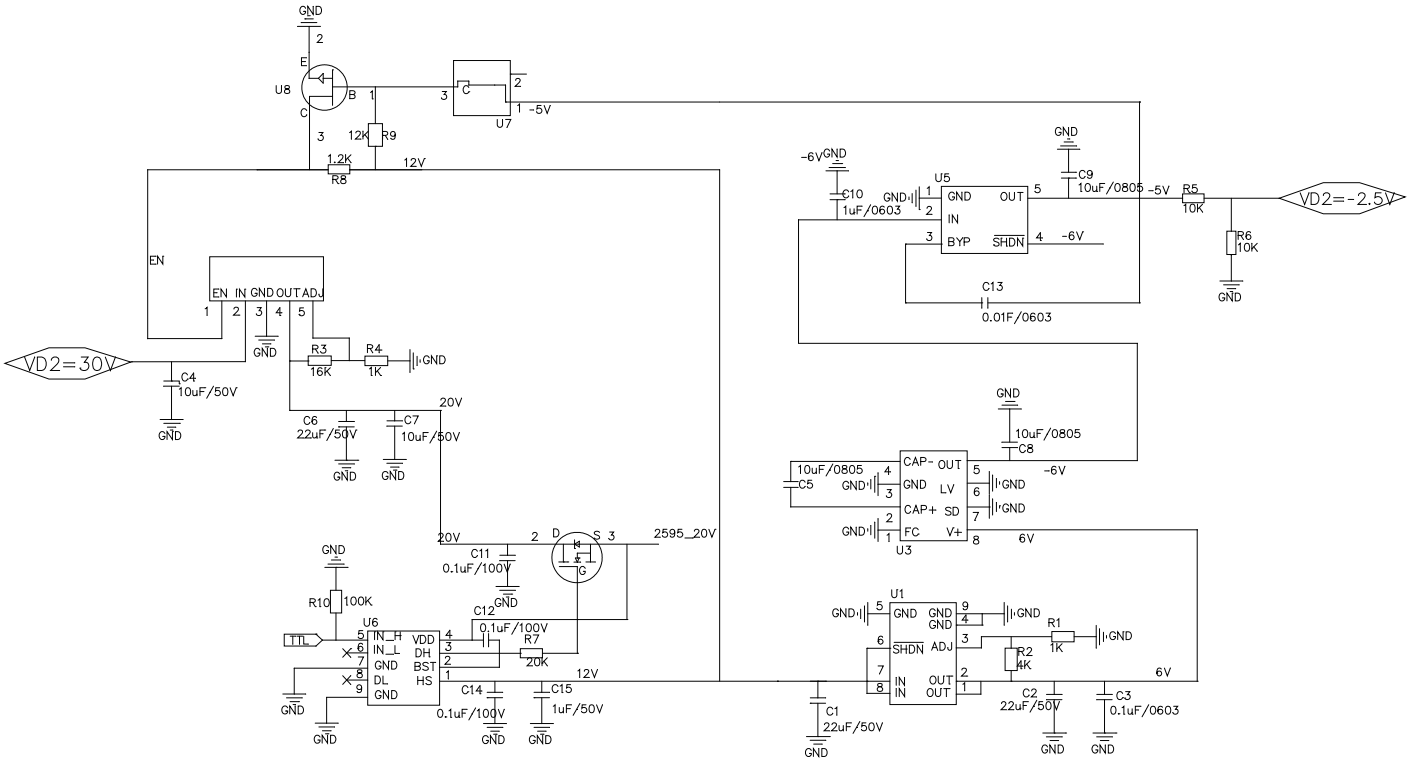

FIGURE 4. The circuit principle of the power amplifier.

ror operation to the high voltage caused by power amplifier device damage.

Design idea of protection circuit:

MIC29500(U2) is a voltage regulator with enabling regulation function, which can realize the switch control of the equipment and is suitable for a simple logical interface. Its output OUT allows programming output voltages between 1.25 V and 25 V. Here, we need to output 20 V voltage, so we use two resistors to control the output voltage. The specific two resistors can be calculated according to Equation (1):

$$R_1 = R_2 * \left(\frac{V_{out}}{1.24} - 1\right) \tag{1}$$

U_2 plays a vital role in the protection circuit. On the one hand, when the temperature of the power amplifier exceeds the maximum safe operating temperature of $+125°$, the thermal shutdown will make the device invalid. In addition, if the input voltage in the line transient protection exceeds about 32 V, the overvoltage sensor disables the voltage regulator, which makes the equipment ineffective and plays a protective role.

MAX15018A(U_6) is a high-speed, half-bridge MOSFET driver. The pin: BST boost, used for high-side MOSFET driver power supply; DH is the high-side gate driver output, and the driver output is the high-side MOSFET gate. IN_H is the high-side non-reverse logic input. Therefore, the signal input from the high voltage side into the circuit can maintain the phase unchanged after passing through the circuit and finally generate 12 V voltage.

LT1965(U_1) is a low noise, low difference linear regulator, and low output noise characteristics make it very suitable for the power amplifier power supply design. The internal integrated circuit of U_1 includes current limiting, countercurrent and overtemperature protection, which can protect GaN devices when the maximum operating environment temperature exceeds 125°C or when the load is instantaneous. It is the pull-up resistor in the circuit that is pulled low first, and then U_1 enters a low-power state, because there is a "logical or" relationship between the SHDN pin and pull-up resistor (which can be regarded as a circuit composed of diodes). Therefore, if the power supply is reversed, U1 is equivalent to a diode in series with the input. Thus playing the role of power protection. In the case that the SHDN pin logic cannot be referenced to the reverse input of the power supply, if the power supply is reversed, U_1 is equivalent to a diode in series with its input. Therefore, when the protection circuit plays the role of providing voltage for the gate of GaN power amplifier, we need to further design the gate voltage converter. OUT is the output pin, and the output voltage ranges from 1.20 V to 19.5 V. A minimum output capacitance of 10 µF is used to prevent oscillations. According to the design requirements, the output voltage of 6 V is required, and the calculation formula of the two resistance values at the output end is given by Equation (2):

$$V_{out} = 1.2\,\text{V} * \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} * R_2 \tag{2}$$

Here are: $V_{ADJ} = 1.2$ V, $I_{ADJ} = 1.3$ µA@25° and Output range $= 1.2\,\text{V} \sim 19.5$ V.

ADM8660 (U_3) is a voltage converter that is used to reverse the input voltage. Its conversion to reverse output voltage range is $-1.5\,\text{V} \sim -7$ V. From this we can convert $+6$ V to -6 V.

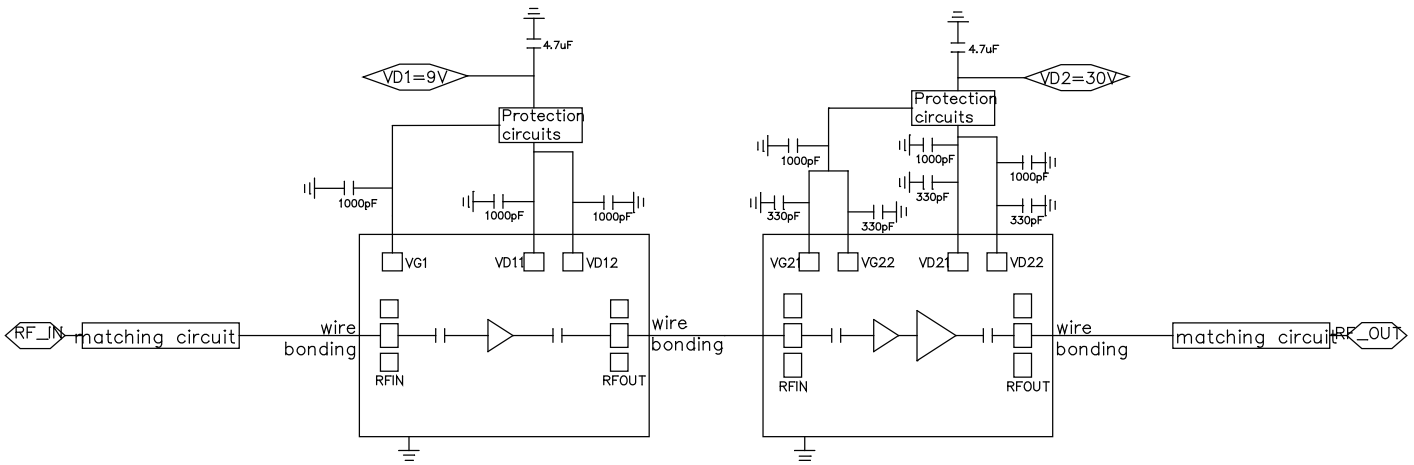

FIGURE 5. Schematic diagram of the protection circuit.

The LT1964 (U_5) is a low noise, low dropout negative regulator. The device has a fixed output voltage of -5 V and an adjustable voltage range of $-1.2\,\text{V} \sim -5\,\text{V}$. The SHDN pin of U_5 allows negative logic drive, and when the SHDN pin is pulled within the GND ± 0.8 V range, the output of the LT1964 will be turned off. Pulling the SHDN pin greater than -1.9 V will turn the LT1964 on. Therefore, there is a parasitic diode between the OUT, ADJ, and SHDN pins and the IN pin in the protection circuit design process, because in the fault case, the OUT, ADJ, and SHDN pins cannot pull more negative voltages than the IN pins by more than 0.5 V and must maintain a higher voltage than the IN pins during operation, so as to achieve the purpose of protecting the circuit. The U_5 output (OUT) has an output voltage range of -1.22 V to -20 V. The output supplies power to the load, and the output capacitance is 10 µF to prevent oscillation. The gate voltage of -2.5 V for the final GaN amplifier circuit is set by the ratio of the two external resistors as shown in Fig. 5 and is determined by Equation (3):

$$V_{out} = -1.22\,\text{V} * \left(1 + \frac{R_2}{R_1}\right) - I_{ADJ} * R_2 \qquad (3)$$

Here are: $V_{ADJ} = -1.22$ V, $I_{ADJ} = 30$ nA@25° and Output range $= -1.2\,\text{V} \sim -20$ V.

The circuit schematic diagram of the entire power management module is shown in Fig. 5, and U_5 and U_7 jointly generate an enabling signal, which is transmitted to U_2. Only when U_2 receives the enabled signal, U_2 will work normally and generate gate voltage, through the action of the entire circuit protection mechanism, so that the whole protection circuit forms a perfect loop, which can not only generate gate voltage, but also play the role of protection circuit.

3. HEAT DISSIPATION DESIGN OF THE POWER AMPLIFIER

The heat dissipation design of power amplifiers usually needs to consider the simulation of device thermal characteristics, heat conduction model, heat dissipation structure design, working environment simulation, and temperature distribution analysis. If heat is not dissipated in time, the temperature of the chip will rise, which can lead to performance degradation, failure, or even permanent damage. Good thermal design helps to maintain the stable operating temperature of the chip, and maintain the stability of device performance and output. At the same time, lowering the temperature helps extend the chip life and improve system reliability. Therefore, thermal treatment is critical in the design of power amplifiers to ensure their performance, reliability, and longevity.

3.1. Thermal Simulation Model

The GaN power amplifier mainly uses a fin-shaped heat dissipation structure, because the fin-shaped heat sink can improve heat dissipation efficiency by increasing the surface area, so that heat can be transferred to the surrounding environment more quickly. Secondly, the materials and processes required to manufacture fin heat sinks are relatively simple and low cost, which is suitable for the large-scale production of 5G communication RF transmitter modules. The thermal conductivity of the materials in the thermal simulation model is shown in Table 1, and the main body of the fin-shaped heat dissipation structure is shown in Fig. 6, in which the main material of the fin-shaped heat dissipation structure is composed of copper alloy, and a fin-shaped lower cover plate and a power amplification circuit carrier are used as heat dissipation holes and metallized.

3.2. Thermal Simulation Boundary Conditions

In the simulation of finite element simulation software, it is necessary to carry out thermal simulation according to the assembly mode and actual application conditions of the amplifier. The size of the GaN power amplifier chip is 3.88 mm × 3.49 mm × 0.1 mm, and the chip is connected with the substrate through $Au_{80}Sn_{20}$ solder. The substrate and PCB are connected by $Sn_{63}Pb_{37}$ solder. The PCB is connected to the carrier by $Sn_{96.5}Ag_3Cu_{0.5}$ solder. Subsequently, according to the internationally prescribed GJB548B thermal performance test method [1], the thermal simulation environment of the amplifier was set at a constant temperature of 70°, and the heat transfer model is shown in Fig. 7. According to this model, the

TABLE 1. Thermal conductivity of each material in the model.

Name	Material	Thermal Conductivity/ (W/(m·K))
Chip	GaN	200
Chip soldering layer	$Au_{80}Sn_{20}$	57
PCB	Ro4350C	0.68
Carrier	Copper alloys	110

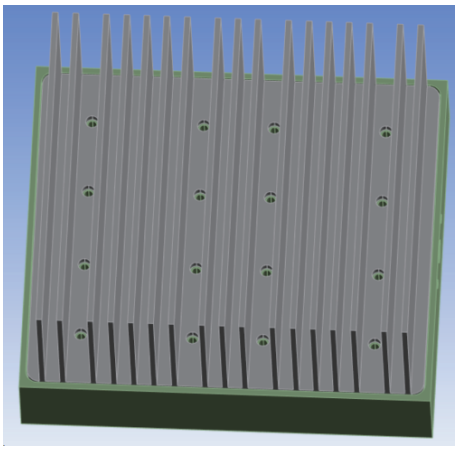

FIGURE 6. Fin-shaped heat dissipation structure of the amplifier.

parameters set in Ansys mainly included heat flow, heat flux, internal heat generation and convection. The heat flow is the thermal dissipation power consumption of the chip, and the calculation method of the specific parameters is as follows:

$$\text{Chip volume: } V = 2.53 * 1.84 * 0.1\,\text{mm}^3$$

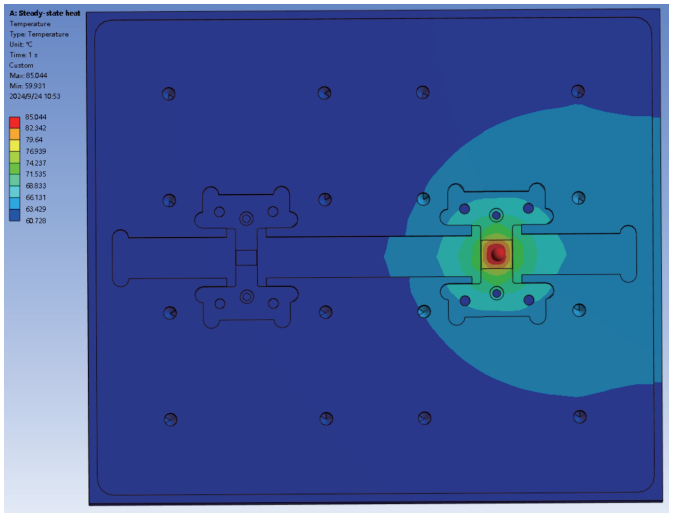

FIGURE 7. Schematic diagram of fin-shaped heat dissipation simulation.

Internal Thermal Generation A:

$$A = \frac{\text{Thermal dissipation power consumption}}{V} \quad (4)$$

Note that the heat flow needs to be calculated according to the actual simulation, and the area of the chip is converted into heat flux. If it is the volume of the chip, it is converted into internal heat generation, which is brought into the thermal simulation software for analysis. If the heat dissipation power consumption of the GaN chip is 15 W, the internal heat generation is generated, 3.22×10^{10} W/m^3, i.e., the heat dissipation of 15 W is applied to the active region of the chip during the simulation, and the constant temperature boundary condition is used as the simulation boundary condition to carry out the steady-state thermal simulation analysis of the model under continuous wave.

3.3. Analysis of Thermal Simulation Results

Thermal simulation is carried out before the chip package is processed into the shell and PCB, and the junction temperature structure of the power amplifier can be simulated in advance to evaluate the thermal stability and reliability of the device, and make necessary thermal design improvements, and formulate appropriate thermal management strategies according to the thermal simulation results, including heat dissipation system design, fan heat dissipation control, temperature monitoring and protection, etc., in order to ensure that the power amplifier can maintain good heat dissipation performance under various operating conditions. The thermal simulation temperature field indexing of the power amplifier is shown in Fig. 7 and Fig. 8, respectively, and the results of heat dissipation show that the maximum temperature of the chip is 85°C, which is far lower than the sintering temperature of the chip of 310°C, and the heating temperature range is controlled within the working temperature of the chip of 85°C. In the absence of heat dissipation, the maximum operating temperature for a long time is 127°C, which far exceeds the maximum temperature at which the chip can operate normally. Table 2 is a comparison of the chip heat dissipation temperatures of similar devices in this paper and other literatures, and it can be seen that the heat dissipation model of this power amplifier design has obvious advantages in ensuring the heat dissipation of the power amplifier to ensure the normal operation of the device for a long time.

4. PROCESSING AND TESTING OF POWER AMPLIFIERS

For the process realization of the power amplifier, considering the high energy consumption and large heat generation of

TABLE 2. Comparison of the heat dissipation temperatures of similar devices in this paper and other literatures.

Reference	Minimum chip temperature/°C	Chip maximum temperature/°C
[1]	72.16	195.33
[2]	48.8	109.53
This paper	59.9	85

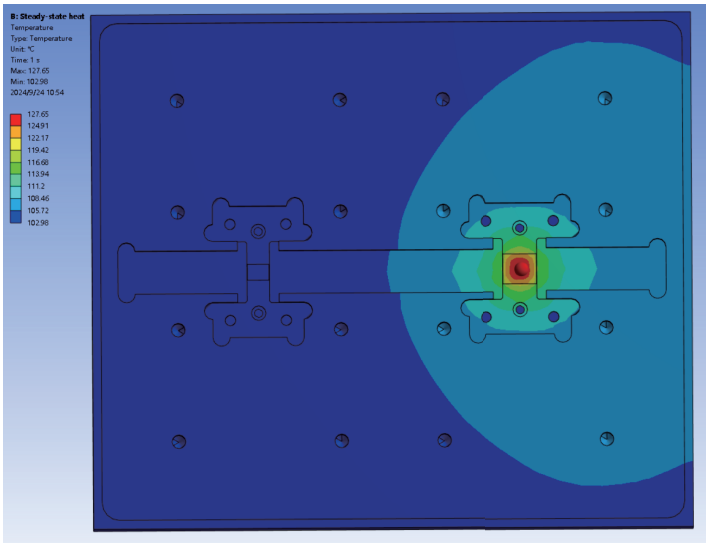

FIGURE 8. Schematic diagram of finless heat dissipation simulation.

the device, in order to ensure that the junction temperature of the device is lower than the limit value and thus works stably, the corresponding assembly process needs to be adopted for the power amplifier chip. Specifically, it is to first use low-temperature solder to sinter the substrate and the cavity, and then use the copper alloy with thermal conductivity and expansion rate that meet the requirements of the industry as the carrier of the power amplifier chip, and use high-temperature solder to sinter the power amplifier chip and chip capacitor on the carrier, and the assembly of the power amplifier chip and capacitor is completed as shown in Fig. 9(a). Then, the carrier is fixed in the corresponding position in the module cavity; after these operations are completed, the electrical connection between the pads is completed by gold wire bonding; and the assembly of the entire power amplifier circuit is finally completed [8]. The actual GaN power amplification circuit is shown in Fig. 9(b). Finally, the fin-shaped heat dissipation module is assembled to complete the packaging of the entire GaN power amplifier, and the appearance of the entire GaN power amplifier is shown in Fig. 9(c).

After the RF and power modules of the power amplifier are connected and assembled, the static power-on test of the power amplifier module is started. Before adding power, check the gate and drain resistance of the power amplifier chip. Under normal circumstances, the gate resistance should be tens of megapohms, and the drain resistance is about 1 ohm. After confirming that there is no abnormality, the power can be added. When power is added, the GaN drain voltage is 28 V according to the instructions, and the gate voltage converted by the protection circuit is -2.5 V. At this time, the quiescent current is 835 mA, which exceeds the typical value of 800 mA given by the chip. Therefore, it is necessary to adjust the bias voltage. Finally, when $V_d = 30$ V, the static current $I_{dq} = 800$ mA, which meets the design requirements.

The RF performance of the power amplifier was tested. Under the continuous wave test condition, the GaAs drain working voltage $VD_1 = 9$ V and GaN drain working voltage $VD_2 = 30$ V were used to test the RF index at the frequencies of 2 GHz, 4 GHz, and 6 GHz, respectively. The actual RF test diagram is shown in Fig. 10.

The input power of the signal generator is adjusted to test from -30 dBm to 10 dBm at an interval of 2 dBm, and the actual microwave electrical performance test results are shown in Fig. 11. When the operating frequency is $2 \sim 6$ GHz, the

TABLE 3. Advantages of developed GaN PA compared to existing ones.

Reference	Frequency/GHz	P_{sat}/dBm	Gain/dB	PAE/%
[1]	$2 \sim 6$	40.5	23	35
[3]	$4.4 \sim 5.0$	35	32	38
[10]	$1.8 \sim 5.5$	43	13	40
[11]	$2 \sim 6.7$	31	18	20
This paper	$2 \sim 6$	42	45	40

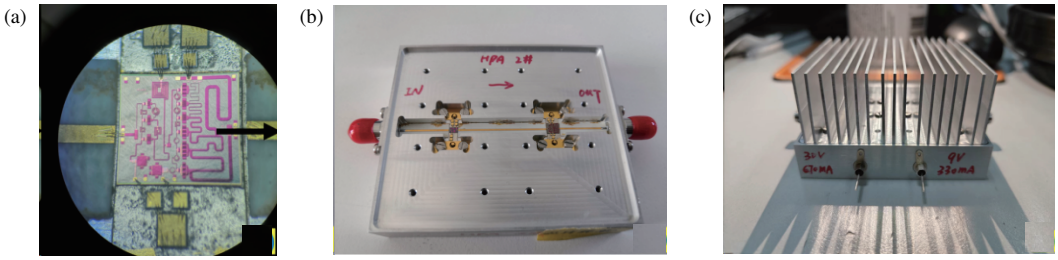

FIGURE 9. (a) GaN die assembly diagram. (b) GaN amplification circuit. (c) GaN power amplifiers.

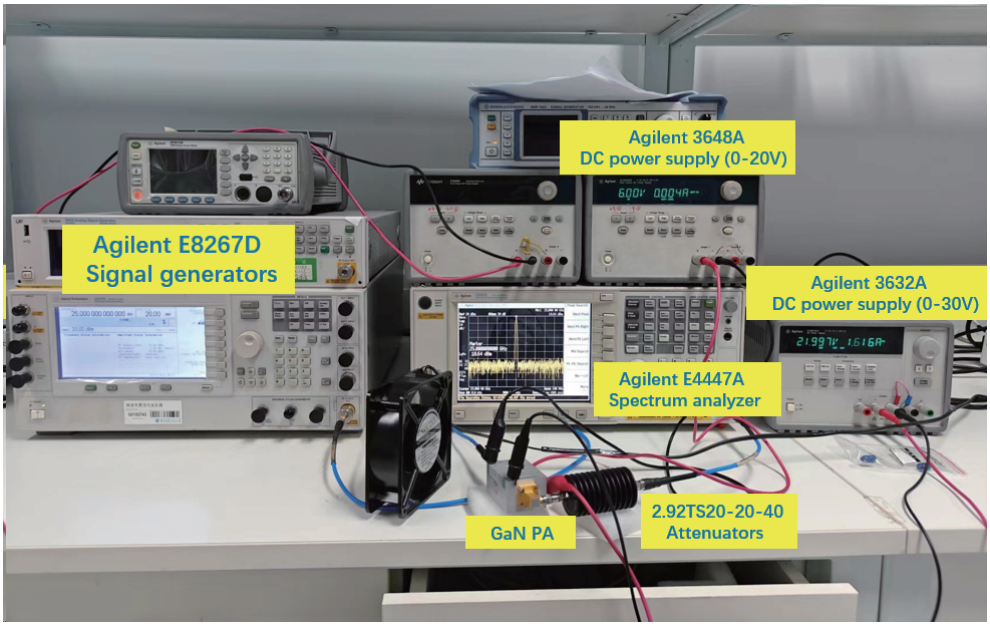

FIGURE 10. Schematic diagram of RF test.

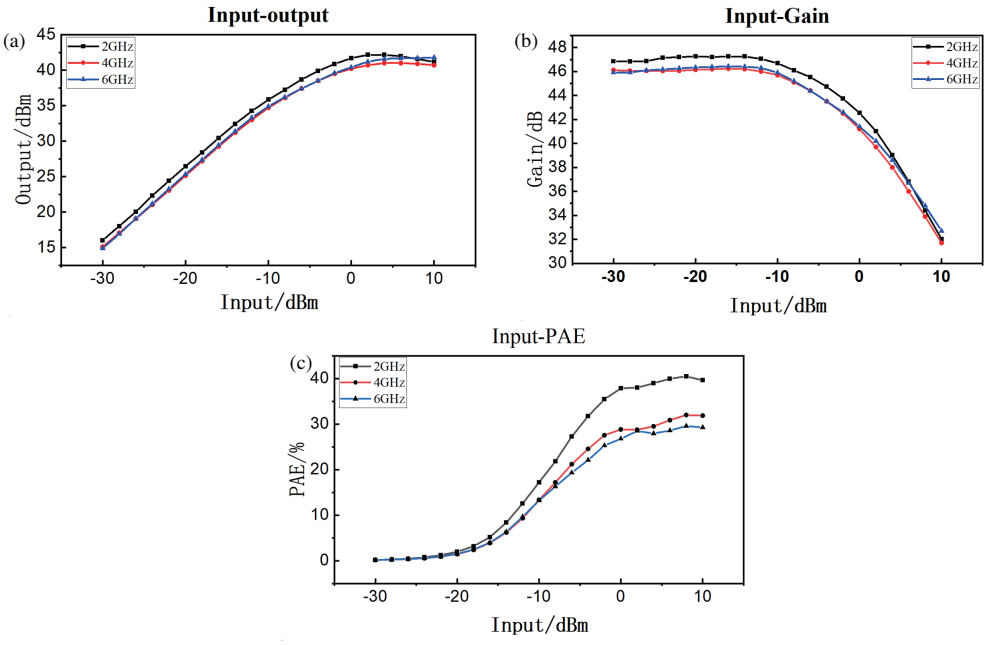

FIGURE 11. (a) Output of PA DUT test. (b) Gain of PA DUT test. (c) PAE of PA DUT test.

saturation output power is $P_{sat} = 42$ dBm; the power gain is $Gain = 45$ dB; and the power added efficiency is $PAE > 40\%$. The test results meet the expected design requirements and can well meet the actual needs. Moreover, the power amplifier has stable performance and excellent heat dissipation under long time operation. It can ensure that the power amplifier is in the normal working environment temperature for a long time. The test results prove that the design scheme is feasible. Table 3 shows the performance comparison between this paper and similar devices in other literatures. It can be seen that the power amplifier designed in this paper has certain advantages in terms of output power [3, 11], efficiency [11], and gain [10, 11].

5. CONCLUSION

In this paper, an ultra-wideband GaN power amplifier operating from 2 to 6 GHz for 5G communication is designed. The final practical test results achieve an output power of more than 40.7 dBm in the bandwidth of $2 \sim 6$ GHz. The test results of continuous signal are as follows: the saturation output power $P_{sat} = 42$ dBm, the power gain $Gain = 45$ dB, and the power added efficiency (PAE) $> 40\%$ when the power amplifier operates in the frequency band of 2–6 GHz. The heat dissipation design was carried out before packaging to control the maximum temperature of the chip under long-term operation within 85°C. It can be seen that the power amplifier not only has good heat dissipation but also has obvious advantages in bandwidth, gain, and power added efficiency of the power amplifier itself, which can be widely used in the field of 5G communication.

ACKNOWLEDGEMENT

The research was carried out within the framework of joint project with the support of the National Key Research and Development Program of China (2022YFE0122700) and the Belarusian Republican Foundation for Fundamental Research (T22KITG-018).

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