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Accurate on Wafer Calibration and S-Parameter Measurement Setup for InP-Based HEMT Devices to 220 GHz

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ABSTRACT: In this paper, the on-wafer S-parameter measurement of InP-Based HEMT devices up to 220 GHz is presented. The calibration kits utilizing a CPWG structure are meticulously designed on an InP substrate. The corresponding structure for calibrating the reflection mechanism is designed in order to reduce the influence between the two ports during the calibration process and improve isolation. The TSVs process is employed to attain broadband load. The design concept of the calibration structure is discussed, and the simulation results up to 220 GHz are provided for demonstration. The measurement results encompass frequency ranges of 0.2–66 GHz, 75–110 GHz, 110–170 GHz, and 170–220 GHz. Moreover, the test results obtained from different calibration methods for InP HEMT devices are compared and analyzed. By employing interpolation techniques, comprehensive S-parameter data for actual DUTs ranging from 0.2 to 220 GHz is successfully obtained. Furthermore, the intrinsic parameters C_{gs} is extracted from device test results, and various calibration methods are utilized for comparison. The extrapolated maximum current gain cut-off frequency f_T based on a -20 dB/decade slope in H_{21} is determined as 252 GHz while the extrapolated device maximum oscillation frequency fmax calculated through the maximum stable gain (MSG)/the maximum available gain (MAG) and Umason approaches reaches up to 435 GHz.

1. INTRODUCTION

The rapid advancement of defense aerospace systems, such as space technology, space exploration, and satellite remote sensing, has resulted in an increased demand for devices and circuits with higher frequency and bandwidth. In recent years, the frequency of Monolithic Microwave Integrated Circuit (MMIC) design has been rapidly approaching the terahertz region to meet this requirement. Furthermore, due to their exceptional characteristics including high electron mobility, high frequency capability, low noise performance, and high power gain in the terahertz band, Indium phosphide high electron mobility transistor (InP HEMT) devices have found widespread applications across various technologies. As such, precise test data plays a crucial role in circuit design. However, as the wavelength decreases with increasing frequency within this range, even minor fluctuations can significantly impact measurement precision [1]. Therefore, developing testing techniques for InP HEMT devices operating at terahertz frequencies has become an urgent problem that needs to be addressed.

The intrinsic behavior of devices, excluding the influence of pads, is crucial for accurate measurement, particularly in the case of transistors. The current procedure for eliminating the parasitic parameters of pads primarily involves off-wafer calibration, followed by de-embedding utilizing specialized structures. Among these techniques, a two-step de-embedding method open and short (OS de-embedding) is commonly employed. However, it has been reported that OS de-embedding at higher frequencies may introduce significant errors [2]. To enhance accuracy, three-step de-embedding techniques such as pad-open-short (POS de-embedding) or open-short-thru (OST de-embedding) can be utilized [3, 4]. Unfortunately, the main drawback of these methods is that the standard calibration parts typically consist of ceramic sheets, which exhibit significant differences in electrical characteristics compared to those being tested in the terahertz frequency band. In such scenarios, on-wafer calibration results, which eliminate parasitic effects caused by pads, are more reliable [5].

This paper primarily examines the calibration technology in the terahertz band. Line-Reflect-Reflect-Match (LRRM) calibration structure and multi-line Thru-Reflect-Line (TRL) calibration structure are proposed and fabricated on an InP substrate, covering a frequency range from 75 to 220 GHz. The LRRM calibration structure includes open, short, thru, and load components, with accurate preparation of the load being a major technical challenge during calibration kit fabrication [6]. The precision of the structure's preparation significantly impacts the calibration effectiveness. The multi-line TRL mainly consists of open, thru, and three line structures. Three sets of transmission lines are designed within this calibration structure to cover frequencies ranging from 75 to 220 GHz. The effects of using three lines in each frequency band are presented, compared, and analyzed. In this paper, we compare

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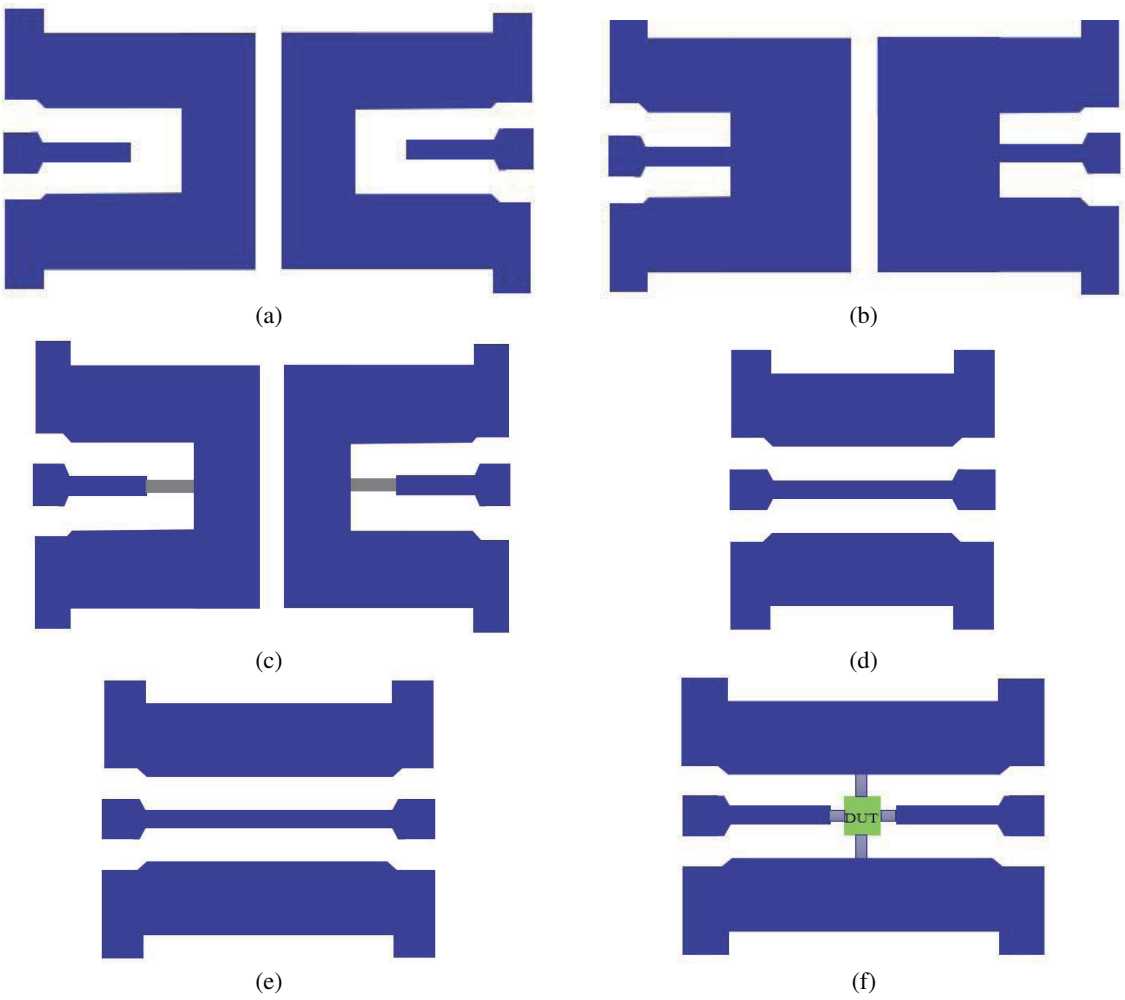

FIGURE 1. The schematic diagram of calibration kits and devices under test. (a) Open. (b) Short. (c) Load. (d) Thru. (e) Line. (f) Device under test (DUT).

the measurement results of InP HEMT devices calibrated by both LRRM and TRL methods at different frequency ranges: 0.2–66 GHz, 75–110 GHz, 110–170 GHz, and 170–220 GHz, respectively. Furthermore, we analyze the accuracy of these respective calibration methods based on variations in intrinsic parameter characteristics such as current gain, cut-off frequency, and maximum oscillation frequency extracted from relevant test data [7, 8].

2. CALIBRATION KITS AND INP HEMT DEVICE

The dispersion of the fundamental mode and even mode in coplanar waveguide ground (CPWG) structures is lower than that in microstrip line at high frequencies, making them suitable for designing circuits with high frequency and large bandwidth. This advantage becomes more pronounced when CPWGs with smaller gap widths are used. Additionally, compared to circuits based on microstrip lines, circuits with CPWG structures can be designed to be smaller while meeting the same specifications, and the presence of additional ground beside each branch can effectively reduce the coupling between adjacent structures. Based on these advantages, this paper proposes calibration kits using CPWG structures on the calibration methods discussed in this article including LRRM and TRL. LRRM consists of an open circuit, a short circuit, thru connection, and load termination, whereas TRL utilizes three additional transmission lines. Figure 1 illustrates the schematic diagram of the calibration kits and devices under test [8].

The open and short design of the reflection structure shown in Figure 1 offers the advantage of enhancing signal isolation between identical types of reflection standards by leveraging the isolation generated through probes contacting similar standards [9, 10].

The structural details of the open configuration are depicted in Figure 2(a), while Figure 2(b) illustrates its corresponding equivalent circuit. Within the open structure, a fraction of the waves is transmitted towards the unoccupied space behind the discontinuous points. This arrangement establishes an additional stray electric field at the termination of the open coplanar waveguide, thereby storing reactive energy. Simultaneously, a portion of the waves propagates along the substrate surface into free space or penetrates into the substrate.

The parasitic capacitance increases as the center line width (w) increases, and the total slot width (d) decreases. Properly

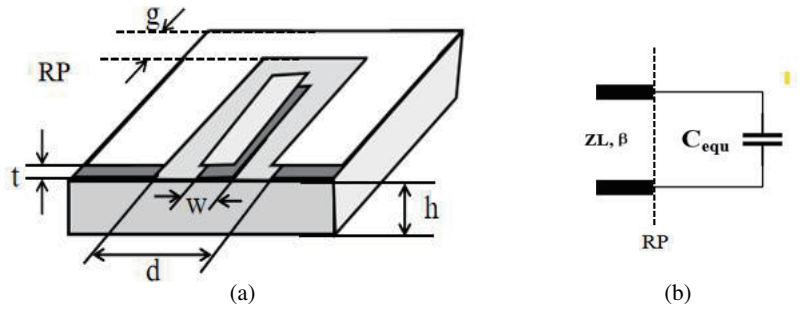

FIGURE 2. Open structure design. (a) Open structural detail. (b) Equivalent circuit for open.

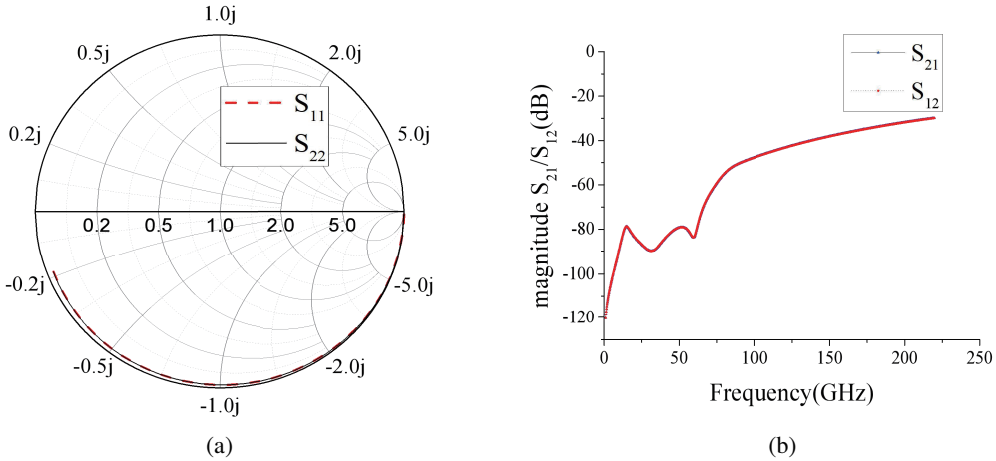

FIGURE 3. Simulated results for open structure. (a) Simth chart of S_{11} and S_{22}. (b) Magnitude of S_{21} and S_{12}.

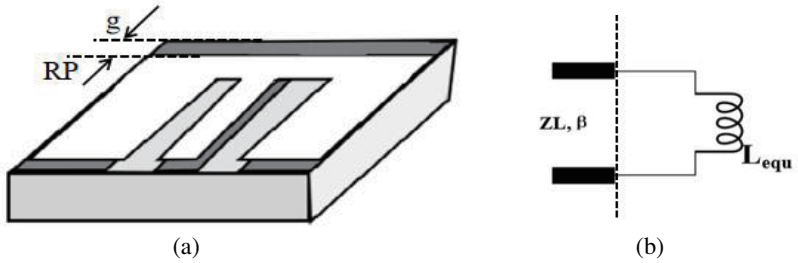

FIGURE 4. Short structure design. (a) The structural details of the short. (b) Equivalent circuit for short.

designing the gap width (g) can avoid significant additional capacitance effects at the open end. The simulation results of the open structure are presented in Figure 3, indicating satisfactory but not optimal performance due to radiation effects. Based on these findings, it can be concluded that the open structure is suitable for on-wafer calibration within the frequency range of 0.2–220 GHz.

The structural details of the short are depicted in Figure 4(a), while its equivalent circuit is illustrated in Figure 4(b). Typically, the slot width between the central conductor and the ground plane in a short structure is extremely narrow, rendering the short end akin to an ideal short circuit within the lower frequency range. However, as the frequency band approaches terahertz frequencies, certain field interferences arise at the SHORT end necessitating introduction of an equivalent inductance L_equ for characterization.

The equivalent inductance decreases significantly as the center line width w increases, or the slot width decreases. The equivalent inductance is influenced by the width of the ground wire g, but when g exceeds the slot width, its impact on the equivalent inductance can be disregarded. The simulation results of the short structure are presented in Figure 5, indicating satisfactory but not optimal values due to transmission loss. Based on the findings shown in Figure 5, it can be concluded that the short structure is suitable for on-wafer calibration within the frequency range of 0.2–220 GHz.

To achieve wideband loading, the loading structure in this paper incorporates through substrate vias (TSVs) technology. Momentum simulation was conducted using Advanced Design System (ADS) settings and High-Frequency Structure Simulator (HFSS) finite element analysis to determine the optimal position and number of through holes. The satisfactory simulation

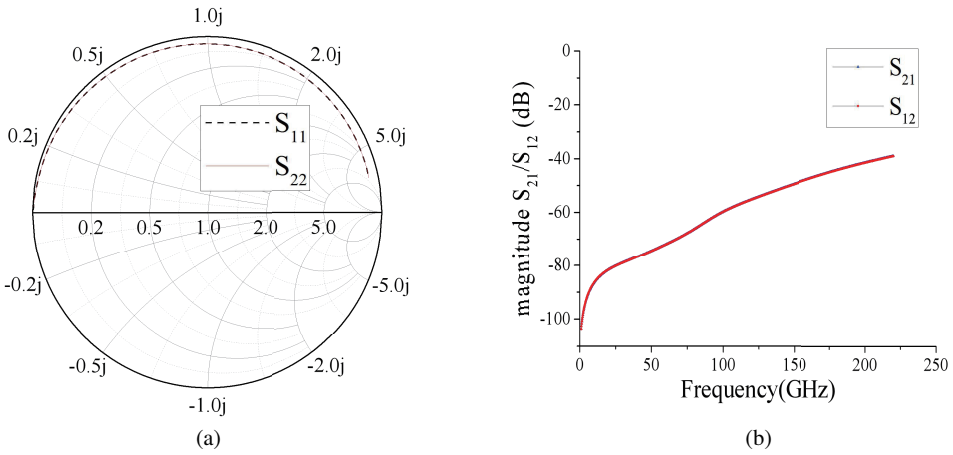

FIGURE 5. Simulated results for short structure. (a) Smith chart of S_{11} and S_{22}. (b) Magnitude of S_{21} and S_{12}.

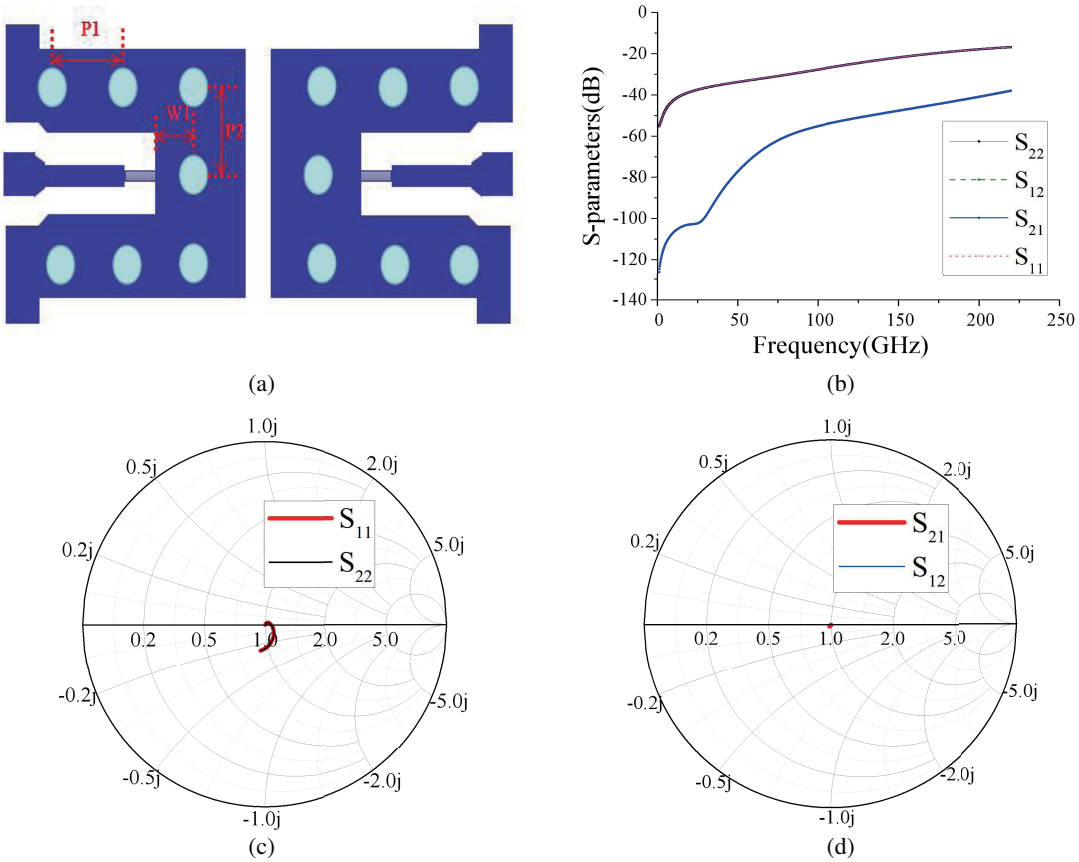

FIGURE 6. Load structure design and simulated results. (a) Load with TSVs. (b) Magnitude of S parameters. (c) Smith chart of S_{11}/S_{22}. (d) Smith chart of S_{12}/S_{21}.

results shown in Figure 6 confirm the reasonability and feasibility of the CPWG structure design method. It should be noted that during simulation, the through-hole design near the PAD structure has a significant impact on the overall load structure's bandwidth.

Moreover, there exists an impedance discontinuity between the ground-signal-ground (GSG) structure and the open, short, thru, and load structures, resulting in a certain level of parasitic capacitance. This phenomenon is particularly prominent in the applications with frequencies up to 220 GHz, thus necessitating the utilization of a gradient structure with equal impedance to mitigate the impact of parasitic capacitance. In this paper, we propose a transition structure to address this issue, as illustrated in Figure 7.

The lengths of the three lines are 98 µm, 195 µm, and 220 µm, respectively. According to the design principles in [11–16], the phase difference between the thru and line should be within a range of 20° to 160°.

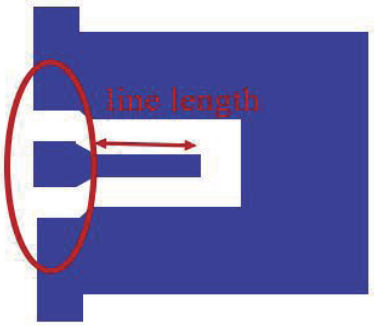

FIGURE 7. Impedance step.

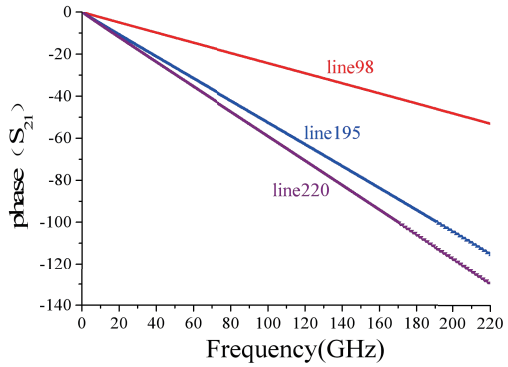

FIGURE 8. Simulated results for line structure.

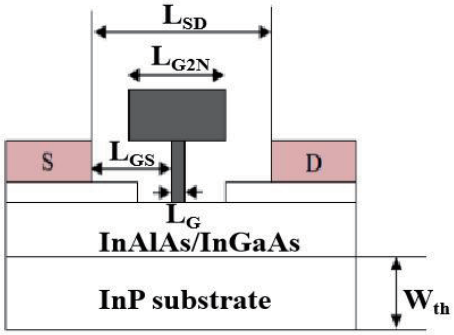

FIGURE 9. Cross section diagram of InP HEMT active area.

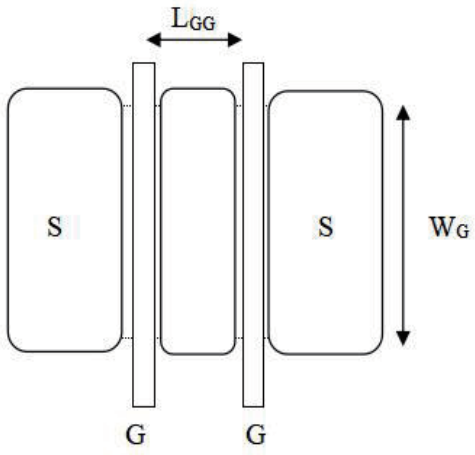

FIGURE 10. Plan view of active devices.

TABLE 1. The scope and meaning of parameters.

Parameters	Parameter range	describe
L_{SD}	2.0 μm ± 0.2 μm	Source drain spacing
L_{GS}	0.95 μm ± 0.1 μm	Grid source spacing
L_G	0.035 μm ± 0.007 μm	grid length
L_{G2N}	0.65 μm ± 0.1 μm	Length of grating cap
W_{th}	50 μm ± 3 μm	Substrate thickness

The simulated results in Figure 8 illustrate the ideal characteristics of standing waves and reflections.

The cross-sectional schematic diagram of the active devices utilized in this paper is presented in Figure 9, accompanied by a comprehensive explanation of the parameter ranges, and their respective meanings are provided in Table 1.

Due to the high frequency and gain of the device under investigation in this paper, it is necessary to appropriately reduce the source-drain distance in order to enhance the maximum current and transconductance while ensuring sufficient breakdown characteristics. Figure 10 illustrates a planar schematic diagram of the active devices employed in this paper, with detailed explanations for each parameter provided in Table 2.

Due to the significant impact of the gate width on device frequency characteristics, it is generally required to decrease the single finger gate width as the frequency increases. Considering the frequency requirements stated in this paper, gate spacing of approximately 10 μm and a single finger gate width about 20 μm are selected to ensure sufficient high-frequency gain. Note that this InP HEMT has been developed by Nanjing Electronic Devices Institute.

3. CALIBRATION TECHNIQUE

The S-parameter measurements were conducted on CPWG topology substrates for extended reference plane devices, covering a frequency range of 0.2–66 GHz and further extended to 220 GHz [17]. Additionally, the LRRM and TRL calibration structures (75–220 GHz) were fabricated on wafer. To de-embed the device S-parameters within the frequency range of 0.2–67 GHz, open/short pads identical to the devices were employed.

TABLE 2. Parameters of plan view of active devices.

Parameters	Parameter range	describe
L_{GG}	$10 \sim 30$ μm	Grid spacing
W_G	$10 \sim 20$ μm	Single finger grating width

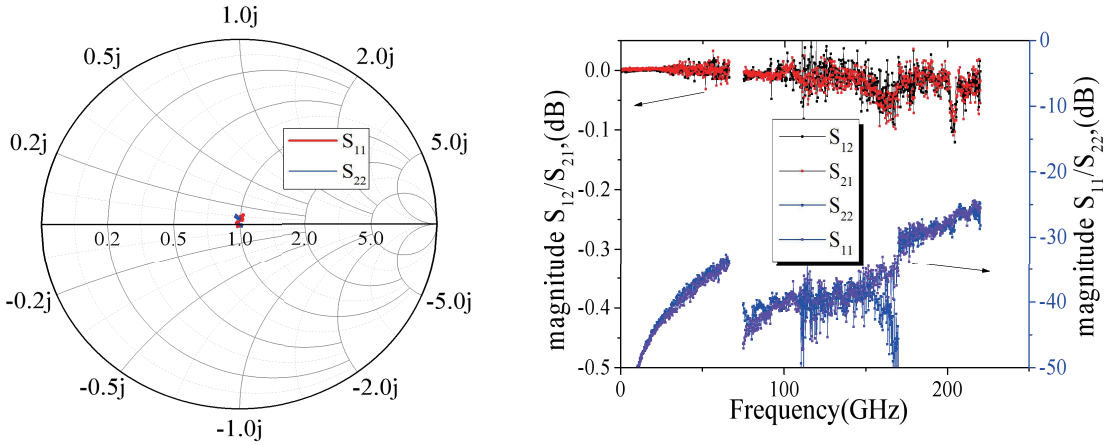

FIGURE 11. TRL calibration verification on "THRU" standard. (a) Smith chart of S_{12}/S_{21}. (b) Magnitude of S parameters.

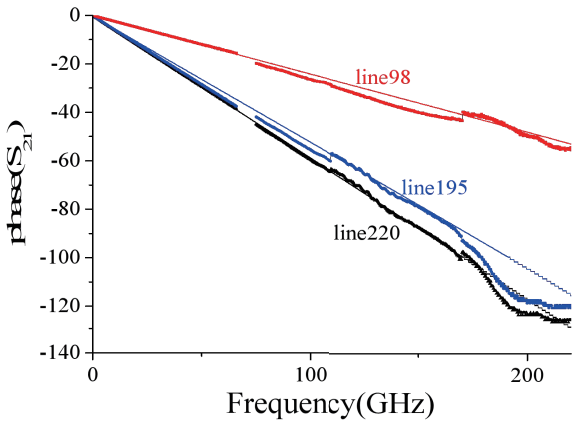

FIGURE 12. TRL calibration verification on "LINE" standard.

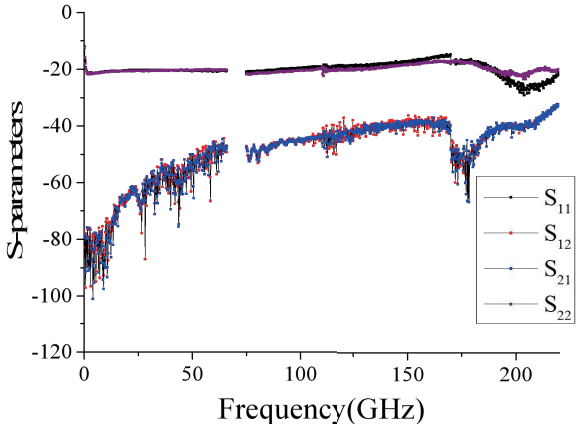

FIGURE 13. LRRM calibration verification on "LOAD" standard.

The experimental setup for the 220 GHz wafer-level measurements involved an Agilent N5227A PNA, equipped with frequency extend modules covering the ranges of 75–110 GHz, 110–170 GHz, and 170–220 GHz. On-wafer calibration was conducted using TRL calibration kits. The verification of calibration on the thru standard within the 220 GHz range is illustrated in Figure 11 [18].

The ideal scenario is for S_{12} and S_{21} to exhibit 0 dB at all frequencies, indicating that all energy flowing into one port will flow out of the other. Consequently, in an ideal case, both S_{11} and S_{22} should be infinitely low as no energy is reflected back. In Figure 11, S_{11} and S_{22} are < -25 dB, and S_{12} and S_{21} are < 0.05 dB, respectively. It demonstrates that the calibration is adequate for extracting reliable device data from measurements [19, 20].

The calibration verification of the line standard in the frequency range of 0.2–220 GHz is illustrated in Figure 12. Accordance with the design principles, the phase difference between the line and thru should fall within the range of 20° to 160°. The chosen line length is 220 μm for W band (75–110 GHz), 195 μm for D band (110–170 GHz), and 98 μm for frequencies ranging from 170 to 220 GHz.

The on-wafer calibration is conducted using LRRM calibration kits. The verification of the calibration on the load standard in the 0.2–220 GHz range is illustrated in Figure 13.

The primary technical challenge encountered in the design of LRRM calibration structure within the terahertz band lies in the observation of a significant deviation in the value of the impedance of the load. As depicted in Figure 4, it is evident that the load structure exhibits commendable performance across a frequency range spanning from 0.2 to 220 GHz.

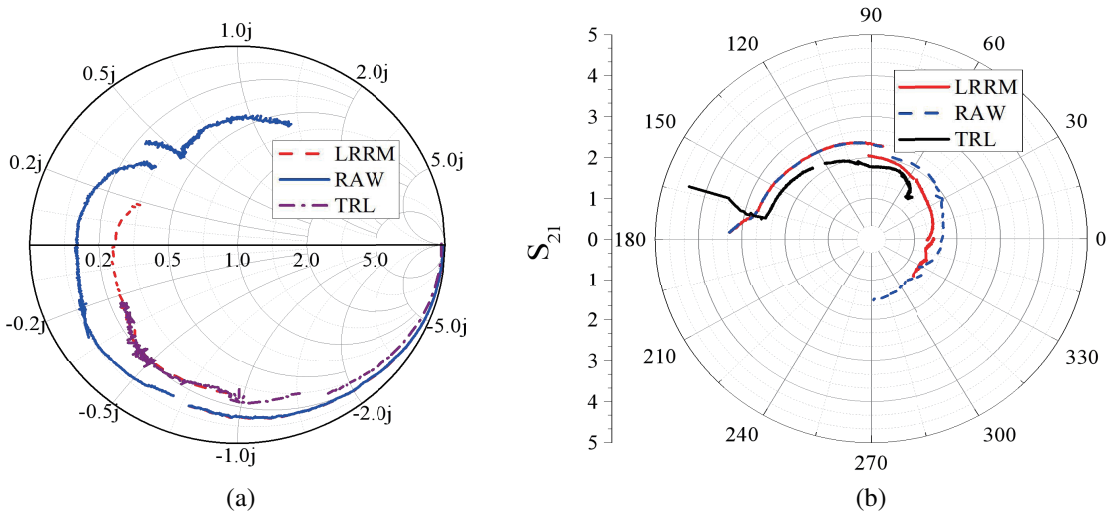

FIGURE 14. Comparisons of raw, LRRM and TRL ($Vds = 1$ V, $Vgs = 0.1$ V) freq (0.2–66 GHz, 75–110 GHz, 110–170 GHz, 170–220 GHz). (a) S_{11}. (b) S_{21}.

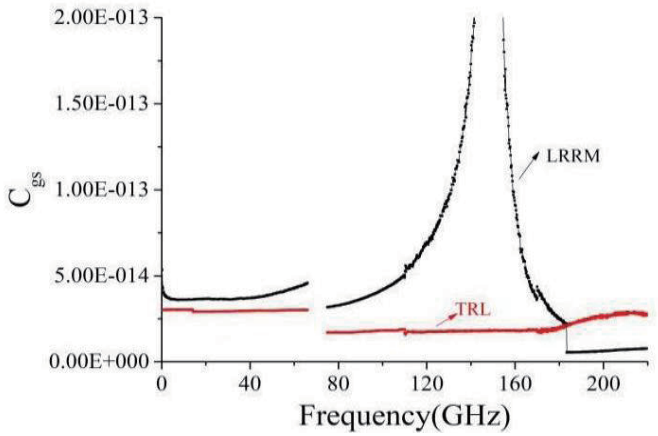

FIGURE 15. Comparison of the extracted device parameters C_{gs}.

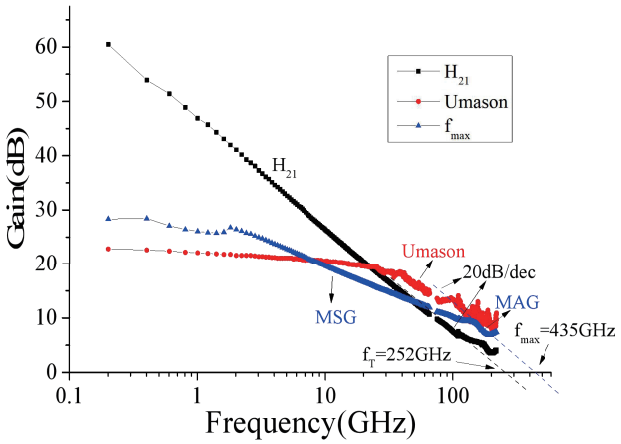

FIGURE 16. H_{21}, MAG/MSG and Umason versus frequency.

4. INP HEMT DEVICE MEASUREMENTS SETUP

Finally, the InP HEMT device is characterized using LRRM calibrations, respectively. The S-parameter comparisons are presented in Figure 14 with a drain bias of 1 V and a gate bias of 0.1 V.

The extracted key device parameter C_{gs} was obtained as depicted in Figure 15. By comparing the two calibration methods, it is observed that below 40 GHz, the extracted C_{gs} exhibits good consistency. However, a significant disparity is observed above 75 GHz. The figure illustrates that the C_{gs} extracted by TRL calibration remains relatively constant above 75 GHz, except for considering the discontinuity of LRRM calibration shows substantial variations which contradict the expected behavior of intrinsic device parameters remaining unchanged with respect to frequency. Hence, TRL calibration methods achieve superior calibration effectiveness.

The results of the two calibration methods differ significantly at high frequencies. The test error of TRL is mainly caused by the inability to completely eliminate interconnect parasitism during the calibration process. In the terahertz frequency band, the presence of interconnection parasitism cannot be ignored, resulting in certain errors in the test results. The LRRM test error is primarily due to the requirement for extremely accurate match preparation, which poses difficulties in accurately preparing loads in the terahertz band and leads to significant errors in this calibration method.

According to the theory [21], the H_{21}, MAG, and Umason values calculated for de-embedding to the device reference planes exhibit a slope of -20 dB/decade, as depicted in Figure 16. The on-wafer TRL calibration demonstrates excellent agreement within the frequency range of 75–110 GHz and provides reliable results within the frequency range of 110–220 GHz. Consequently, TRL calibration is deemed more accurate for measurements in higher frequency bands [22, 23].

The extrapolated f_T from H_{21}, which exhibits a slope of -20 dB/decade, is 252 GHz. Additionally, the extrapolated device fmax based on MSG/MAG and U calculation is determined to be 435 GHz [24].

5. CONCLUSIONS

The paper proposes calibration kits for TRL and LRRM on an InP substrate, covering a frequency test range of 75 to 220 GHz. The phase verification effect of lines with varying lengths is utilized to determine the appropriate lines for each frequency band. Thru and load measurements are employed to validate the TRL and LRRM calibrations, respectively. Furthermore, a comparison is made between the S-parameters obtained through Raw, TRL, and LRRM calibration methods. The extracted C_{gs} demonstrates that this set of TRL calibration structures yields superior testing results primarily due to challenges in accurately preparing loads for LRRM. The current gain cut-off frequency f_T for H_{21} is 252 GHz based on the -20 dB/dectave slope extrapolation, while the extrapolated device maximum oscillation frequency fmax based on MSG/MAG and Umason calculation reaches 435 GHz.

The primary focus of this paper is to analyze the impact of pad parasitism in the terahertz band on test results and the implementation of various on-wafer calibration methods. A comparison is made between the advantages and disadvantages of practical design and preparation techniques for LRRM and multi-line TRL calibration structures, while also presenting measured analysis results up to 220 GHz.

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