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LTCC-Packaged Branch-line Coupler Using Capacitance Improved Capacitor for VHF-Band Applications

Shunjie Yu[1], Bo Zhou[1,*], Gang Shi[1], and Shanwen Hu[1,2]

[1] College of Electronic and Optical Engineering & College of Flexible Electronics (Future Technology)
Nanjing University of Posts and Telecommunications, Nanjing, China
[2] National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing, China

ABSTRACT: A compact branch-line coupler is proposed with capacitance improved capacitor (CIC) using low-temperature co-fired ceramic (LTCC) packaged technology. The proposed CIC is constructed for higher capacitance without any size increment by further separated horizontal finger pads on VIC. The area of the coupler is only $10.3 \times 9.4 \times 1\,\text{mm}^3$, which is equivalent to $0.0041 \times 0.0035 \times 0.0004\lambda g^3$. The application frequency band covers maritime and aircraft navigation in the very high frequency (VHF)-band. The measured in-band S_{11}, S_{21}, S_{31}, and S_{41} are better than -15, -4.1, -2.2, and -18 dB from 47 to 67 MHz, respectively. And the measured phase difference between the coupled and through ports is within $90 \pm 0.2^\circ$, which presents an excellent linear characteristic.

1. INTRODUCTION

Recently, small wireless communication equipment requires smaller components to fit into. Thus, circuit miniaturization is a key consideration when building practical radio frequency (RF) and microwave circuits. Branch-line couplers, also known as quadrature couplers, are fundamental parts utilized in RF circuits like balanced amplifiers, image rejection mixers, beam-forming networks, and phase shifters for array antennas. The coupler working for 30–300 MHz very high frequency (VHF)-band application takes up large size due to the low frequency applications. Thus, coupler miniaturization helps to shrink the size of the entire system. Conventionally, components working for the VHF-band require lumped-elements with higher inductances and capacitances. However, Capacitance lower than 20 pF and inductance lower than 40 nH are impractical to make smaller parts at the VHF-band [1]. Recently, three-dimension (3D) system-in-package technology of low temperature co-fired ceramic (LTCC) uses capacitance increased vertically-interdigital-capacitors (VICs) [2, 3] for circuit miniaturization with high Q-factors [4–9]. GaAs, SiGe, and CMOS have also been used to build compact passive components with lumped elements [10–12]. However, semiconductor process is not appropriate for passive circuit miniaturization when the working frequency is less than 1 GHz, because the required capacitance and inductance are very high. Thus, LTCC process is appropriate to make VHF-band passive components, where high inductance and capacitance are required.

VIC is one of the most common elements used in LTCC-based circuit design. Figures 1(a) and (b) describe the structure of traditional VIC and its equivalent circuit. There are only vertical fingers installed on traditional VIC, which limits its capacitance. The more the quantity of fingers in vertical is, the higher the capacitance reaches. But more quantity of fingers in vertical will lead to more substrate layers, thicker substrate, and thus finally increase fabrication cost. Consequently, increasing capacitance while reminding the VIC's size in both vertical and horizontal directions is vitally important. Although the capacitance increase of VIC is important for miniaturization, few related literatures have been reported in recent years.

During this work, a compact LTCC coupler is made utilizing the proposed capacitance improved capacitors (CICs) for the VHF-band applications. Horizontal finger pads are further divided to formulate additional horizontal couplings for capacitance improvement. By utilizing the proposed CIC, the entire size of the coupler is $0.0041 \times 0.0035 \times 0.0004\lambda g^3$, which reaches a size reduction of 19.6% compared with that mentioned in [2].

2. CIRCUITRY DESIGN

2.1. Coupler's Topology

As the coupler working between 47 and 67 MHz is desired to build for miniaturization, the first step in this design is to have an appropriate circuit topology with a minimal number of capacitors and inductors, because size reduction is the key target. Figures 1(c) and (d) show the selected coupler's model and its corresponding performances of S-parameters. As the bilaterally and longitudinally symmetrical topology can be observed, same valued inductance L and same valued capacitance C are shared by four inductors and three capacitors, respectively. Thus, only two parameters L and C can be simply used to calculate its performance. Also, the circuit analysis is implemented using the even-odd method. The values of L and C in the topology can be considered with Formulas (1)–(2):

$$L = \frac{1}{2\pi f Z_0} \tag{1}$$

* Corresponding author: Bo Zhou (sarahxboy@hotmail.com).

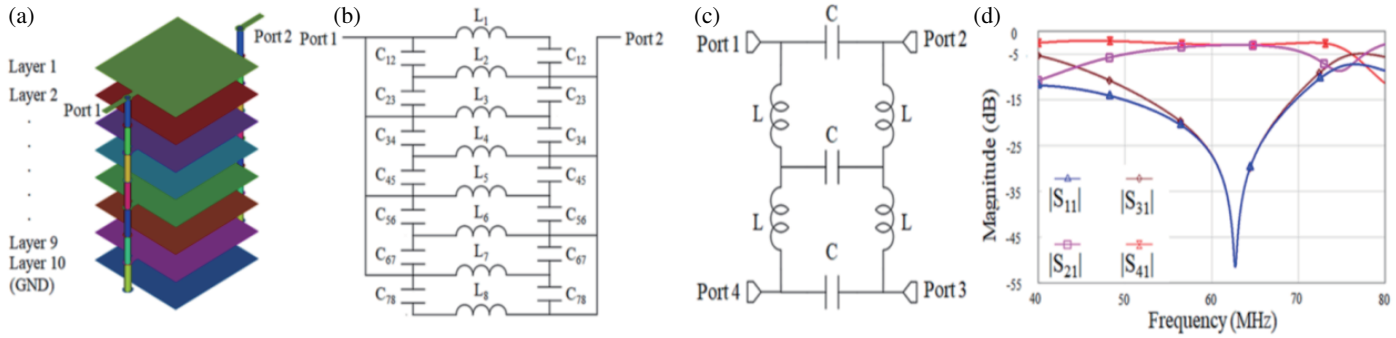

FIGURE 1. (a) 3D structure of traditional VIC, (b) equivalent circuit model of traditional VIC, (c) circuit topology of the coupler and (d) corresponding circuit simulated S-parameters.

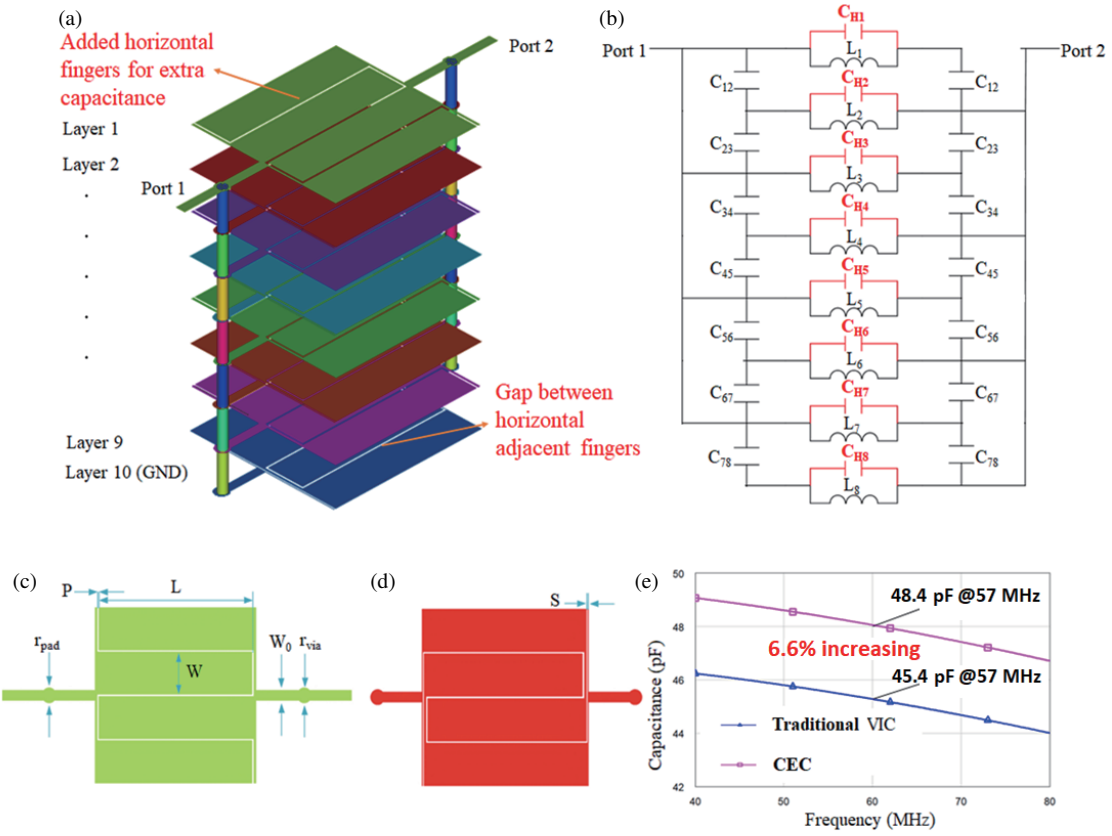

FIGURE 2. (a) 3D structure of the proposed CIC; (b) Equivalent circuit model of CIC; (c) Odd-layer layout of CIC with dimensional parameters; (d) Even-layer layout of CIC with dimensional parameters; (d) The EM-simulated capacitance of CIC and traditional VIC with same size for comparison.

$$C = \frac{Z_0}{2\pi f} \tag{2}$$

where f is the working center frequency, and Z_0 is the port impedance. For the application frequency from 47 to 67 MHz and with the simulation of Cadence MWO simulator [13], $C = 48$ pF and $L = 133$ nH are easily obtained.

2.2. CIC Design

Figure 2(a) presents the proposed CIC with eight vertical fingers, which are embedded into LTCC substrate with 10 layers. Each vertical finger is further separated into four horizontal fingers for gaining extra capacitance. The odd layers are designed with the same dimension parameters and so are the even layers. Thus, the CIC structure can be easily realized. On the even layers, an additional 0.75 turns of capacitance is added to minimize the loss of vertical coupling between vertical layers.

Figure 2(b) shows the equivalent circuit model of CIC. Vertical coupling capacitance between adjacent vertical fingers is represented by this C_{ij}, where i and j are the layer number. L_i stands for the equivalent inductance of microstrip pads, and C_{Hi} stands for the added horizontal coupling. Thus, higher

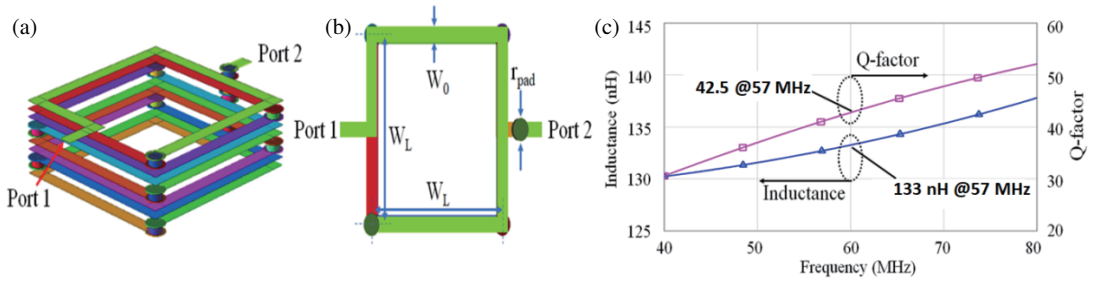

FIGURE 3. (a) 3D structure of the spiral inductor; (b) The planar view with dimensional parameters; (c) The EM-simulated inductance and Q-value of the Spiral inductor.

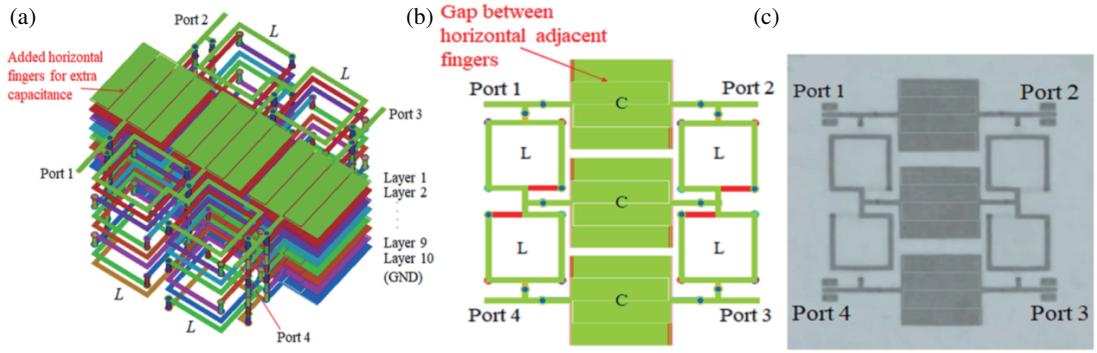

FIGURE 4. The proposed coupler (a) 3D structure. (b) Planar view and (c) photograph.

capacitance is gained due to the added vertical fingers. Figures 2(c) and (d) show the odd- and even-layer's geometry of the CIC, respectively.

For a rough modeling, the distance between horizontal fingers on the same layer is defined by P. The fingers' width and length are described by Wc and L, respectively. In [2], when Wc or P is reduced, the capacitance increases. When L changes, the equivalent capacitance keeps constant. The conductor loss will increase as well if Wc becomes very small. Finally shown in Figure 2(e), the capacitance reached 48.4 pF at 57 MHz. Based on the same dimensions, EM-simulated capacitance of the CIC reached 6.6% higher than traditional one. Furthermore, the parasitic capacitance between the plate and bottom ground becomes much smaller because of the smaller pads.

2.3. Spiral Inductor Design

Because the passband S_{21} is easily affect by spiral inductor's the Q-factor, 9.5-turn inductors with a line width of $W_0 = 0.2$ mm are selected to enhance the Q-factor. The dimension of length and width is set to the same values in order to have a smaller number of parameters to optimize. Figures 3(a) and (b) present the 3D structure and a planar geometry, respectively. Finally shown in Figure 3(c), the capacitance reached 133 nH with a Q-factor of 42.5 at 57 MHz when $W_L = 2.48$ mm.

2.4. Coupler Layout Arrangement

The entire layout of the coupler is shown in Figure 4(a). The three CICs are arranged in parallel form and placed at the center, while four spiral inductors are situated around. The whole coupler is implemented and packaged with LTCC materials with 10 layers. The dielectric constant of 5.9, each layer's thickness of 0.1 mm and loss tangent of 0.002 are all taken into the consideration when simulation and optimization are implemented. Full-wave electromagnetic (EM) simulator Cadence Analyst [14] is used to finally fix the final dimensions. Thus, final dimensions are listed: $W = 0.5$ mm, $W_0 = 0.2$ mm, $W_C = 0.83$ mm, $W_L = 2.5$ mm, $L = 3.25$ mm, $S = 0.02$ mm, where the parameters are defined in Figures 2(c), (d), and Figure 3(b).

3. RESULTS AND COMPARISONS

The EM-simulated and measured performances of S-parameters are both plotted in Figure 5(a). Measurements are carried out by cascaded summit 200 probe station and ZNB8 network analyzer from Rohde & Schwarz. The measured S_{11}, S_{21}, S_{31}, and S_{41} are superior to -15, -4.1, -2.2, and -14 dB from 47 to 67 MHz, respectively. The zoom in of S_{21} and S_{31} parameters are plotted in Figure 5(a) for a detailed observation. Observed in Figure 5(b), the through and coupled ports' measured phase difference is within $90 \pm 0.2°$, and a less than 1.9 dB measured amplitude imbalance from 47 to 67 MHz is obtained, which presents an excellent linear characteristic.

Performance comparison with literatures is presented in Table 1. The coupler reached a very tiny size of only $0.0041 \times 0.0035 \times 0.0004\lambda g^3$, where λg is the guided wavelength on the 1-mm thick Ferro-A6 material substrate at the center frequency of 57 MHz. The proposed coupler reduced 19.6% size compared with that in [2]. Among the literatures [2–6, 11–13], the

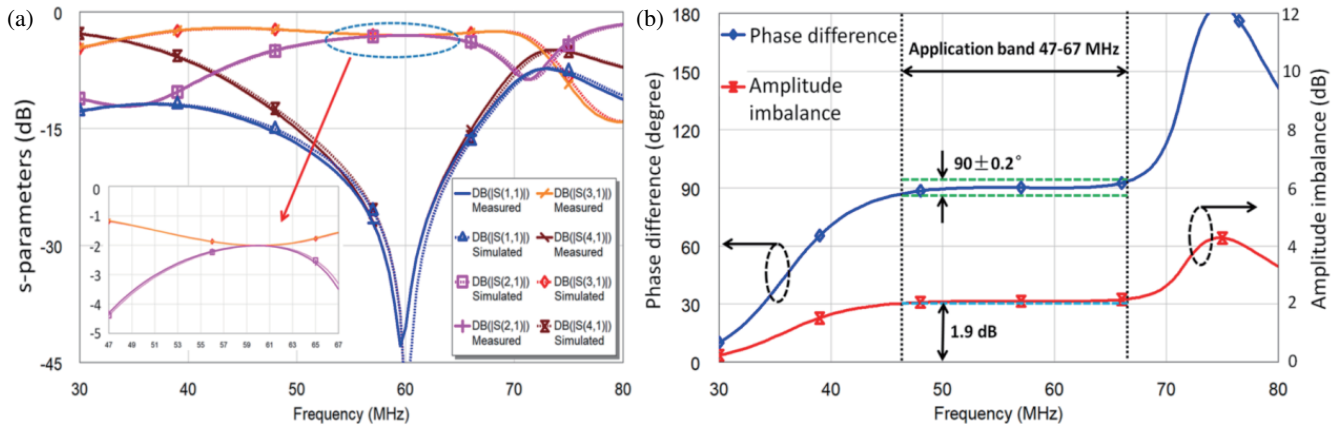

FIGURE 5. (a) EM-simulated and measured S-parameters and (b) Measured phase difference between the through and coupled ports, and measured amplitude imbalance.

TABLE 1. Size and performance comparisons.

Ref.	Center frequency (GHz)	FBW based on 15 dB return loss	Return loss (dB)	Isolation (dB)	Amplitude imbalance (dB)	Phase difference (degree)	Overall size (λg^3)	Process
2	0.06	182%	15	12	2.8	±1	$0.005 \times 0.004 \times 0.0004$	LTCC
3	0.1	213%	14	12	1.9	±2	$0.0045 \times 0.0045 \times 0.0004$	LTCC
4	2.5	136%	15	13	3.5	±2	$0.25 \times 0.19 \times 0.0114$	PCB
5	1.5	1894%	12	10	2	±1	$0.1385 \times 0.0458 \times 0.0238$	PCB
6	0.87	888%	15	13	2.1	±1.4	$0.11 \times 0.11 \times 0.0035$	PCB
10	5	20%	15	14	2.2	±2	$0.02 \times 0.01 \times 0.003$	GaAs
11	55	27%	14	13	3.1	±1.5	$0.04 \times 0.02 \times 0.009$	SiGe
12	90	29%	15	12	2.4	±1	$0.028 \times 0.018 \times 0.04$	CMOS
This work	0.57	323%	15	14	1.9	±0.2	$0.0041 \times 0.0035 \times 0.0004$	LTCC

Note: Data are estimated from the literature

coupler reached the tiniest reported size, lowest amplitude imbalance, highest return loss, maximum isolation, and minimum phase difference.

4. CONCLUSION

A compact LTCC-packaged coupler is proposed and implemented for VHF-band applications. For circuit miniaturization, CIC is proposed with additional separated horizontal fingers for capacitance increasing without horizontal and vertical size expanding. The overall circuit area is $0.0041 \times 0.0035 \times 0.0004\lambda g^3$, which leads to a 19.6% size reduction compared with traditional coupler. Additionally, very low phase imbalance and amplitude imbalance are both reached. The proposed coupler has broad application fields in VHF-band aircraft and maritime navigation systems.

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