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An On-Chip Integrated Current Sensing Technology for Real-Time Detection of Phase Current in BLDC Motors

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ABSTRACT: This paper presents an on-chip integrated sensing circuit for real-time detection of phase currents in three-phase brushless direct current (BLDC) motors. The three-phase sinusoidal currents generated in the motor winding are detected by an innovative Sense FET technology, which can accurately measure the currents of high side and low side power transistors simultaneously. A dynamic matching elimination method is proposed for the detection current mismatch problem due to the large difference in aspect ratio. Using a 90 nm BCD process for design and verification, the detection circuit of the high side and low side can well follow the change of sine wave phase current of the three-phase motor. The detection accuracy is above 96%, and the best accuracy can reach 99.219%. The elimination effect of circuit current mismatch is obvious, and the error of the sensing current can be reduced by 38.9%.

1. INTRODUCTION

BLDC motor drive has a wide range of applications in intelligent motion control systems and has gradually penetrated into industrial control, smart home, automotive, automation systems, healthcare equipment, and aerospace fields, and plays an increasingly important role [1, 2]. Phase current detection in a three-phase motor drive system is an important factor affecting the cost and performance of the system. By monitoring the current signal of the motor winding, information about the position and torque can be obtained, and only if the current detection is accurate, the coordinate conversion of vector control can be correct. In some applications, it is necessary to obtain current information on the motor winding to display and track changes of the load current. The real-time detection of motor phase current is also of great significance for monitoring motor status and detecting overcurrent and other faults in a timely manner [3, 4].

At present, the detection methods of motor current mainly include resistance sampling, hall current sensor, and MOSFET RDS(on) detection as shown in Fig. 1. The first method is widely used in a variety of motor drive systems due to its low cost, small size, and simple structure. It usually involves connecting a power resistor to the motor's off-chip phase line or DC bus. However, since all the drain current of the power transistors must pass through the sampling resistor, a large power loss will be generated at the sampling resistor. At the same time, this method has a sampling blind spot, and it cannot detect the current when each sector is switched during the motor rotation [3]. Hall current sensor is also an off-chip motor current detection method, with high sampling accuracy and galvanic isolation [5, 6]. It can realize contactless detection of the motor phase current. However, most of the hall current sensors are separate integrated devices, and calibration is required before use. The off-chip current sensing methods mentioned above all require additional devices to implement and cannot be highly integrated, which increases the cost and area of the system [7–10]. The MOSFET RDS(on) method requires no additional devices or circuit structures, enabling simple and low-cost current detection [4]. However, since the RDS(on) varies greatly with temperature and is affected by the parasitic inductance of the package form, it is easy to cause poor detection accuracy.

As the need for high accuracy, high efficiency, high integration, and low cost increases, traditional series resistors sensing or similar passive circuits can be replaced by current sensing MOSFETs [11–13]. In this paper, a current detection method based on sense field effective transistor (FET) technology is proposed, which has the characteristics of high accuracy and is suitable for on-chip integration. It is the simplest and most effective method to obtain real-time motor winding current and achieve lossless current detection. Compared with other methods, sense FET current sensing can simplify the circuit design, but due to the large difference in aspect ratio between the power transistor and sensing transistor, there will be a current mismatch [14, 15]. The amount of mismatch is directly reflected in the error between the detected current and actual current, which has a great impact on the accuracy. The dynamic element matching (DEM) technique proposed in this paper is very effective in reducing the random mismatch of the current mirror, and this method does not introduce additional power loss to the sense FET.

The proposed BLDC motor current detection system design is described in Section 2. The implementation of critical circuits is covered in Section 3. The simulation results are shown in Section 4. The paper is summarized in Section 5.

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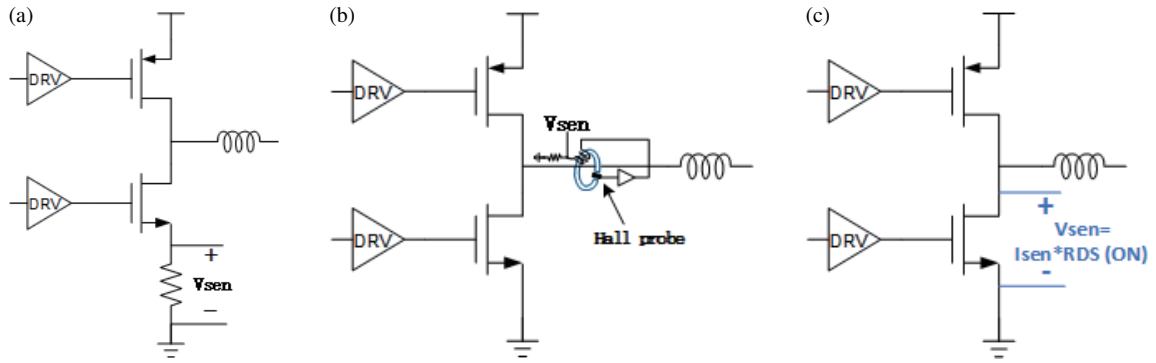

FIGURE 1. Traditional current detection methods: (a) series resistance sensing; (b) hall current sensor; (c) MOSFET RDS(on) detection.

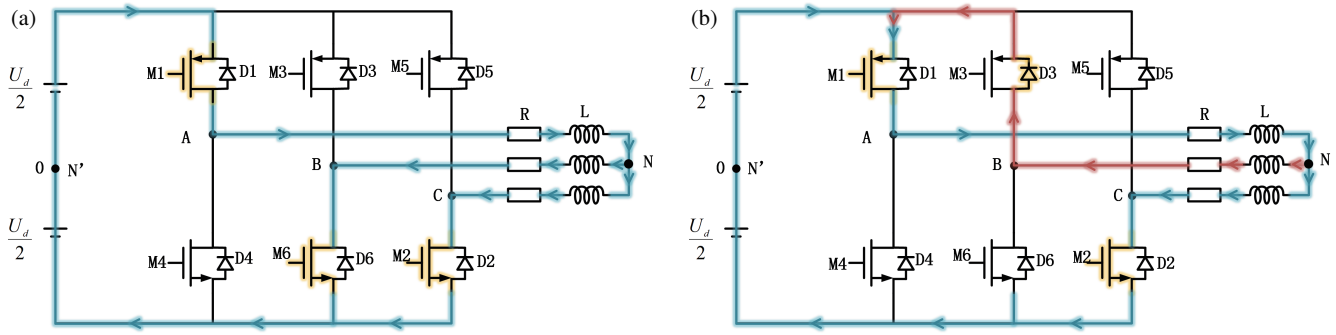

FIGURE 2. (a) Three-phase inverter bridge M6M1M2 conduction phase and; (b) M1M2D3 freewheeling phase current flow diagram.

2. SYSTEM DESIGN

2.1. BLDC Motor System Structure and SPWM Modulation Mode

The modulation method used in the three-phase BLDC motor drive system in this paper is sinusoidal pulse width modulation (SPWM). According to the impulse equivalent principle, the PWM waveform equivalent to the sinusoidal signal can be generated by comparing the isosceles triangular carrier wave with the sinusoidal modulation wave [16–18]. The SPWM signal controls the conduction and shutdown of each power transistor in the three-phase inverter bridge circuit to output the desired voltage waveform.

The three-phase inverter bridge consists of six power transistors. Each bridge arm is of a $P + N$ structure, and the load is a three-phase motor winding connected into a star pattern. There are six conduction states in one cycle of motor rotation, which are controlled by the SPWM signal in the conduction order of M5M6M1 → M6M1M2 → M1M2M3 → M2M3M4 → M3M4M5 → M4M5M6 as shown in Fig. 2. Taking the phase change processes of M6M1M2 → M1M2M3 as an example, the direction of current flow in the inverter bridge during this process is shown in Fig. 2(a). Since the direction of the current on the load inductor cannot change abruptly, the commutation process cannot be completed instantaneously, that is, M3 cannot be turned on immediately. At this time, the current must go through the bulk diode D3 of M3 for freewheeling as shown in Fig. 2(b). After the load current drops to 0, M3 is turned on. The principle of the remaining five phase change processes is also the same and will not be repeated here.

After the above six state cycle switching, the output three-phase sinusoidal current forms a circular rotating magnetic field in the motor space, which generates a constant electromagnetic torque and drives the motor to rotate. Fig. 3 shows the three-phase inductor current waveform. The solid part of the current is the inductor current when the power transistor is on, and the dotted part is the freewheeling current. Since the freewheeling current is equal to the conduction current in the opposite direction, and it is exactly a discharge process of the current generated when the power transistor is turned off, it is only necessary to detect the current value of the conduction part during the current detection, that is, the solid line part in Fig. 3.

2.2. Current Detection System

The structure block diagram of the proposed three-phase BLDC motor phase current detection system is shown in Fig. 4, which is mainly composed of drive, protection, current detection, and other circuit blocks. Current detection block is divided into high side and low side detections. The detected current is converted into voltage and sent to the positive input of the comparator to compare with Vref. If the over-current occurs, the logic control block will cut off the power transistor to avoid circuit damage.

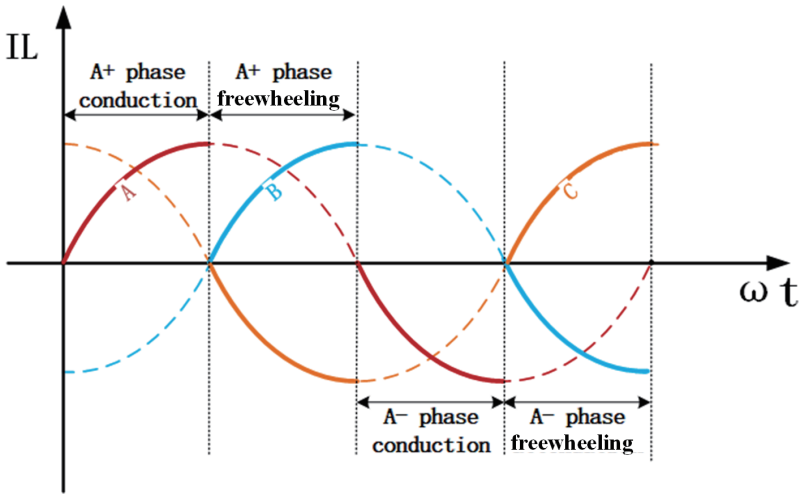

FIGURE 3. A, B, C three-phase inductor current conduction and freewheeling diagram.

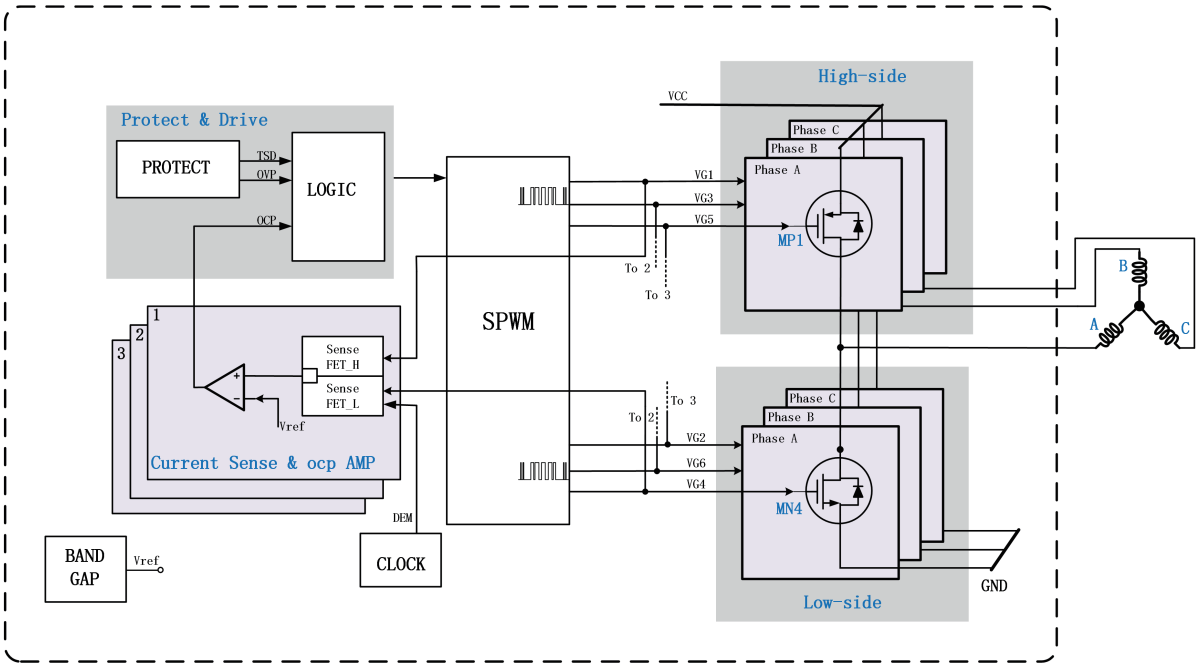

FIGURE 4. Overall block diagram of three-phase BLDC motor current detection system.

3. CIRCUIT IMPLEMENTATION

3.1. Sense FET Current Detection Circuit

The basic principle of sense FET circuit is: the currents of the power transistor MP and MN are proportionally mirrored by the sensing transistor MPS and MNS, respectively. As shown in Fig. 5(a), the two pairs of transistors are driven by the same gate voltage signal P and Q, and the channel lengths are equal. Their aspect ratios are $1:K1$ and $1:K2$, where $K1$ and $K2 \gg 1$. Take high side detection as an example, if the source voltage of the sensing transistor and power transistor can be clamped at the same electric potential, Eq. (1) can be obtained, where R_{DS_MP} and R_{DS_MPS} can be expressed as Eq. (2). Then, the ratio of the power transistor current I_{MP} to the sensing current I_{MPS} is also equal to $K1$, as shown in Eq. (3). During the detection, we only need to measure I_{MPS} at the output and multiply it by the corresponding proportionality factor $K1$, and we can accurately derive the output current of the power transistor, so that the current can be monitored in real-time.

$$V_{DS\_MP} = V_{DS\_MPS},\ I_{\mathrm{MP}} R_{DS\_MP} = I_{\mathrm{MPS}} R_{DS\_MPS} \quad (1)$$

$$R_{DS\_MP} = \frac{1}{\mu_p C_{ox}(W/L/K1)(V_{GS} - V_{TH})},$$

$$R_{DS\_MPS} = \frac{1}{\mu_p C_{ox}(W/L)(V_{GS} - V_{TH})} \quad (2)$$

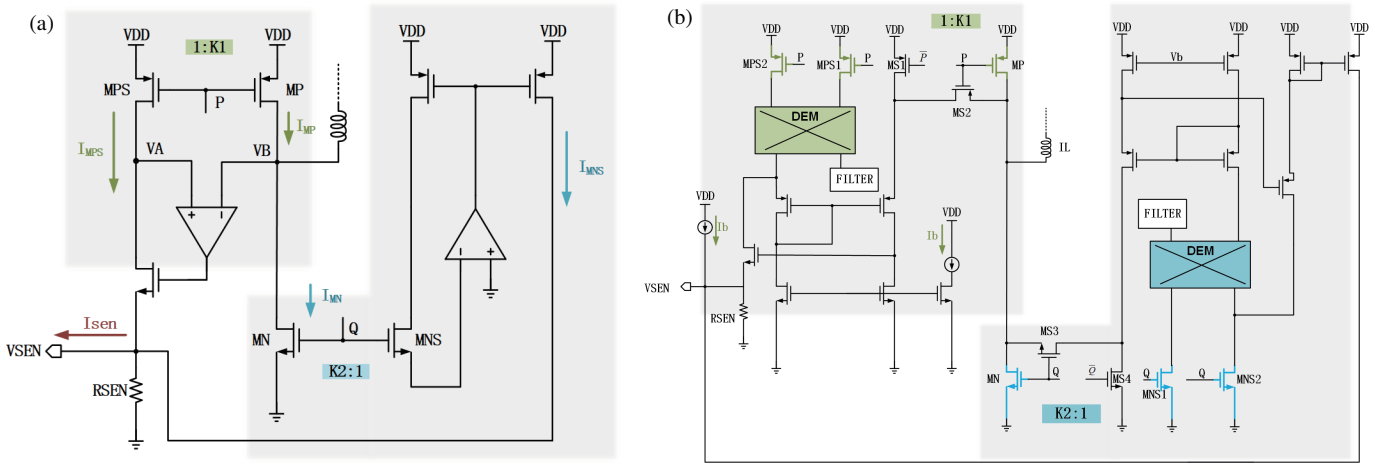

FIGURE 5. (a) Circuit structure sketch of conventional current detection method and; (b) Circuit structure diagram of proposed current detection method.

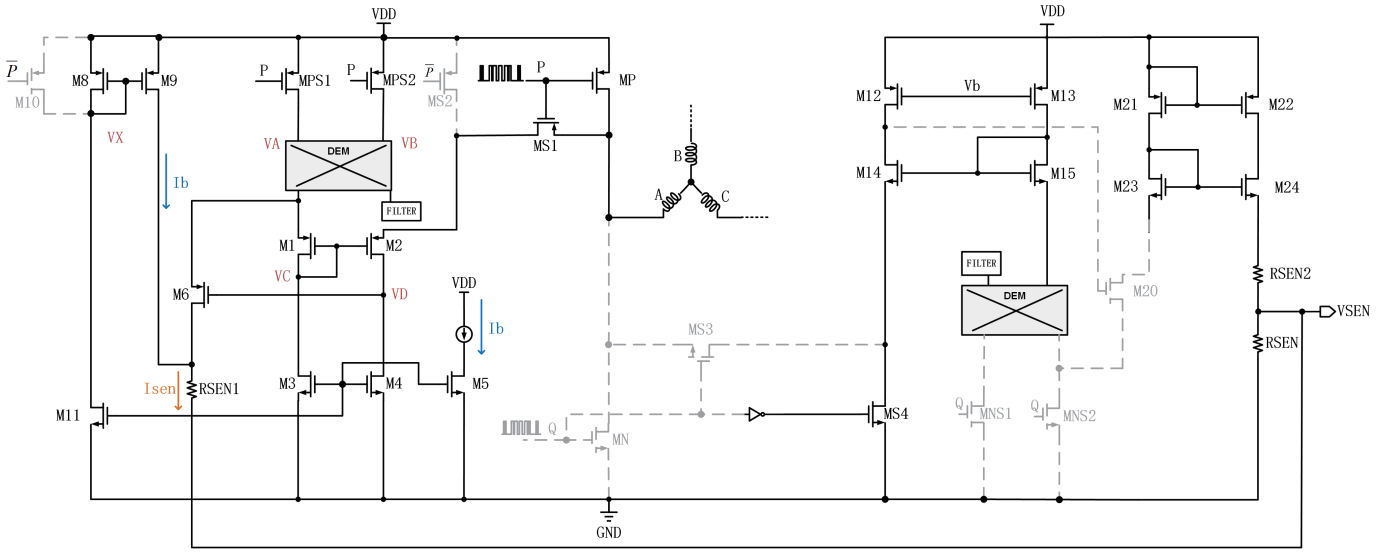

FIGURE 6. High side current detection circuit diagram.

$$I_{\mathrm{MPS}} = \frac{I_{\mathrm{MP}}}{K1} \tag{3}$$

The conventional circuit structure uses the "virtual short" and "virtual open" principle of the amplifier to ensure that the voltages of VA and VB are equal [20, 21], as shown in Fig. 5(a). The accuracy of this method is limited by the compensation capacitance and bandwidth of the amplifier, which is very demanding for the design of the op-amp. It is not suitable for the detection of the motor phase current. Fig. 5(b) is the proposed sense FET current detection circuit in this paper. The common gate amplifier feedback structure is used to replace part of the amplifier in Fig. 5(a), which simplifies the circuit structure and reduces power consumption while ensuring the accuracy. At the same time, considering the influence of the inevitable mismatch between power transistor and sensing transistor with large proportional coefficient on the detection accuracy, a method of using DEM to reduce the random mismatch is proposed, which will further improve the detection accuracy.

When voltage signal P is low, the power transistor MP is turned on, and the high side current detection part, which is the solid-line part of the circuit in Fig. 6, begins to work. MPS1 and MPS2 are sensing transistors. The size of the high and low sides power transistor is determined according to the peak current requirement of the circuit. The size of the sensing transistor is selected by considering the power transistor, chip area, and power consumption. Therefore, the width-to-length ratio coefficient K1 is set to 930, and K2 is set to 910. MS1 and MS2 are state switches. MS2 is controlled by the voltage opposite to P. When the high side detection circuit does not work, the VB point voltage is maintained at VDD, which is convenient for the next high side power transistor to enter the current detection state faster, thereby reducing the establishment time when the

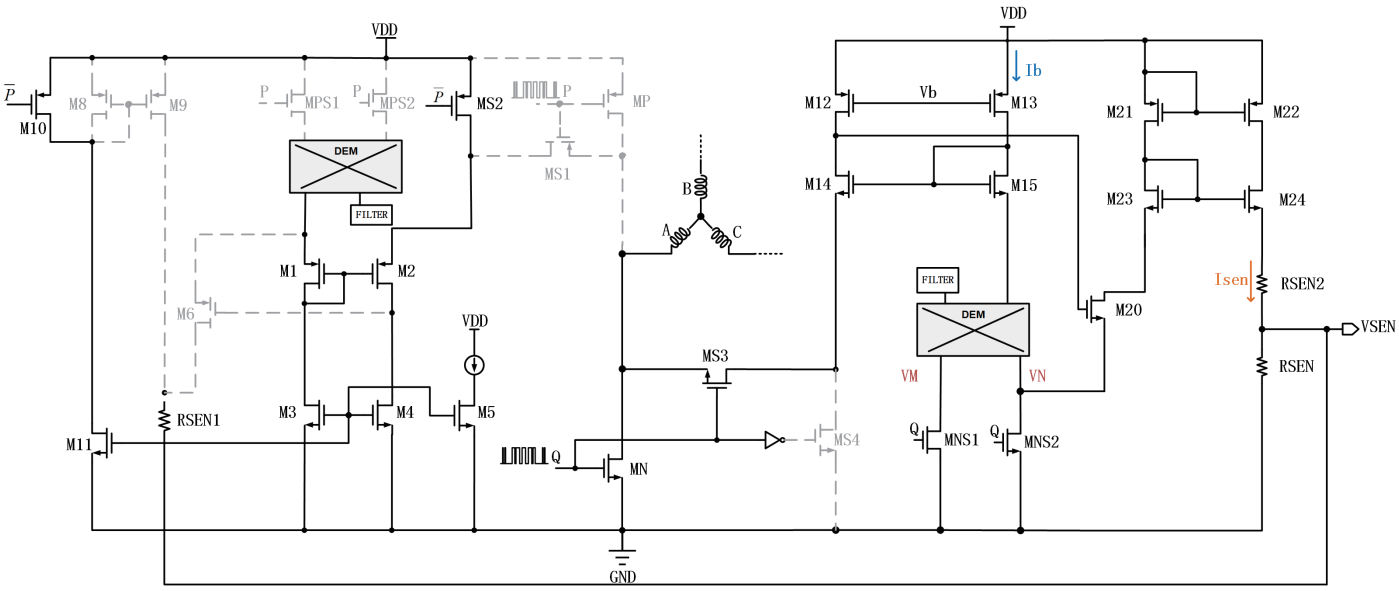

FIGURE 7. Low side current detection circuit diagram.

high and low sides are switching and improving the response speed of the circuit. When the high side power transistor is on, M10 is closed, and M8 and M9 are on to provide a compensation current equal to Ib for the output; when the upper transistor MP is off, the M10 transistor is on; the VX point voltage is pulled up to VDD; M8 and M9 are closed, thereby cutting off the current compensation branch and reducing the power consumption of the high side current detection part. During the high side detection stage, MP, MPS1, and MPS2 are on. The current I_{MPS1} of the sensing transistor MPS1 flows at node VA to the two branches where M1 and M6 are located, respectively. The current relationship is shown in Eq. (4):

$$I_{\text{MPS1}} = I_{M1} + I_{M6} \tag{4}$$

The relationship between the current I_{MP} of MP and I_{MPS1} of MPS1 is shown in Eq. (5):

$$I_{\text{MP}} = K1 \times I_{\text{MPS1}} \tag{5}$$

Due to the current mirror structure, the currents flowing through M1, M2, and M9 are all equal to the bias current I_b:

$$I_{M1} = I_{M2} = I_{M9} = I_b \tag{6}$$

In other words, the proposed current compensation circuit structure can compensate the current I_b lost at VA by the sensing current I_{MPS1} to ensure that the output sensing current I_{sen} is more accurate, which is expressed as Eq. (7):

$$I_{sen} = I_{M6} + I_{M9} = I_{\text{MPS1}} = \frac{1}{K1} \times I_{\text{MP}} \tag{7}$$

The key to form the current detection is $VA = VB$, and the negative feedback effect of M6 can ensure the realization of this condition. For example, when VA increases, I_{MPS1} will decrease due to Eq. (8), and the current of M6 becomes smaller so that the detection current becomes smaller. Since M6 works in the saturation region, the current can be expressed as Eq. (9), so VD must increase, and VB will also increase, and vice versa.

$$I_{\text{MPS1}} = \mu_p C_{ox}(V_{DD} - |V_{TH}|)(V_{DD} - V_A) \tag{8}$$

$$I_{M6} = \frac{1}{2}\mu_p C_{ox}[(V_A - V_C) - |V_{TH}|]^2 \tag{9}$$

When the gate drive signal Q is high, MP is turned off, and MN is turned on. The low side current detection part, which is the solid line part of Fig. 7, begins to work. MNS1 and MNS2 are sensing transistors. MS3 and MS4 are state switches. The drive signal of MS4 is reverse to Q. When MN is turned off, the sensing circuit is separated from the power stage. Meanwhile, MS2 is turned on, and the voltage of the node VB is raised to VDD to keep the amplifier active during the turn-off stage. Maintain the current path of the current source at VB so that the sensing part of the next cycle can quickly enter the working state and improve the response time. The working principle of the low side detection is similar to the high side, and the negative feedback of M12, M13, M14, M15, and M20 is used to ensure that VM and VN are clamped at the same voltage. The detection currents of high side and low side are converted to a voltage output from the VSEN port via the RSEN resistor.

The accuracy η_1 and η_2 can be expressed as Eq. (10) and Eq. (11), where $I_{sen(MP)}$ and $I_{sen(MN)}$ represent the final output sensing currents of the compensated high side and low side detections, respectively:

$$\eta_1 = \frac{|I_{\text{MP}} - K1 \times I_{sen(MP)}|}{I_{\text{MP}}} \tag{10}$$

$$\eta_2 = \frac{|I_{MN} - K2 \times I_{sen(MN)}|}{I_{MN}} \tag{11}$$

3.2. DEM Mismatch Reduction Circuit

Device mismatch refers to the inevitable variation and offset of electrical parameters between transistors in the process of

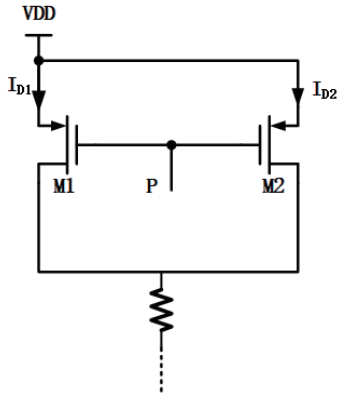

FIGURE 8. Simplified model diagram of current detection.

manufacturing, including deterministic mismatch and random mismatch. The deterministic mismatch is caused by unreasonable layout design, which can be eliminated by optimizing layout and circuit design. Random mismatch is caused by the irrational factors of the process, which leads to the change of transistor parameters and cannot be avoided. The mismatch of threshold voltage V_{th} in random mismatch has a great influence on circuit performance and current detection accuracy [17, 18].

The circuit based on sense FET proposed in this paper has a large width-to-length ratio between the sensing transistor and power transistor, and the mismatch of the devices is obvious, which will reduce the accuracy. The main structure of the detection circuit is abstracted into a simple current mirror structure of Fig. 8 for mismatch analysis, assuming that M1 and M2 have the same length and $W_1 = K * W$, $W_2 = W$.

Considering the deviation of the threshold voltage V_{th}, there is Eq. (12):

$$\left(\frac{\sigma(I_D)}{I_D}\right)^2 = \left(\frac{g_m}{I_D}\right)^2 \sigma^2(V_{th}) \tag{12}$$

According to the definition of mismatch, it can be concluded that:

$$\sigma^2(V_{th}) = \frac{1}{2}\sigma^2(\Delta V_{th}) = \left(\frac{A_{Vth}}{2WL}\right)^2 \tag{13}$$

where ΔV_{th} is the difference between the thresholds of M1 and M2, and A_{Vth} is the threshold voltage mismatch coefficient. Therefore, the mismatch variance of I_{D1} is:

$$\left(\frac{\sigma(I_{D1})}{I_{D1}}\right)^2 = \left(\frac{g_{m1}}{I_{D1}}\right)^2 \times \left(\frac{A_{Vth}}{2W_1L}\right)^2 \tag{14}$$

where I_{D1} is the current of M1. Similarly, the mismatch variance of I_{D2} can be expressed as:

$$\left(\frac{\sigma(I_{D2})}{I_{D2}}\right)^2 = \left(\frac{g_{m2}}{I_{D2}}\right)^2 \times \left(\frac{A_{Vth}}{2W_2L}\right)^2 \tag{15}$$

where I_{D2} is the current of M2. Therefore, the STD ratio of current mismatch "M" can be expressed as:

$$\frac{\sigma(M)}{M} = \sqrt{(\frac{g_{m1}}{I_{D1}})^2 \times \left(\frac{A_{Vth}}{2W_1L}\right)^2 + (\frac{g_{m2}}{I_{D2}})^2 \times (\frac{A_{Vth}}{2W_2L})^2} \tag{16}$$

Because $W_1 = K * W$, $W_2 = W$, $I_{D1} = K * I_D$, $I_{D2} = I_D$, $g_{m1} = K * g_m$, $g_{m2} = g_m$, Eq. (16) can be expressed as Eq. (17):

$$\frac{\sigma(M)}{M} = \sqrt{\left(\left(\frac{g_m}{I_D}\right)^2 \times (\frac{A_{Vth}}{2WL})^2\right)(K+1)} = \frac{g_m}{I_D}\frac{A_{Vth}}{2WL}\sqrt{K+1} \tag{17}$$

It can be seen from Eq. (17) that the larger the K is, the greater the effect of mismatch is on the current mirroring results. Therefore, the amount of mismatch needs to be eliminated.

In this paper, a DEM circuit is added to the high and low sides of the current detection to reduce the mismatch. We added two sensing transistors, MPS2 and MNS2, to change the traditional $1:K$ current detection circuit into a $1:1:K$ structure.

The DEM circuit is controlled by the two-phase non-overlapping clock CLK1 and CLK2. The schematic diagram is shown in Fig. 9(a). The input ports in_1 and in_2 are connected to two sensing transistors. Under the control of the clock signal with a duty cycle of 50% shown in Fig. 9(c), the two sensing transistors MPS1 and MPS2 on the high side and the two sensing transistors MNS1 and MNS2 on the low side are alternately connected into the detection circuit. The mismatch is eliminated in the uniform alternating distribution process. The circuit structure is shown in Fig. 9(b).

4. SIMULATION AND EXPERIMENTAL RESULTS

The proposed BLDC motor current detection system is fabricated in a 90 nm CMOS process. The layout is shown in Fig. 10. The chip area is 935 µm × 1465 µm; the area of three-phase inverter power transistor is 935 µm × 410 µm; and the area of predrive circuit and current detection circuit is 120 µm × 225 µm. The motor drive system is simulated under the condition of input voltage $VDD = 5$ V, frequency of 20 kHz, and three-phase inductance load $L = 280$ µH. As shown in Fig. 11, the output motor current is a stable three-phase sine wave with a peak current of around ±500 mA.

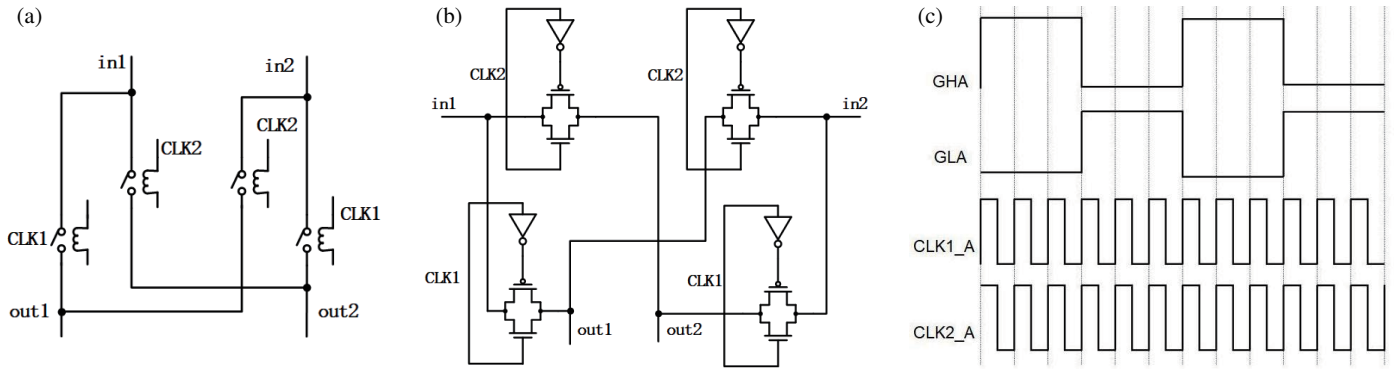

FIGURE 9. (a) Proposed DEM structure diagram; (b) DEM circuit diagram; (c) Two non-overlapping clock timing diagrams.

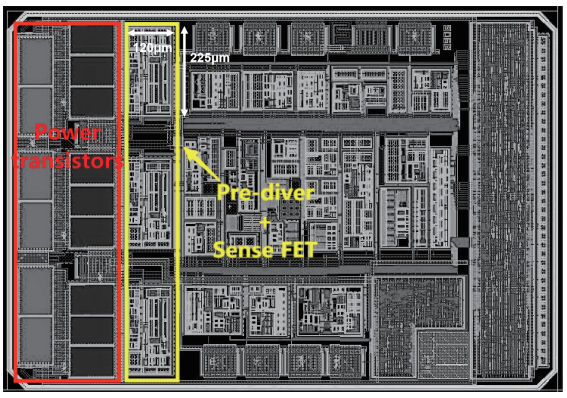

FIGURE 10. The layout of the BLDC motor drive system.

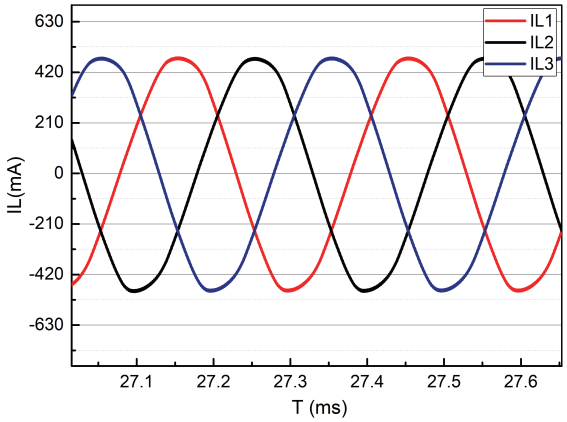

FIGURE 11. Three Phase Current Simulation Waveform of Motor Drive System.

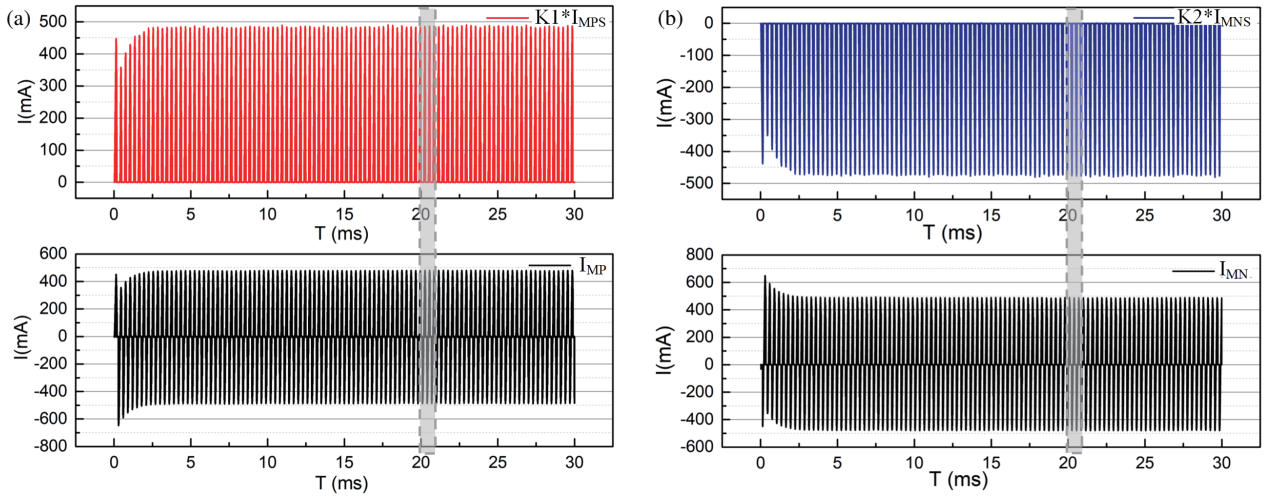

FIGURE 12. (a) Single-phase bridge arm P-type transistor current and sensing current waveform of the proposed circuit and; (b) Single-phase bridge arm N-type transistor current and sensing current waveform of the proposed circuit.

Figures 12(a) and 12(b) show the current waveforms of the high side power transistor current I_{MP} and sensing current I_{MPS}, the low side power transistor current I_{MN} and sensing current I_{MNS} in the conduction phase. For the convenience of comparative observation, the sensing current is multiplied by the respective detection proportional coefficients K1(930) and K2(910). After the stable rotation of the motor, the current waveform is partially amplified as shown in Fig. 13(a) and

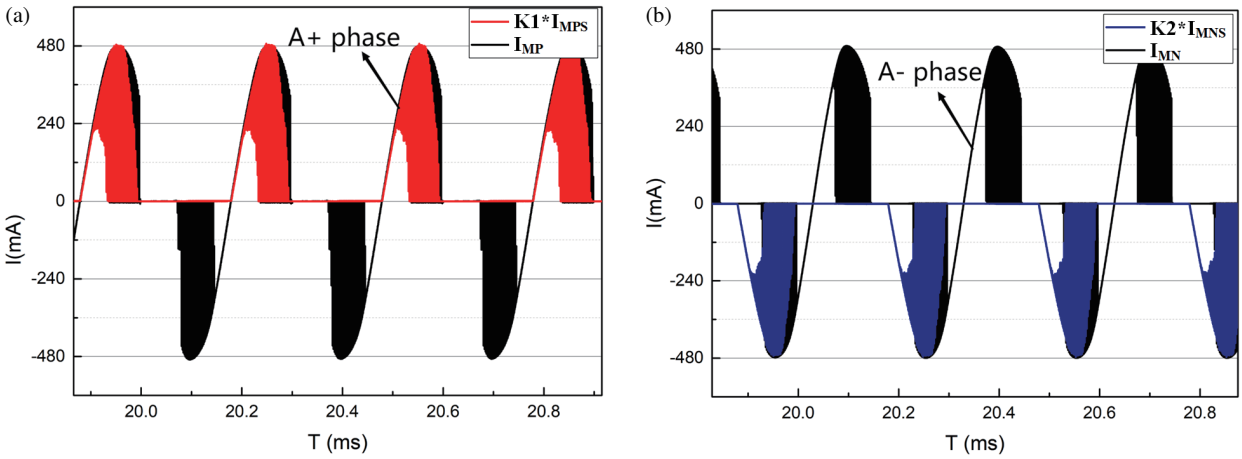

FIGURE 13. (a) Current detection waveform of A+ phase transistor and; (b) Current detection waveform of A- phase transistor.

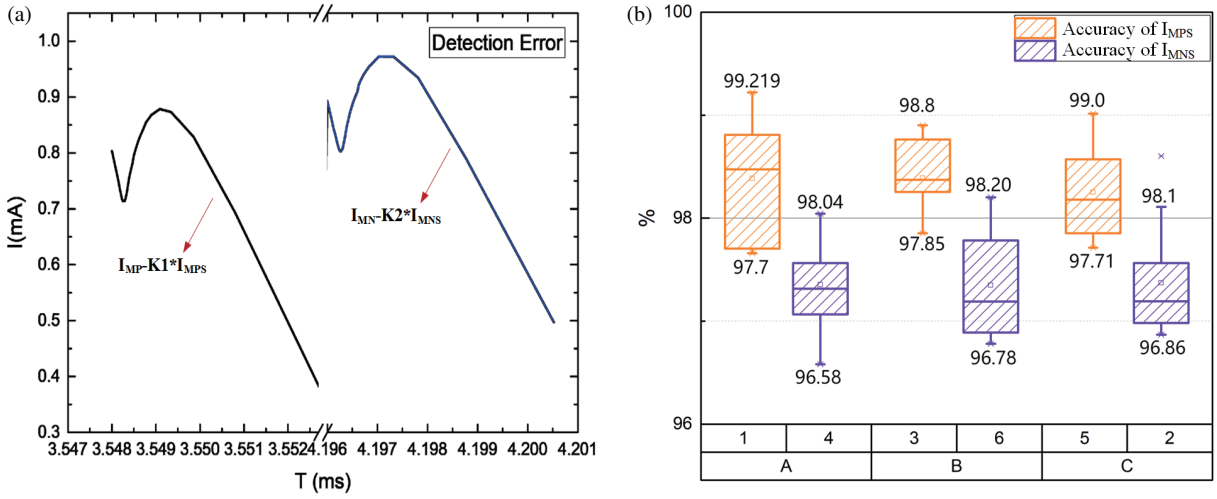

FIGURE 14. (a) Detection error curve of high side and low side in one conduction period and; (b) Box diagram of current detection accuracy of each power transistor in three-phase bridge.

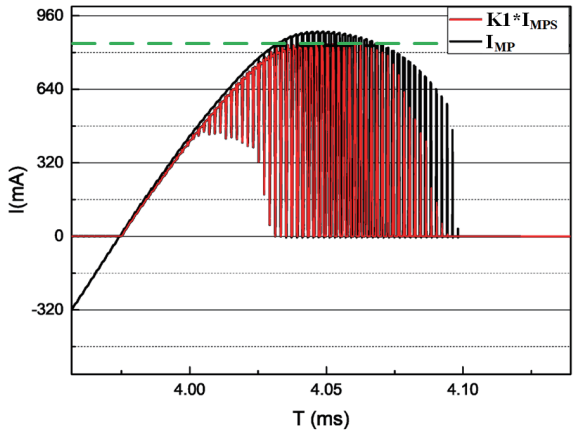

FIGURE 15. Maximum current that can be detected by the current detection circuit.

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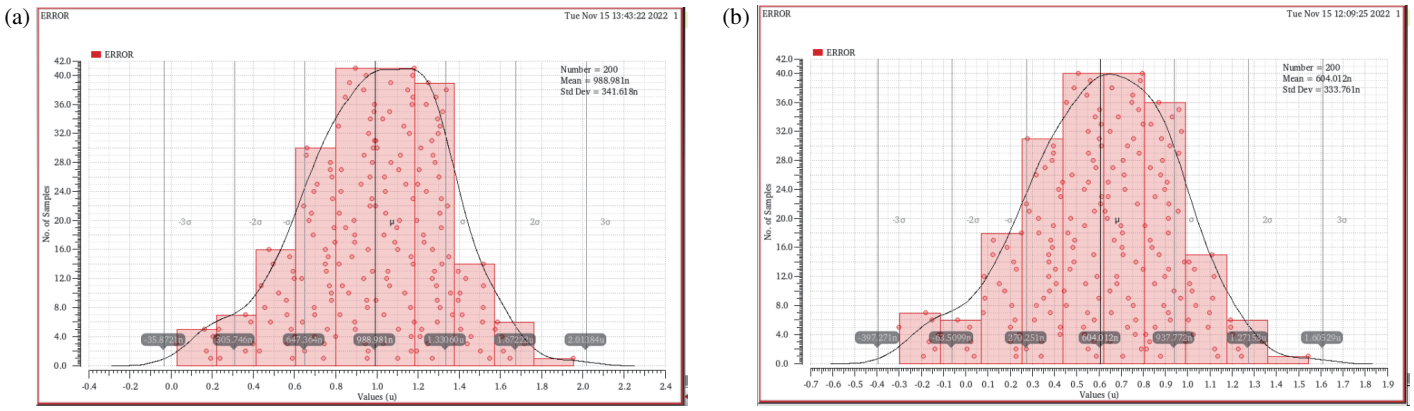

FIGURE 16. (a) Monte Carlo simulation diagram of current detection error without DEM and; (b) Monte Carlo simulation diagram of current detection error with DEM.

TABLE 1. The comparison results of the performance of circuits.

Reference	[20]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[21]	This work
Input voltage/V	2	-	1.2–2	3.3	-	2.5–5	-	2.7–5.5	4	3–5
Frequency	2 MHz	2 MHz	2 MHz	5 MHz	1 MHz	700 kHz–1.4 MHz	100 Hz	4 MHz	2 MHz	200 kHz
Max. output current/mA	225	500	-	500	400	500	100	600	-	830
Detection method	Sense FET	Sense FET	Sense FET	Sense FET	Sense FET	Sense FET	Sense FET+ Auto-adjustment	Sense FET	Sense FET	Sense FET+DEM
Proportional Coefficient (K)	1000	-	-	-	700	1000	1000	-	2000	930/910
Single or both side	both	both	single	both	single	single	single	single	both	both
Accuracy%	98 (max)	Above 90	94	91	95	89.8	99.2	90	97	99.219 (max)
Area (mm^2)	-	1.3 × 1.0	4.87	5	0.54	-	1.31	0.069	2.25	0.027
Technology	0.5 μm	0.35 μm	0.6 μm	0.35 μm	0.35 μm	0.18 μm	0.18 μm	0.5 μm	0.5 μm	90 nm BCD

Fig. 13(b). It can be seen that the current waveform of each power transistor is almost completely coincident with the detection output waveform with high accuracy. It proves that both the sensing currents of the two sides can follow the current of the power transistor well in the conduction stage, which is the the solid line in Fig. 3 mentioned in Subsection 2.1. Fig. 14(a) shows the variation curve of the detection error during a conduction period. It can be seen that the error is relatively smooth, with all below 1 mA.

Select a certain conduction stage of any six power transistors, calculate the detection accuracy according to Eq. (10) and Eq. (11), and analyze the accuracy box diagram as shown in Fig. 14(b). It can be seen that the detection accuracy is above 96%, and the highest can reach 99.219% or more, which totally meets the application requirements of motor drive system. Since the current is always varying, in addition to focusing on instantaneous accuracy, we also need to measure the difference between the continuity sensing current and the actual current by calculating the Root Mean Square Error (RMSE) value according to Eq. (18). If the resulting RMSE value is closer to zero, it proves that the error in the predicted value is smaller. Substituting I_{MP} for $X_{model,i}$ and $K1 * I_{MPS}$ for $X_{obs,i}$ in Eq. (18), the RMSE value of 0.0012 is obtained, which proves that the error of the proposed current detection circuit is stable in continuity, i.e., there are no large deviation points. Fig. 15 shows that the maximum motor phase current that can be detected by the circuit is 830 mA. The motor has a normal operating current of about 500 mA, so the current detection circuit can fully meet the application requirements.

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n} (X_{obs,i} - X_{model,i})^2}{n}} \tag{18}$$

Monte Carlo simulation reflects the mismatch between devices and can better illustrate the process error of the circuit in the actual tape-out. Fig. 16(a) shows the current detection error without DEM, and Fig. 16(b) shows the current detection error with the DEM circuit added. Monte Carlo simulation is performed on 200 samples, where σ represents a statistical term that reflects the size of the sample dispersion, and μ represents the arithmetic mean of all the sample values. The simulation results show that the average detection error of the circuit without DEM mismatch elimination is 988.981 nA, and the average current detection error after adding DEM is reduced to 604.012 nA and the error reduced by 38.9%. The mismatch elimination achieves a good effect.

The proposed current detection circuit's performance is summarized and compared with other current detection circuits in Table 1. It can be seen that the circuit proposed in this paper uses the sense FET technology, which can detect both high side and low side power transistors with high accuracy. At the same time, the circuit also uses DEM mismatch elimination technology to eliminate the current mismatch caused by the large proportional coefficient K and further improves the detection accuracy.

5. CONCLUSIONS

In this paper, a novel current detection circuit based on sense FET technology is proposed, which can simultaneously detect the high-side and low-side power transistor currents of the three-phase inverter bridge of BLDC motors. Meanwhile, a DEM technology is added to the current detection system, which changes the traditional $1 : K$ detection mode into a $1 : 1 : K$ detection mode and eliminates the current mismatch caused by the large size difference between the sensing transistor and power transistor. The circuit can realize on-chip integration and has simple structure and high detection accuracy. Under the conditions of power supply voltage of 3–5 V, the motor winding inductance of 280 μH and temperature of $-40°$C to $125°$C, the proposed method is simulated and verified by 90 nm BCD process, and the following conclusions can be drawn:

1) The circuit can accurately detect the current of six power transistors of three-phase inverter bridge. The maximum motor phase current that can be detected by the circuit is 830 mA.

2) The detection error is less than 1 mA for both high and low sides. The instantaneous detection accuracy is above 96%, and the highest accuracy can reach 99.219%. The RMSE value of the calculated detection error is 0.0012, which indicates that the accuracy is stable in continuity.

3) The DEM circuit can reduce the detection error caused by current mismatch from 988.981 nA to 604.012 nA, and the error is reduced by 38.9%.

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