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Design of True Time Delay Line Based Octal Transmit Receive Module for Wideband Phased Arrays

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ABSTRACT: Wideband phased arrays for Electronic Warfare (EW) applications utilize narrowband phase shifters in a switched configuration to cover a multi-octave bandwidth in split bands. Wideband True Time Delay (TTD) line circuits are the best candidates to replace narrowband phase shifters in such systems, covering the complete operating bandwidth in a single step. The Transmit Receive Module (TRM) is a critical component of any phased array system. A novel design of a TTD line-based Octal Transmit Receive Module (OTRM) for a 32-element EW phased array over a frequency range of 1–6 GHz is presented in this paper. The OTRM is designed on a single multi-layer PCB by integrating eight transmit-receive (TR) channels, associated controllers, and power conditioning circuitry in a compact size and weight of 800 grams. The paper addresses challenges associated in the design of TR channels to fit within the inter-element spacing of 14 mm and to achieve isolation of $\geq$ 40 dB between channels. The designed OTRM tunes time delay up to 508 ps maximum with a step of 2 ps by using a single TTD line circuit for $\pm 45^{\circ}$ scan coverage. The OTRM has demonstrated its potential capability for the use in wideband Radar, EW, and Communication system applications. Efficient thermal management of the OTRM is achieved by introducing Copper coins below the final power amplifiers and a liquid cold plate to dissipate a heat load of 32 watts per TR channel. The proposed OTRM delivers transmit power of 8 watts (CW), receive gain of 25 dB, and a noise figure of 6 dB per TR channel with an overall efficiency of 19% (min) over a 5 GHz bandwidth. RF path analysis of the TR channel in transmit and receive paths is carried out using the Systemvue software tool. To verify the design of the OTRM over different time delay and attenuator states, measurements are conducted using a Vector Network Analyzer (VNA).

1. INTRODUCTION

Active Phased Arrays (APAs) find extensive use in Radar, EW, and Communication systems due to their numerous advantages, including rapid beam agility, high directivity, graceful degradation, dynamic beam shaping, and transmit power control [1–4]. TRM is a key component of any phased array system. It is responsible for amplifying transmit and receive signals, facilitating electronic scanning, and controlling the sidelobes of the antenna beam in real-time [5]. Phased arrays operating across substantial instantaneous bandwidths and wide scan angles encounter issues like beam squint and pulse stretching, necessitating the utilization of wideband TTD lines instead of narrowband phase shifters [6, 7]. A TTD line is a circuit whose time response is independent of frequency, making it a desirable choice for substituting narrowband phase shifters in wideband applications. Unlike phase shifters, long-time delays are required for phased arrays depending on their size, maximum scan angle, and operating bandwidth due to the unwrapping nature of time delay [6]. Various TTD line circuit topologies such as coaxial cables, planar microwave transmission lines, MMIC, Optical/Photonic Integrated Circuits, and digital delay lines are utilized in wideband phased arrays. Nonetheless, TTD lines suffer from drawbacks such as bulky in size, high cost, and restricted time delay capacity, hindering their seamless integration as components within TRMs. The multi-layer RF switched delay lines and Monolithic Microwave Integrated Circuits (MMIC)/Radio Frequency Integrated Circuits (RFIC) are widely integrated into TRMs of phased arrays [8, 9]. Even though optical delay lines offer long-time delay with low frequency independent loss, they require additional RF to optical and optical to RF converters, which increases the cost, power consumption, and weight of TTD lines and makes it difficult to integrate them at the TRM level.

EW systems operating over a wide electromagnetic spectrum of 0.5–40 GHz are generally configured into three split bands: 0.5–6 GHz (low band), 6–18 GHz (mid band), and 18–40 GHz (high band) based on practical realization [10–12]. The design and development of compact EW systems are mainly influenced by the availability of wideband components, including antennas, phase shifters, amplifiers, attenuators, circulators, etc. Especially in the lower band of the EW system, a series of narrowband phase shifters are employed in a switched mode to cover the entire bandwidth in a time-shared fashion, as wideband phase shifters are not available. The TTD line circuits emerge as the optimal candidates for substituting narrowband phase shifters in these systems, encompassing the entire 5 GHz bandwidth in a single sweep. In recent years, the emergence of wideband TTD line Monolithic Microwave Integrated Circuits (MMICs)/Radio Frequency Integrated Circuits (RFICs) with maximum delays of up to 500 ps has facilitated the development of compact, small-scale (up to 64 elements) wideband EW phased arrays.

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Numerous designs have been reported on TTD line-based multi-channel TRMs for wideband phased arrays, typically featuring 4 to 8 TR channels. These designs adopt a hybrid arrangement, combining phase shifters at the TRM level with TTD line circuits at the sub-array level [13–20]. However, these arrays suffer from drawbacks such as bulkiness, high cost, and performance limitations due to array quantization sidelobes. The Octal TRM design for an EW phased array, as presented in [21], utilizes four narrowband phase shifters in a switched configuration per TR channel. The array has to operate in four distinct split bands (1–1.6 GHz, 1.6–2.4 GHz, 2.4–3.2 GHz, and 3.2–6 GHz) to encompass the entire 5 GHz bandwidth.

In this paper, a novel design of OTRM is proposed by integrating a single wideband TTD line RFIC in place of multiple switched phase shifters for 32-element EW phased array to cover 5 GHz bandwidth in a single step. The designed OTRM is capable of tuning time delay up to 508 ps maximum in a step of 2 ps, demonstrating its potential capability to use in wideband Radar, EW, and Communication system applications. The OTRM is designed to demonstrate characteristic parameters of 8-watt CW transmit power, receive gain of 25 dB, and noise figure of 6 dB per TR channel with an overall efficiency of 19% (min) over 1 to 6 GHz.

The paper is structured into five sections: Section 2 describes the design of OTRM and TR channel along with RF path simulation results. The PCB design of OTRM is presented in Section 3. The measured results of the OTRM are provided in Section 4, and inferences are discussed in Section 5.

2. DESIGN OF OCTAL TR MODULE AND TR CHANNEL

2.1. Design of a 32-Element Phased Array

A 32-element (4×8) phased array tailored for Electronic Warfare (EW) applications, depicted in Figure 1, is structured by integrating four Octal Transmit Receive Modules (OTRMs) along with other associated functional blocks. The array is designed to generate an Effective Radiated Power (ERP) of 64 dBm(minimum) excluding radome loss in Electronic Attack (EA)/Jammer mode by using 32 TR modules radiating a total transmit power of 53 dBm(min) with array gain of 11 dB(min) including cable loss. The array in receive mode offers a sensitivity of -60 dBm in Electronic Support (ES) mode. Antenna array is designed using wideband Body of Revolution (BOR) antenna elements with inter-element spacing of 15 mm to provide $\pm 45^\circ$ scan volume in both azimuth and elevation planes [11]. The bi-directional amplifier and array controller module (BAC) integrated within the array provides RF, power, and signal interface to four OTRMs. The array is designed to operate with a single $+28$ V DC power supply and RS-422 interface for timing and control. A 32 (4×8) element EW array at 6 GHz with $m = 4$, $n = 8$, $d_x = d_y = 15$ mm requires a maximum time delay of 500 ps in order to scan $\pm 45^\circ$ in both azimuth (θ) and elevation (ϕ) planes from Equation (1) below [8].

$$\text{Time delay } (\tau_d) = m \times \tau_x + n \times \tau_y \tag{1}$$

where,

$$\tau_x = \frac{d_x \sin(\theta)\cos(\phi)}{c}, \quad \tau_y = \frac{d_y \sin(\theta)\sin(\phi)}{c}. \tag{2}$$

Equation (2) represents the progressive time delays. d_x and d_y are inter-element spacings along X and Y axes; m and n are the number of rows and columns of the array, respectively; and c is the velocity of propagation.

2.2. Octal Transmit Receive Module (OTRM)

The OTRM is configured into 4 functional blocks, viz., wideband Transmit-Receive (TR) channels, Power divider/combiner, Controller, and Power conditioner, as shown in Figure 2. The OTRM is designed to integrate eight 1–6 GHz TR channels, a $1:8$-way RF power divider/combiner (PDC), a Field Programmable Gate Array (FPGA) based controller, and power conditioning circuitry. Each wideband TR channel incorporates MMICs, power amplifiers, gain equalizers, high power and low power switches in both transmit and receive paths. The OTRM controller is interfaced to the system controller, generates the required control signals, and monitors the status of all TR channels. The power conditioner circuitry integrates DC-DC converters, EMI filters, low drop-out (LDO) regulators, etc., and generates the required supply voltages from a $+28$ V DC supply for all TR channels and the FPGA controller. The power conditioning circuitry integrates a bias sequencer to sequence the gate and drain voltages to MMICs used in TR Channel. The $1:8$-way PDC uses four $1:2$-way wideband PDCs, providing a bi-directional RF interface to the eight TR channels. All eight TR channels, along with controller and power conditioning circuitry, are integrated into a single multi-layer PCB in compact size. The design aspects of the TR channel and OTRM controller are discussed in the below subsections.

2.2.1. Transmit Receive (TR) Channel Design

The TR channel is the pivotal functional block within the OTRM tasked with producing the necessary transmit output power and delivering low-noise amplification of received signals from the antenna. The main design challenges are compact packaging of RF circuitry within an inter-element spacing of 15 mm, achieving a continuous wave (CW) output power of 38 dBm over a substantial bandwidth of 5 GHz with proper thermal management. The proposed functional block diagram of the TR channel of OTRM, as shown in Figure 3, has been formulated using commercially available wideband RF components.

A wideband Gallium Nitride (GaN) power amplifier, spanning the frequency range of 1 to 8 GHz, with saturated output power (Psat) of 10 W and a large signal gain of 25 dB has been selected [22]. This specific choice is aimed at offering CW output power of 38 dBm (minimum) operating continuously at 100% duty cycle required for EA mode instead of a short period of pulsed operation. The chosen power amplifier is intrinsically matched to 50-ohm impedances at both the input and output stages. Operating at $+28$ V obviates the need for additional

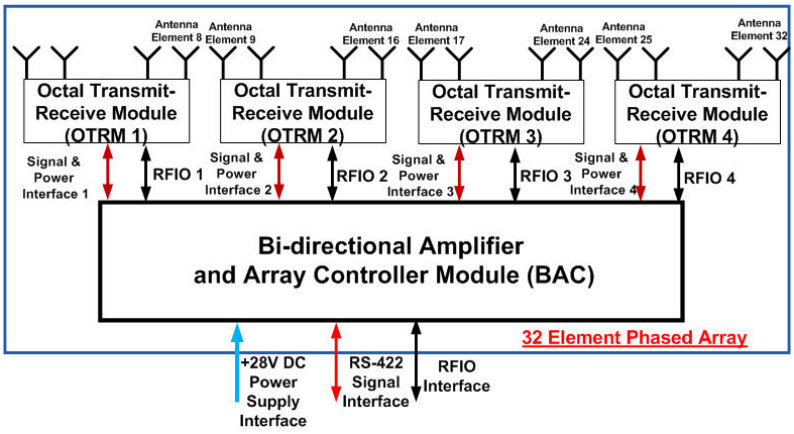

FIGURE 1. Block diagram of a 32-element phased array.

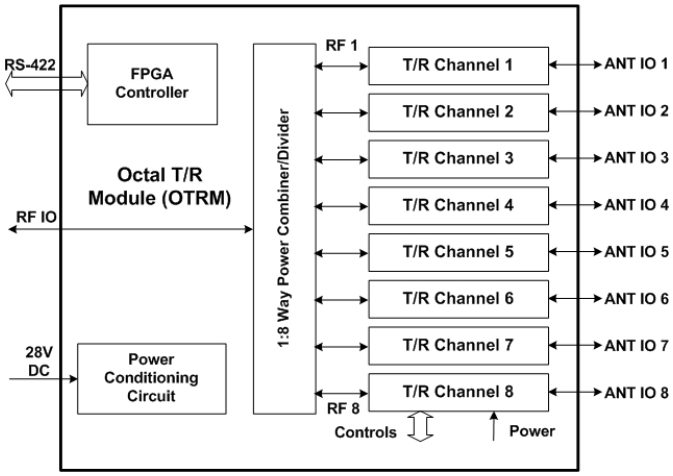

FIGURE 2. Functional block diagram of Octal TR Module (OTRM).

DC-DC converters, resulting in a more compact TR channel design. The duplexer circuit, which connects the antenna to TRM, is realized through the utilization of a GaN-based Single Pole Dual-Throw (SPDT) switch capable of handling high power (40 W) and exhibiting minimal insertion loss ($\leq$ 1 dB) [23]. The receiver protector to protect Rx path of TR channel under poor Voltage Standing Wave Ratio (VSWR) is realized by using a high input power (100 W) handling passive limiter with flat leakage of $+17$ dBm, low insertion loss of 0.7 dB, and fast recovery time of 40 ns [24]. A Gallium Arsenide (GaAs) Low Noise Amplifier (LNA) is characterized by a low noise figure of 2 dB, a high Output Third Order Intercept Point (OIP3) of $+30$ dBm, a gain of 20 dB, and an output 1 dB compression point (P1 dB) of $+18$ dBm has been selected [25] to meet the specified dynamic range and sensitivity requirements.

For electronic beam scanning and controlling sidelobe levels within the array, the proposed design of the Octal Transmit Receive Module (OTRM) features the application of an ADAR4002 bi-directional 7-bit True Time Delay (TTD) line RFIC [26]. Based on Complementary Metal Oxide Semiconductor (CMOS) technology, this programmable TTD line RFIC can offer a maximum delay of 508 ps, adjustable in steps of 2 or 4 ps. This configuration facilitates beam scanning within the desired $\pm 45°$ range for a 32-element array, as described by Equation (1). Additionally, a digital attenuator is included, providing a maximum attenuation of 31.5 dB in increments of 0.5 dB for sidelobe level control [27]. To address the challenges posed by TTD line RFIC's low input 1 dB compression point (P1 dB) of 0 dBm and the substantial insertion loss of -16 dB, supplementary amplifiers are incorporated into both the Transmit (Tx) and Receive (Rx) paths of the TR channel, as illustrated in Figure 3. The design of the TR channel is strategically optimized by incorporating TTD line in a bi-directional configuration, aimed at attaining the desired RF performance of the OTRM. The overall design philosophy of the TR channel revolves around minimizing component count while achieving the sought-after RF performance. This is achieved by capitalizing on the strengths of TTD line technology and meticulous selection of components to ensure optimal system functionality.

2.2.2. OTRM Controller

The controller for OTRM is developed using a low-power Actel (Microsemi) Field Programmable Gate Array (FPGA), which is responsible for real-time control of the eight TR channels by generating precise timing and control signals. The controller is linked to the system controller via an RS-422 serial interface operating at 10 Mbps. It generates the necessary control signals, monitors the temperature and critical supply voltages, and oversees the operational status of all TR channels. To accommodate calibration error data storage, a flash memory with a capacity of 64 kilo byte is integrated. Moreover, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switches are incorporated into the blanking circuits of both Tx and Rx paths to reduce power consumption and furnish essential isolation during the calibration of TRMs [27]. For the purpose of real-time adjustments to the attenuator and time delay states of the TTD line RFIC, a five-wire high-speed Serial Peripheral Interface (SPI) is established within the FPGA. This interface operates at a clock speed of 40 MHz and offers a switching time capped at 50 ns (maximum). The control voltage of $0/-28$ V required for high power SPDT switch operation is generated using appropriate fast switching transistor circuitry to achieve ≤ 100 ns switching time.

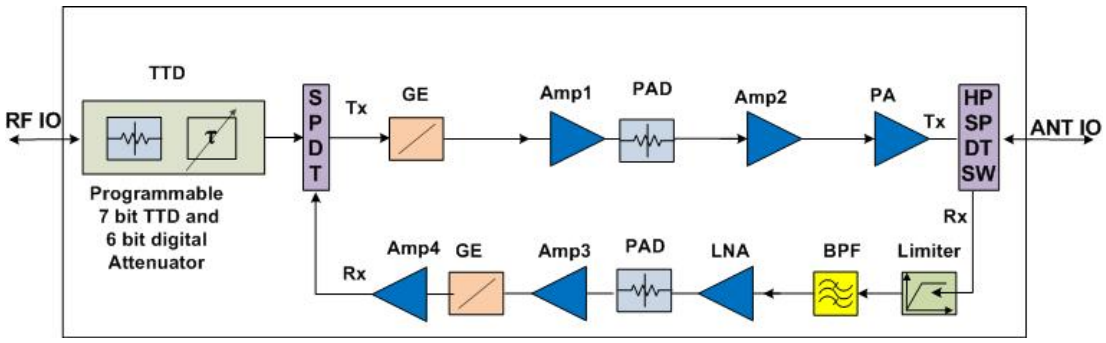

FIGURE 3. Functional block diagram of TR channel.

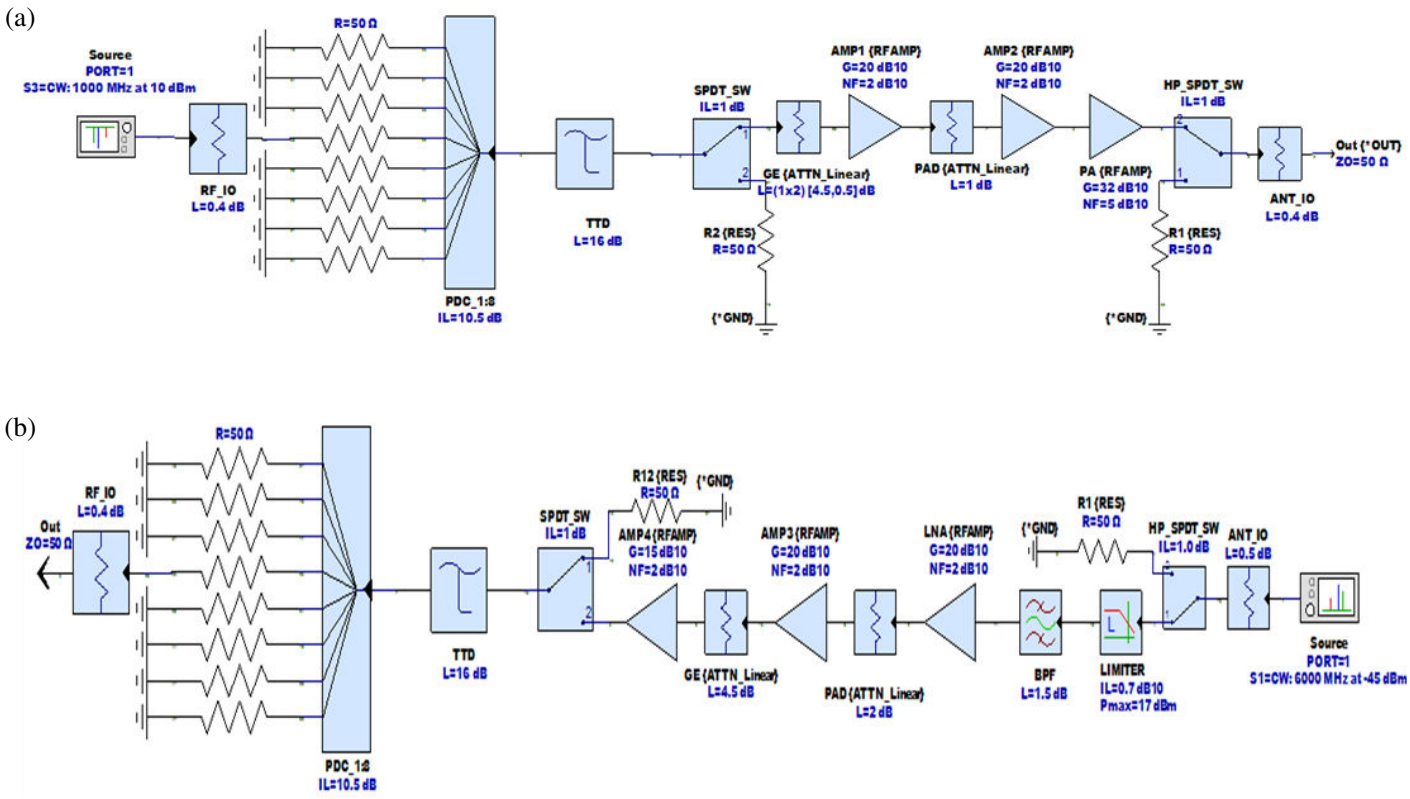

FIGURE 4. TR channel simulation schematics of OTRM: (a) Transmit path and (b) Receive path.

2.3. RF Path Simulation of OTRM

To ensure the robust functionality of the OTRM, an in-depth analysis of the RF path is carried out by using the selected components to achieve a transmit output power of 38 dBm and a maximum receive noise figure of 6 dB per TR channel over the entire bandwidth. The OTRM design is simulated in the transmit and receive paths using the Pathwave system design (SystemVue) software tool [28] with S-parameter models and signal source fed at RFIO and antenna IO ports for one of the TR channel as shown in Figure 4(a) and (b), respectively.

The simulated gain and noise figure at different circuit nodes of receive path are shown in Figures 5(a) and (b) with a 6 GHz input signal fed at antenna IO port. The transmit path of OTRM is simulated at input frequency of 1 GHz and 6 GHz fed at RFIO port, and the output power spectrum depicted in Figures 6(a) and (b) shows that output power is above 38 dBm, and harmonic levels are ≤ -15 dBc. The simulation results reveal that the proposed design configuration meets the intended performance of the OTRM.

3. OTRM PCB AND THERMAL DESIGN

This section covers the design aspects of the Printed Circuit Board (PCB) and the thermal management aspects of OTRM.

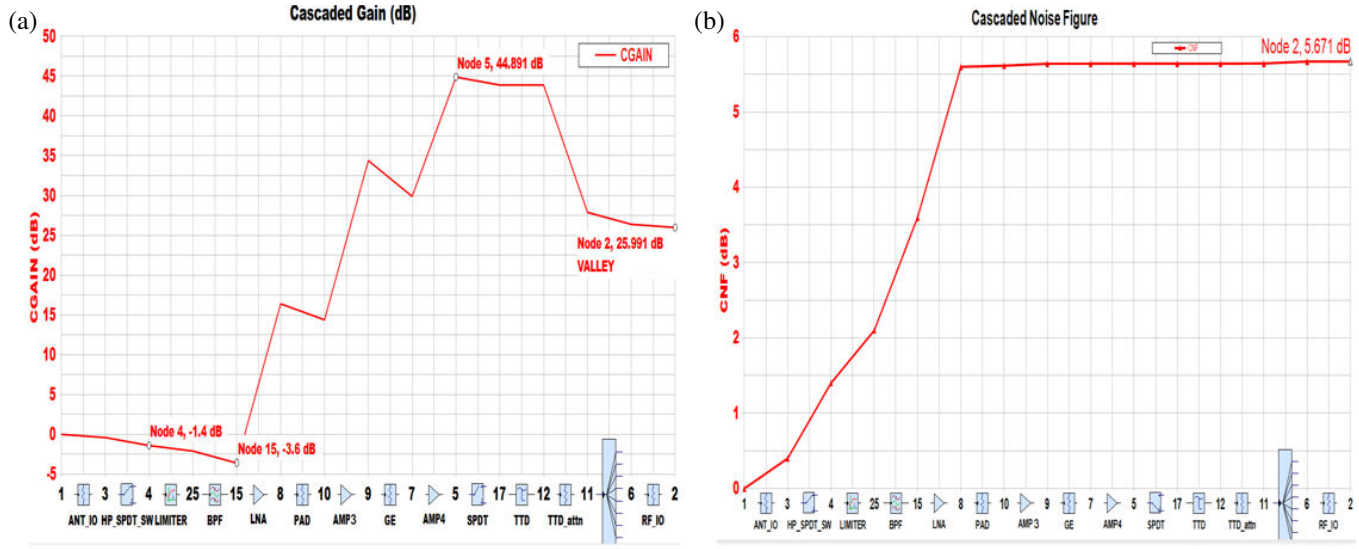

FIGURE 5. OTRM receive path: (a) Cascaded gain and (b) Cascaded noise figure.

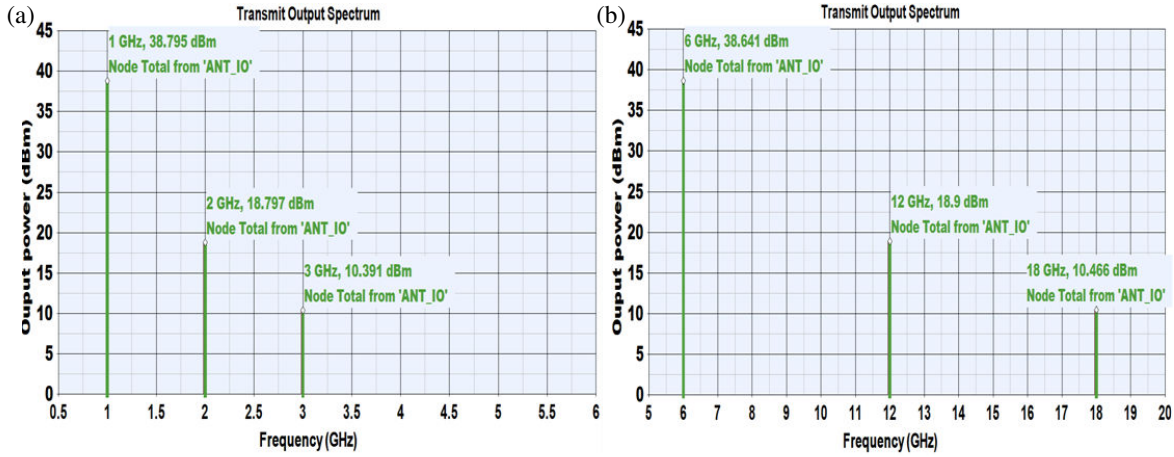

FIGURE 6. OTRM transmit path output spectrum with input: (a) at 1 GHz and (b) at 6 GHz.

3.1. OTRM PCB Design

The OTRM is designed on a single eight-layer PCB. The RF circuitry of TR channel and $1:8$-way PDC is designed using a low loss (loss tangent $(\tan\delta) = 0.0027@10\,\text{GHz}$) RO4003C microwave substrate with 8 mil thickness, $\epsilon_r = 3.48$ dielectric constant, and 0.5-ounce copper [29]. The digital controller and power conditioning circuits are designed using an FR4 laminate of 10 mil thickness, $\epsilon_r = 4.0$. The PCB layer stack-up is depicted in Figure 7 with FR4 pre-preg, appropriate buried vias, and printed through holes for multi-layer interconnection. The $1:8$-way PDC with four $1:2$-way PDC components is integrated on the bottom layer of the PCB, shown in Figure 8(a). All active components are integrated on the top layer of the PCB for easy debugging and reworking, as illustrated in Figure 8(b).

The RF circuit layout is designed and simulated using the Pathwave Advanced Design System (ADS) software tool [30]. The complete PCB layout, along with signal and power integrity analysis for controller and power conditioning circuitry, is carried out using the Cadence Allegro PCB design software tool [31]. The PCB layout for eight TR channels is identical and optimized to fit within a 14 mm width. Narrow partition walls of 0.5 mm thickness are integrated between adjacent TR channels to achieve better than 40 dB of channel-to-channel isolation, and electromagnetic simulation is carried out to verify the isolation performance. The PCB of OTRM is integrated with eight blind mate connectors (BMAs) for Antenna IO, a sub-miniature push-on (SMP) connector for RFIO, and 37-pin Micro-D connector for signal and power interfaces. The assembled view of the developed OTRM PCB is shown in Figure 9.

3.2. OTRM Mechanical and Thermal Design

The OTRM PCB is designed to fit within a mechanical enclosure measuring 185 mm in width, 155 mm in depth, and 15 mm in height. To ensure proper thermal management, the OTRM housing is mounted on a liquid-cooled plate within the array unit, secured with wedge locks, as illustrated in Figure 10(a). The OTRM dissipates 260 W of heat (32 W per TR channel and

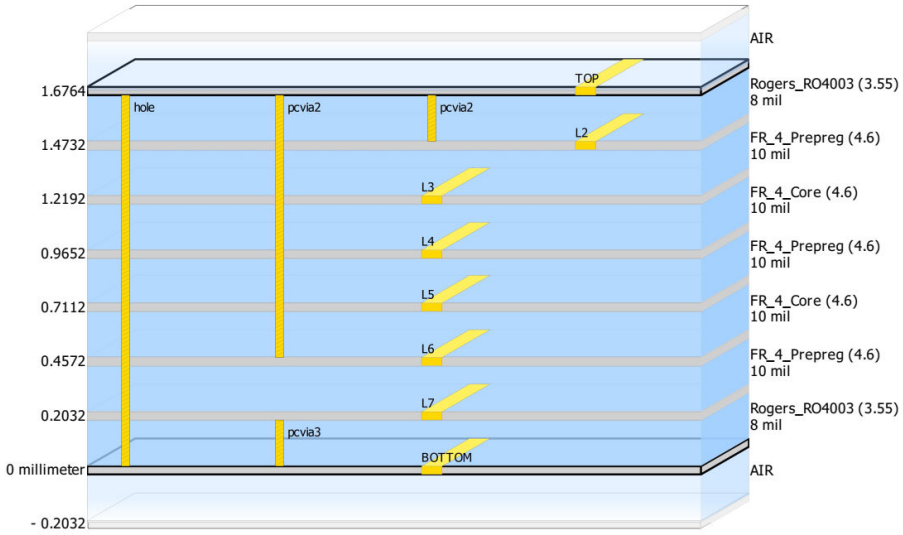

FIGURE 7. OTRM PCB layer stack-up.

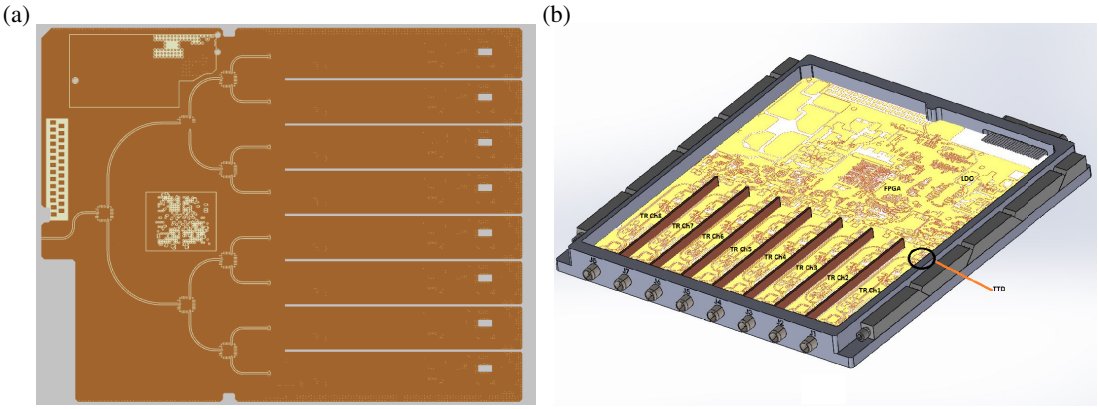

FIGURE 8. Designed OTRM PCB: (a) Bottom view and (b) Top view.

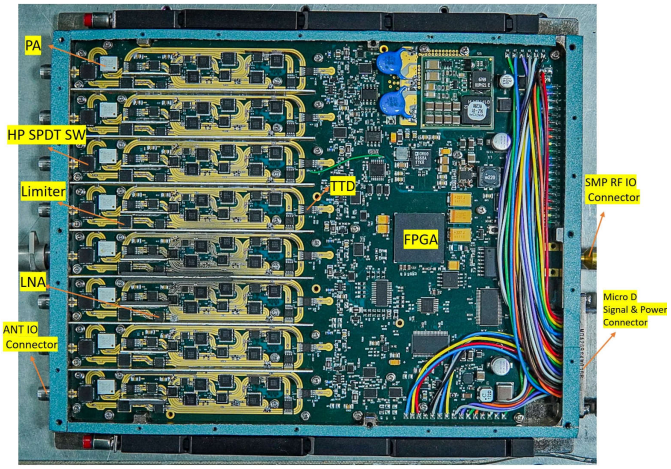

FIGURE 9. Assembled view of developed OTRM.

4 W from other circuits) during CW operation of transmit path, with an overall efficiency of at least 19%. The thermal design of the OTRM incorporates copper coins positioned beneath the final power amplifier components. Additionally, the bottom side of the OTRM is affixed to a liquid cold plate to dissipate the total heat load of 260 watts efficiently.

Thermal analysis is performed using a liquid cold plate with a thickness of 10 mm, supplied with a liquid inlet temperature of 45°C and a maximum ambient temperature of 71°C. The thermal resistance of the mechanical enclosure, PCB, and components are considered in a cascaded thermal model during the analysis. The thermal contour plot of the OTRM, depicted in Figure 10(b), indicates that the highest temperature on the PCB at the power amplifiers reaches 126°C. This value falls within the allowable junction temperature range of the components, demonstrating the effectiveness of the OTRM's thermal design in maintaining component temperatures within acceptable limits during operation.

4. PERFORMANCE MEASUREMENT OF OTRM

The performance of OTRM is measured both in transmit and receive paths of TR channels (Channel 1 to Channel 8) using a Vector Network Analyzer, Spectrum Analyzer, and Signal Generators [32] as illustrated in Figure 11.

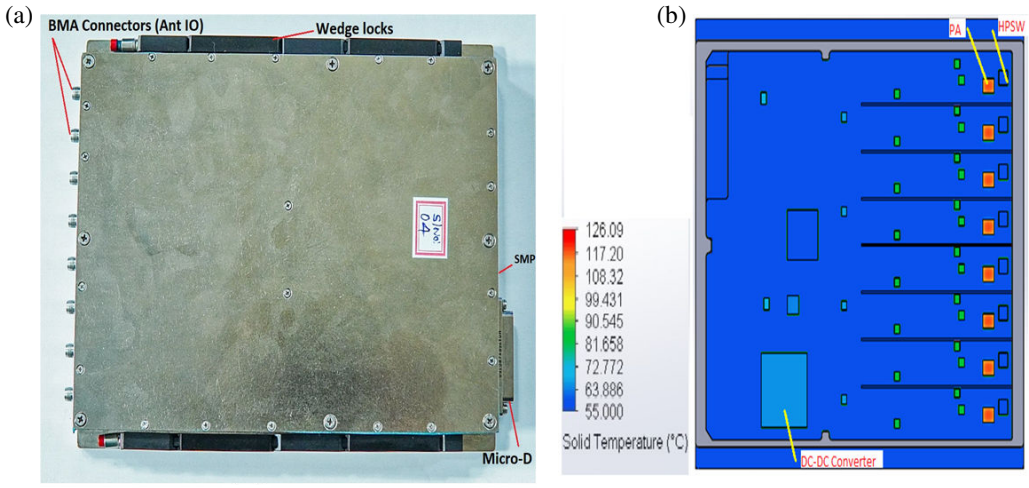

FIGURE 10. OTRM: (a) Mechanical integrated view and (b) Temperature contour of PCB at 71°C ambient temperature.

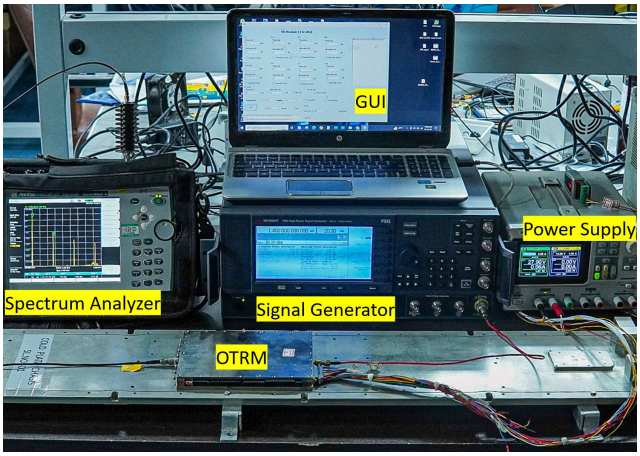

FIGURE 11. OTRM measurement setup.

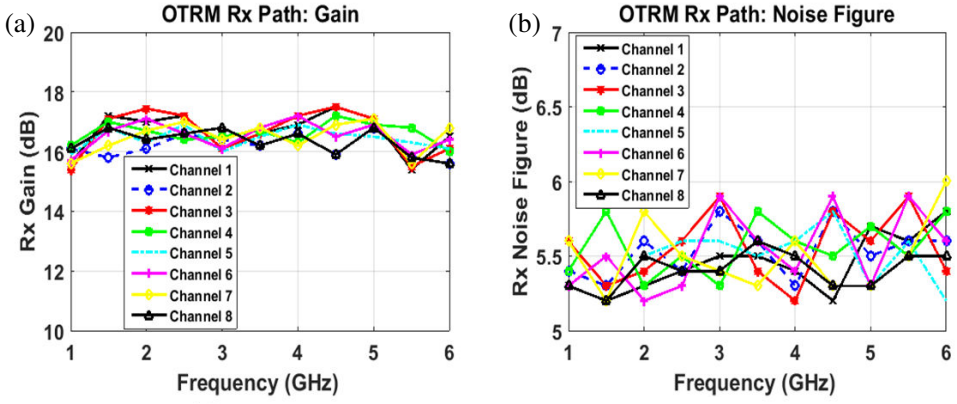

FIGURE 12. Test results of OTRM: (a) Receiver gain (dB) and (b) Receiver noise figure (dB).

The performance evaluation of the OTRM is carried out at a liquid inlet temperature of 45°C. Furthermore, the characterisation is performed across the operating temperature range of −40°C to +71°C. The measured receiver gain, receiver noise figure, transmit output power, and channel-to-channel isolation results for the 8 TR channels of the OTRM are displayed in Figures 12(a) and (b), 13(a) and (b), respectively. The time delay in the OTRM is computed using Equation (3) and is based on

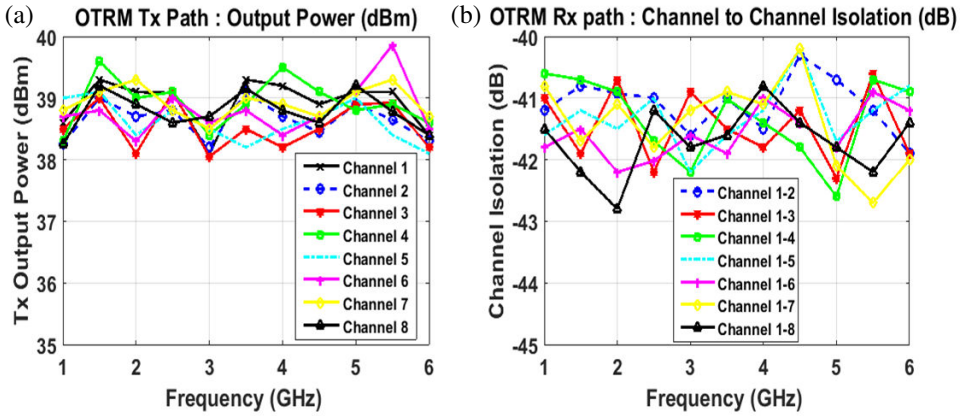

FIGURE 13. Test results of OTRM: (a) Transmit output power (dBm) and (b) Rx channel isolation (dB).

TABLE 1. Performance of developed OTRM.

Parameter	Achieved performance
Frequency	1–6 GHz
Number of TR Channels	8
Transmit input power at RFIO	10 ± 1 dBm
Transmit output power at Antenna IO	8 Watt CW (min)
Transmit in band and out of band noise level	≤ -45 dBm/MHz and ≤ -60 dBm/MHz
Transmit harmonic level	≤ -40 dBc
Receiver gain per TR channel	25 dB (min) and 15 dB (min) with power combiner loss
Receiver Noise figure	6 dB (max)
Receiver out of band rejection	≥ 40 dBc (@$\leq$ 850 MHz and @$\geq$ 6.6 GHz)
Receiver Channel to Channel isolation	≥ 40 dB
Receiver input damage level	10 Watt CW
Tx to Rx, Rx to Tx switching time, attenuator, time delay states settling time	100 ns (max)
Time delay control range	7-bit, 508 ps (max), 2/4 ps resolution
Attenuator control range	6-bit, 31.5 dB (max), 0.5 dB resolution
OTRM Power supply and consumption	28 ± 1 V DC and 325 W
Efficiency and thermal load	19% (min) and 260 W (max)
Operating temperature	-40°C to $+71^{\circ}$C
Dimension and weight	$185 \times 155 \times 15$ mm and 800 grams (max)

the unwrapped phase data obtained from measurements using a Vector Network Analyzer. The unwrapped phase data allows for a continuous and accurate phase representation without the typical modulo 2π wrap-around.

$$\text{Time delay (ns)} = \frac{\text{Unwrapped phase (Deg)}}{360^{\circ} \times \text{Frequency (GHz)}} \tag{3}$$

To ensure the accuracy and reliability of the computed time delay, it is then verified through group delay measurement using a VNA, which helped in validating the time delay performance of the OTRM more precisely. The receive path time delay and gain performance for TR channel-1 is measured using a VNA across all primary states of the time delay and attenuator blocks of the TTD line RFIC. Figure 14(a) shows the variations in time delay observed for different settings of the time delay block, and Figure 14(b) presents the corresponding variations in receiver gain for different attenuator states.

The results obtained from these measurements are instrumental in validating the overall functionality and adherence to performance requirements of the OTRM, thereby ensuring its suitability for the intended application in the electronic warfare array or any other relevant system. The overall performance of the developed OTRM is given in Table 1.

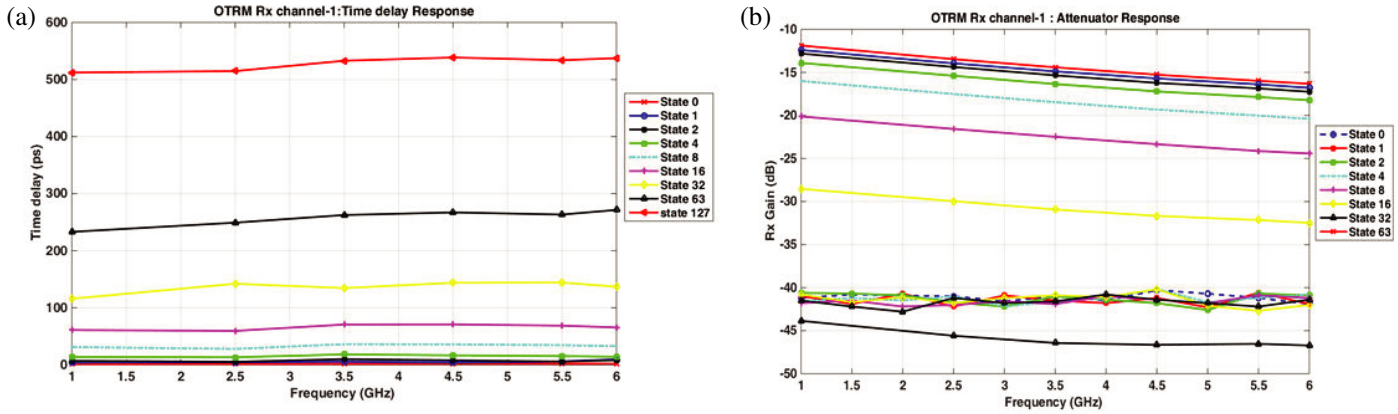

FIGURE 14. TR channel-1 receive path response: (a) Over time delay line primary states and (b) Gain over primary states of attenuator.

5. CONCLUSION

The paper provides the design of a wideband eight-channel TR module, OTRM by utilizing commercially available bi-directional TTD line RFIC and other MMICs for the development of a 32-element wideband Electronic Warfare (EW) phased array, operating across the frequency range of 1–6 GHz. The designed OTRM has demonstrated a minimum transmit output power of 8 Watt, maximum receiver noise figure of 6 dB, gain of 25 dB (excluding power combiner loss), and switching speed better than 100 ns (including SPDT switching time, TTD settling time, power amplifier bias settling, etc.) across 5 GHz bandwidth and over a temperature range of $-40°$C to $+71°$C. The OTRM is ingeniously designed with overall efficiency better than 19%, in a compact form factor measuring $185 \times 155 \times 15$ mm and weighing a maximum of 800 grams.

Indeed, the integration of the current design of the OTRM with a 0.5–19 GHz wideband TTD line RFIC showcases its potential capability to address a wide range of advanced communication and defense applications. Such applications include wideband shared aperture systems, phased arrays for high-resolution imaging radars, high data rate communication links, and EW systems over a broader frequency range of 0.5–18 GHz.

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