# A Scalable PSP RF Model for 0.11 μm MOSFETs

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**Abstract**—An accurate, efficient and scalable SPICE model is essential for modern integrated circuits design, especially for radio frequency (RF) circuit design. A PSP based scalable RF model is extracted and verified in 0.11 μm CMOS manufacturing process. The $S$ parameter measurement system and open-short de-embedding technique is applied. The macro-model equivalent subcircuit and parameters extraction strategy are discussed. The extracted model can match the de-embedded $S$ parameters data well. By combining the model parameters' dependencies on each geometry quantity, the scalable expression of parameters with all geometry quantities included can be obtained. This work can be a reference for the RF MOSFETs modeling and RF circuit design.

## 1. INTRODUCTION

With the radio frequency (RF) wireless communication market growing rapidly, the demand for RF circuits and devices is rising. For RF consumer products, time to market and design circle highly relies on the design environment and circuit simulation capability. For modern circuit design, especially for analog and high frequency circuit design, an accurate, computational efficient and reliable Simulation Program with Integrated Circuit Emphasis (SPICE) [1, 2] model is essential for circuit design efficiency and the reduction of time to market. The data dimensionality reduction is essential for the simulation procedure [3].

Compared with the SPICE model for digital and low frequency analog circuit, the SPICE model for RF circuits is much more complicated and challenging. For the consideration of scalability and flexibility, a practical solution of RF Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is the subcircuit macro-modeling constructed by a compact core model and other parasitic components. These parasitic components can be ignored in direct-current (DC) and low frequency circuits, but they are quite important for RF behaviors prediction. The difficulties of RF modeling come from some aspects: the RF measurement and de-embedding [4–6] of raw data; higher requirements for compact core model; and the extraction and scalability of parasitic components. The measurement of RF MOSFETs requires not only the MOSFET devices under test (DUT) itself but also related de-embedding test structures. De-embedding procedure is also essential before data can be used in following model extraction steps. The open-short de-embedding technique [4] is adopted in this work. The compact model for DC and low frequency circuits mostly focus on the direct measured data, while RF modeling raises higher demands for the model continuity, high order derivatives match and geometry scalability. The surface potential based physical model PSP [7, 8] in this work has a superior performance on these aspects. The scalability of RF model is also essential for circuit simulation efficiency. One practical scalable method proposed in this work is divided into 2 main steps: to find the parameters' dependency on each single geometry parameter and combine these dependencies into an overall scalable expression. The PSP RF model is extracted and verified in 0.11 μm CMOS manufacturing process.

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This article is organized as follows. In Section 2, the RF $S$ parameters measurement system, measurement conditions, and the geometry layout of MOSFET devices are introduced. In Section 3, the de-embedding details and results are illustrated in Subsection 3.1; the macro-model equivalent subcircuit and extraction strategy are given in Subsection 3.2; the scalability details are discussed and illustrated in Subsection 3.3. Section 4 is the conclusion.

## 2. EXPERIMENT DETAILS

The RF modeling of MOSFETs is based on an accurate DC model of devices. Thus, DC and RF measurements are both essential for the RF modeling. On wafer measurement on the Cascade SUMMIT wafer probe station is performed for the DC modeling.

The RF $S$ parameter measurement is carried out on the Cascade SUMMIT wafer probe station.
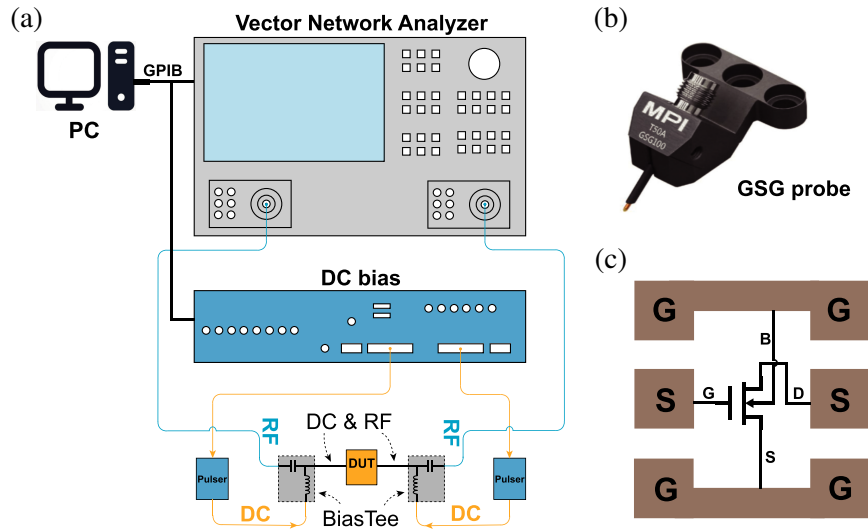


**Figure 1.** The (a) RF $S$ parameters measurement system, (b) photo of GSG probe and (c) GSG connection with common-source MOSFET.
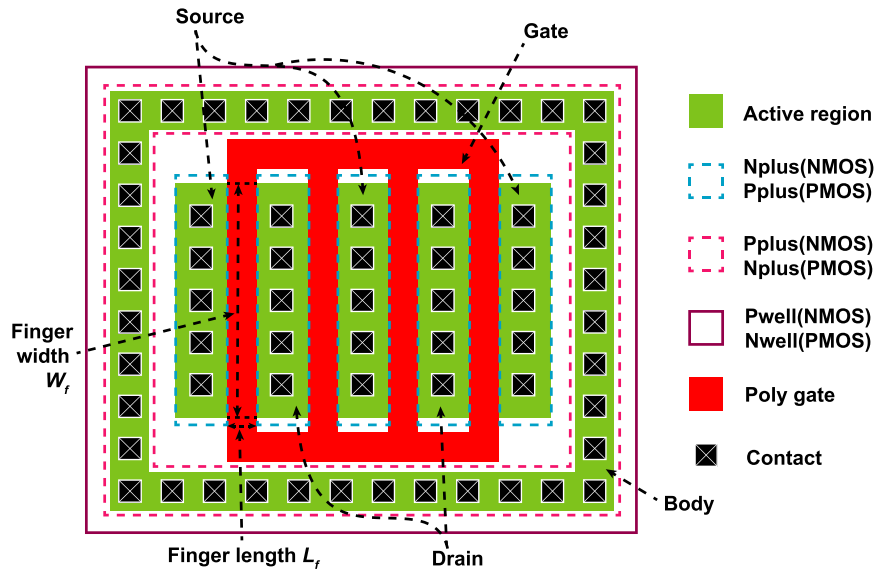


**Figure 2.** The layout of a NMOS/PMOS with the number of fingers $n_f = 4$.

The Agilent N5244A PNA-X vector network analyzer is employed for the $S$ parameters' measurement. The DC bias and RF signal provided by these 2 testing instruments are synthesized by an external BiasTee. Testing instruments are linked to a computer by the general-purpose interface bus (GPIB) and controlled by the Keysight IC-CAP software of computer. The overall $S$ parameters testing system is illustrated in Fig. 1(a). The Ground-Signal-Ground (GSG) RF probes shown in Figs. 1(b) and (c) are used for the probing testing of devices. All devices are measured on the common-source mode. The gate of MOS is port 1, and the drain is port 2. The source and body node of MOS are grounded during $S$ parameter measurement. The frequency range sweeps from 50 MHz to 20.05 GHz.

The DUTs are multi-finger layout n-channel Metal-Oxide-Semiconductor (NMOS) and p-channel Metal-Oxide-Semiconductor (PMOS) devices of 0.11 μm low power process with operating voltage $V_{DD} = 1.5$ V. Fig. 2 is the layout of a 4 fingers NMOS/PMOS device. The key geometry size parameters that determine the electrical performance of MOSFET are channel length $L$, channel width of each finger $W_f$, and the number of fingers $n_f$. The total channel width of device is $W = W_f \times n_f$. The geometry size parameters of DUTs in this work are listed in Table 1.

**Table 1.** The geometry size parameters of MOSFETs.

| $n_f$ | $W_f$ (μm) | $L_f$ (μm) | $n_f$ | $W_f$ (μm) | $L_f$ (μm) | $n_f$ | $W_f$ (μm) | $L_f$ (μm) |
|---|---|---|---|---|---|---|---|---|
| 2 | 2 | 0.12 | 4 | 4 | 0.12 | 8 | 2 | 0.75 |
| 4 | 1.5 | 0.12 | 8 | 4 | 0.12 | 3 | 2 | 0.12 |
| 4 | 2 | 0.12 | 16 | 4 | 0.12 | 5 | 2 | 0.12 |
| 8 | 2 | 0.12 | 4 | 8 | 0.12 | 7 | 2 | 0.12 |
| 16 | 2 | 0.12 | 8 | 8 | 0.12 | 9 | 2 | 0.12 |
| 32 | 2 | 0.12 | 8 | 2 | 0.18 | 17 | 2 | 0.12 |
| 64 | 2 | 0.12 | 8 | 2 | 0.3 | | | |
| 2 | 4 | 0.12 | 8 | 2 | 0.5 | | | |

## 3. RF MODELING

The RF modeling of MOSFET devices is essential for the predictions of high-frequency behavior. This is extremely important for the accurate simulation results of designed RF circuits. Roughly speaking, the RF modeling procedure of MOSFET can be divided into 2 main steps, device measurement and parameter extraction. The measurement system and device list are mentioned in Section 2. There is a necessary step before the measured data can be applied in the model extraction, that is data de-embedding. The de-embedding technique, parameter extraction methods, and the scalability of parameters are discussed.

### 3.1. De-Embedding

To get the real electrical characteristics of devices from the $S$ parameter measurement data, de-embedding is essential for the elimination of parasitic effects induced by the pad and interconnect metal wires between DUTs and probe tips. Different de-embedding techniques have been proposed with different calibration test structures [4–6]. The open-short de-embedding technique [4] used in this work is an effective and practical de-embedding method widely used for MOSFET RF modeling. Fig. 3 illustrates the equivalent circuits in open-short de-embedding technique. Fig. 3(a) is the equivalent circuit with DUT test structures, and the test results include the effects of parallel parasitics, series parasitics, and DUT. Fig. 3(b) is the equivalent circuit of open test structures, and the test result includes the effect of parallel parasitics. Fig. 3(c) is the equivalent circuit of short test structures, and the test result includes the effects of parallel parasitics and series parasitics. The $Y$ parameters matrix
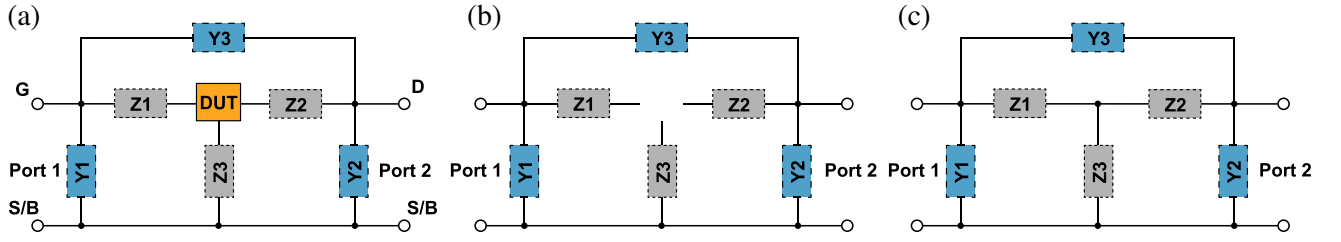
**Figure 3.** The equivalent circuits in open-short de-embedding technique. (a) Equivalent circuit with DUT test structure. (b) Equivalent circuit of open test structure. (c) Equivalent circuit of short test structure.

of DUT $Y_{DUT}$ is given by [4]

$$\frac{1}{Y_{DUT}} = \frac{1}{Y_{total} - Y_{open}} - \frac{1}{Y_{short} - Y_{open}} \tag{1}$$

where $Y_{total}$ is the test result with DUT, $Y_{open}$ the test result of open test structure, and $Y_{short}$ the test result of short test structure.

Figure 4 shows the real and imaginary parts of $Y$ parameters before and after de-embedding for NMOS device with $n_f = 16$, $W_f = $ μm, and $L_f = 0.12$ μm at DC bias of $V_d = V_g = 0.5$ V and
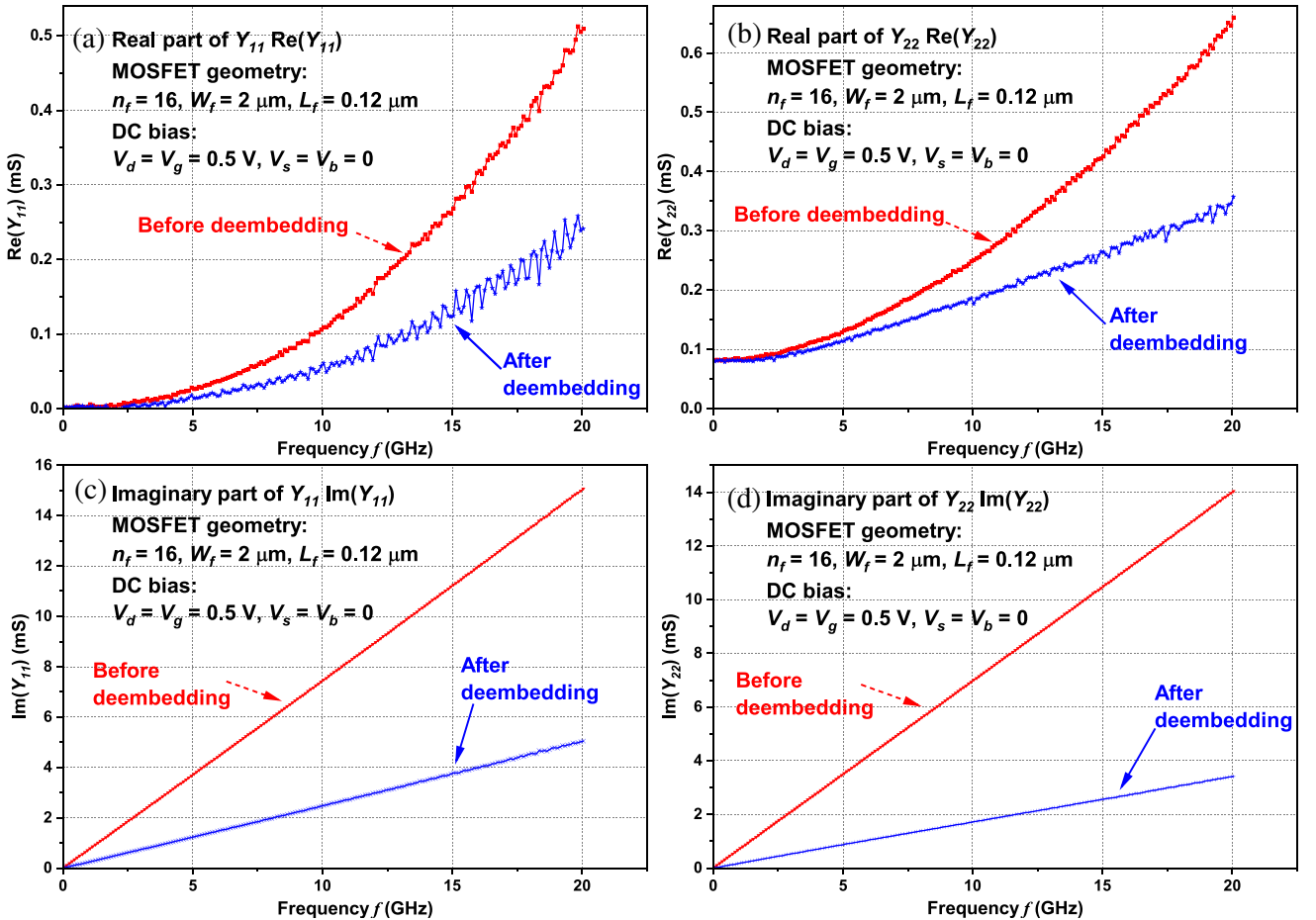


**Figure 4.** The $Y$ parameters of NMOS device before and after de-embedding.

$V_s = V_b = 0$. It tells that parasitic effects have significant impact on the RF measurement results. All MOSFET devices' measurement data in this work are de-embedded before it is applied in the modeling procedure.

## 3.2. Model Subcircuit and Parameters Extraction

For the high frequency (HF) modeling of MOSFET, the parasitic components of devices are really needed to be considered. Some key parasitic components are the parasitic series resistance at source, drain, gate and body 4 terminals, the parasitic series inductance at source, drain and gate 3 terminals, the parasitic capacitance between different terminals, and the parasitic capacitance of body terminal. With the universality of compact models considered, these parasitic components are not included in the MOSFET compact models, like Berkeley Short-channel IGFET Model (BSIM) [9], EKV [10] and PSP [7, 8] model which is used as the core model in this work. Subcircuit based model is adopted in RF modeling for its flexibility. The model subcircuit of this work is shown as in Fig. 5. The parasitic series resistances are $R_s$, $R_d$, and $R_g$; the parasitic series inductances are $L_s$, $L_d$, and $L_g$; the parasitic capacitances between different terminals are $C_{gs}$, $C_{gd}$, $C_{ds}$ and parasitic junction capacitances $C_{jsb}$, $C_{jdb}$; the parasitic substrate distributed resistance and capacitance are $R_b$ and $C_b$. The intrinsic model is PSP model.
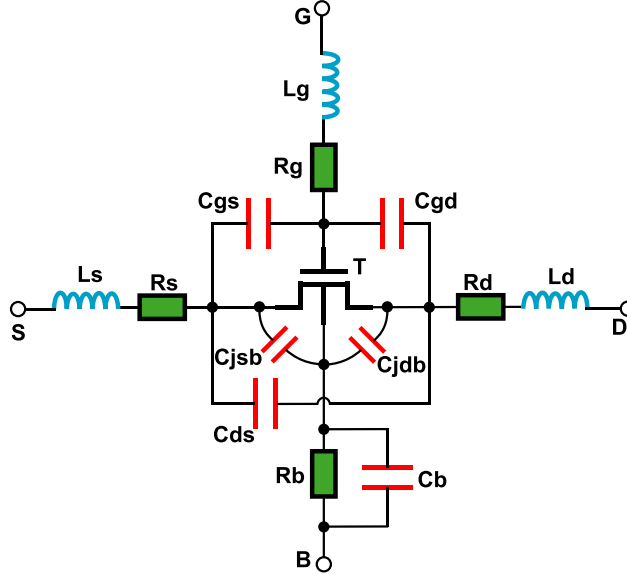


**Figure 5.** The RF model subcircuit.

The zero bias extraction method [11] is used in the extraction procedure. When the DC point of MOSFET is set as zero, $V_{DS} = V_{GS} = 0$, the transconductance $g_m$ and output conductance $g_{ds}$ are 0. Thus, the channel is off under zero bias, and the equivalent circuit can be greatly simplified. Compared with $C_{gs}$, $C_{gd}$, and $C_{ds}$, the parasitic junction capacitances $C_{jsb}$ and $C_{jdb}$ are much smaller. With $C_{jsb}$ and $C_{jdb}$ neglected under zero bias, the impedance parameters $Z$ can be approximately calculated as

$$Z_{11} \approx R_s + R_g + j\left[\omega\left(L_s + L_g\right) - \frac{1}{\omega C_1}\right] \quad Z_{12} \approx R_s + j\left(\omega L_s - \frac{1}{\omega C_2}\right)$$

$$Z_{21} \approx R_s + j\left(\omega L_s - \frac{1}{\omega C_3}\right) \quad\quad\quad Z_{22} \approx R_s + R_d + j\left[\omega\left(L_s + L_d\right) - \frac{1}{\omega C_4}\right]$$

(2)

where $\omega = 2\pi f$ is the angular frequency, and notations $C_1$–$C_4$ are given by

$$C_1 = C_{gs} + \frac{C_{gd}C_{ds}}{C_{gd} + C_{ds}} \qquad C_2 = C_{gs} + C_{ds} + \frac{C_{ds}C_{gs}}{C_{gd}}$$

$$C_3 = C_{ds} + C_{gs} + \frac{C_{gs}C_{ds}}{C_{gd}} \quad C_4 = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}} \tag{3}$$

With this zero bias method, gate resistance $R_g$, 3 terminal inductances $L_g$, $L_s$, $L_d$, the capacitance between terminals $C_{gs}$, $C_{gd}$, $C_{ds}$ can all be roughly estimated. The parasitic source series resistance $R_s$ and drain series resistance $R_d$ originate from the via 1 (V1) and metal 1 (M1) contact resistance at source and drain side. Thus, parameters $R_s$ and $R_d$ are estimated by the V1 number, geometry of M1 of device layout. The sheet resistance of M1 is also involved in the calculation of $R_s$ and $R_d$. The parasitic junction capacitances $C_{jsb}$ and $C_{jdb}$ are small capacitances which are estimated as the level of $0.01\,\text{fF}$. The parasitic substrate distributed resistance $R_b$ is about several hundreds of $\Omega$, and distributed capacitance $C_b$ is of aF level.

With zero bias method and the estimation of other parameters, the approximation of all parameters can be obtained. With the help of IC-CAP modeling software, parameters are tuned to fit measured data after de-embedding.

With all DC and RF parameters extracted, the model can fit the measurement data well. Fig. 6 are the DC modeling results of NMOS devices with $W_f = 2\,\mu\text{m}$, $L_f = 0.12\,\mu\text{m}$, $n_f = 16$. The points are measurement data and curves are model predictions. Fig. 6(a) shows the transfer characteristic curves. Fig. 6(b) shows the output characteristic curves.
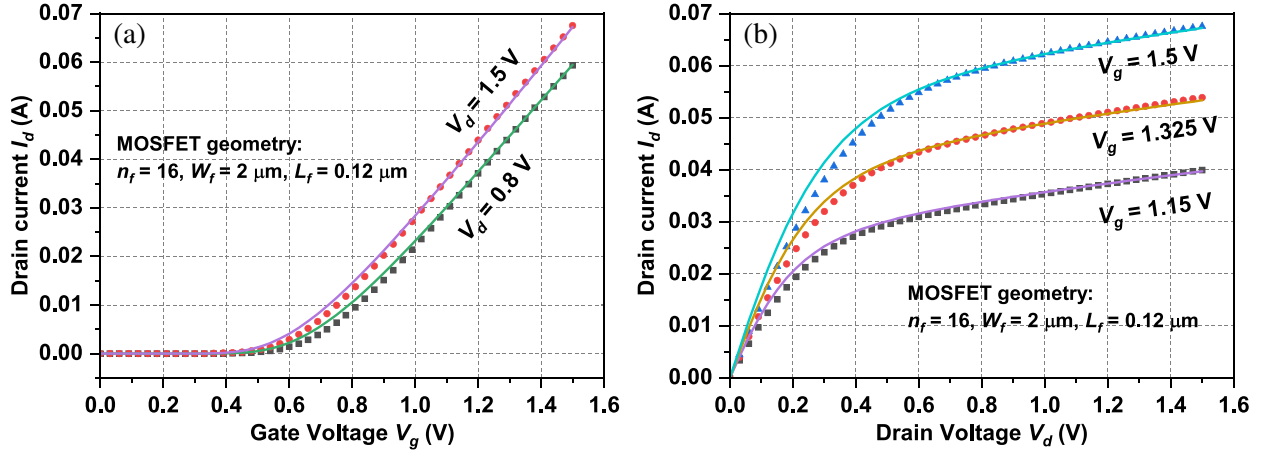


**Figure 6.** The DC curves fitting results of NMOS devices with $W_f = 2\,\mu\text{m}$, $L_f = 0.12\,\mu\text{m}$, $n_f = 16$.

The high frequency $S$ parameter fitting results are illustrated in the Smith chart in Fig. 7. The reflection coefficients of input port 1 $S_{11}$ and output port 2 $S_{22}$ are shown in Fig. 7(a). The reference impedance is $Z_0 = 50\,\Omega$. The reverse isolation coefficient $S_{12}$ and forward transmission coefficient $S_{21}$ are depicted in Figs. 7(b) and (c). The DC bias $(V_d, V_g)$ in volt of Fig. 7 is taken as (0.5, 1) for dc0, (1, 1) for dc1, (1, 1.5) for dc2, and (1.5, 1.5) for dc3.

### 3.3. Parameters' Scalability

With the parameters of each single geometry size extracted, it is necessary to develop a scalable model which can be applied to the device of a geometry range instead a single point size. This is meaningful for the universality and computational efficiency of model.

The geometry size of MOSFET devices in this work is determined by the number of fingers $n_f$, finger width $W_f$, and finger length $L_f$. The exploration of the scalable expression of all 3 geometry quantities is tough. One feasible solution in this work is divided into 2 steps:
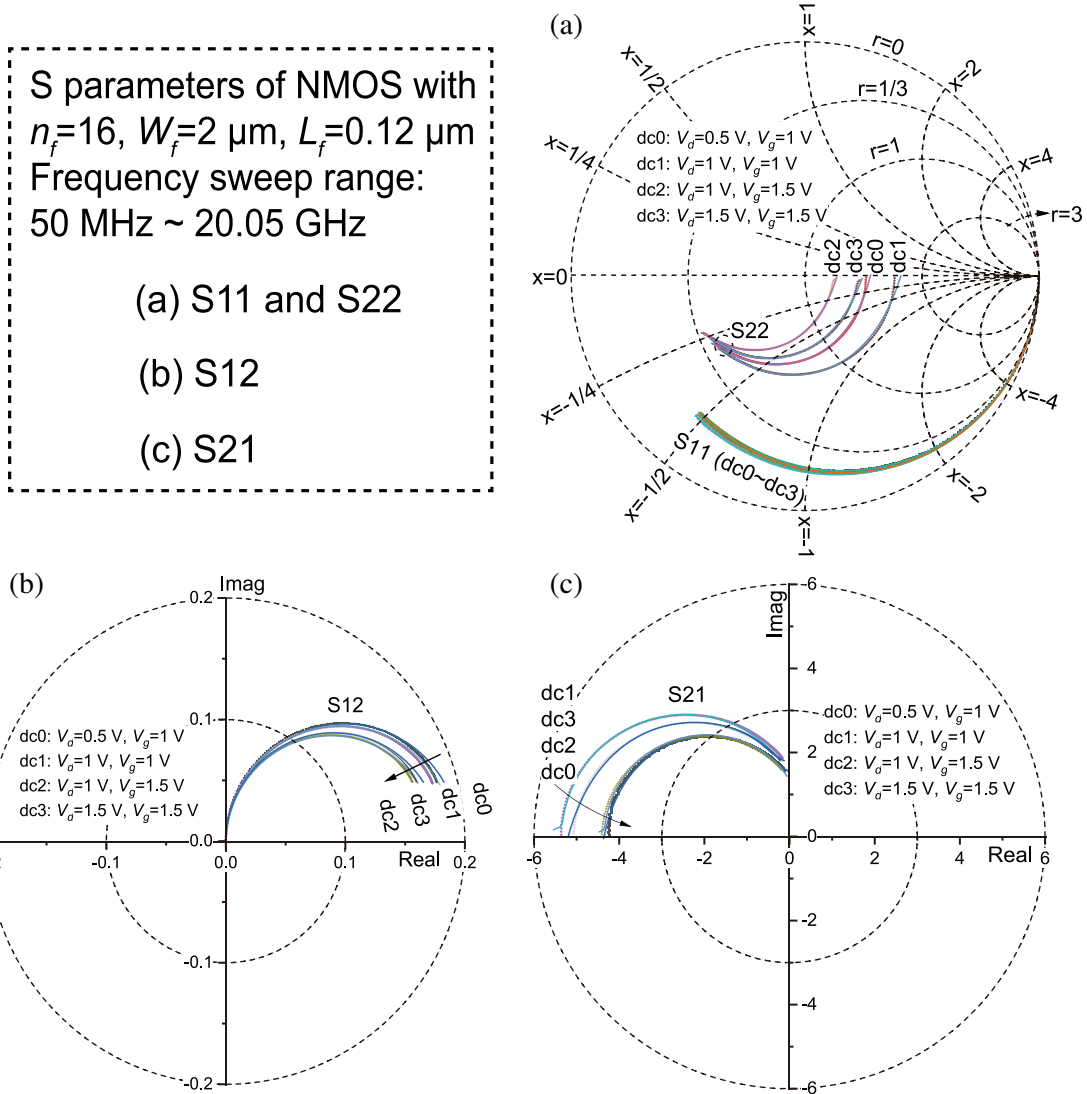
**Figure 7.** The $S$ parameters fitting results of NMOS device with $W_f = 2\,\mu\text{m}$, $L_f = 0.12\,\mu\text{m}$, $n_f = 16$.

(i) Find the model parameters' dependency on a single geometry quantity.

(ii) Combine the dependency on every geometry quantity to get the overall scalable relations.

One thing to be noted is the units of geometry quantity in the following scalable formulas. $n_f$ is dimensionless, and the unit of $W_f$ and $L_f$ is $\mu\text{m}$.

Figure 8 tells the scalable method of parameter gate resistance $R_g$ of NMOS. Fig. 8(a) shows that the gate resistance $R_g$ is roughly inversely proportional to the number of fingers. Fig. 8(b) indicates that the gate resistance $R_g$ also has an inverse proportional relation on the finger width $W_f$. Fig. 8(c) gives an inverse proportional relation between gate resistance $R_g$ and value $L_f^{0.13}$. The overall scalable expression of the gate resistance $R_g$ is depicted in Fig. 8(d). The data tells that the gate resistance $R_g$ is proportional to the value of $n_f^{-1}W_f^{-1}L_f^{-0.13}$ for all NMOS devices. Similar operation processes can also be applied to other model parameters.

The scalable method is also practical for PMOS. Figs. 9(a) and (b) give the scalable relations of gate inductance $L_g$ and body resistance $R_b$ of PMOS. They are found as $L_g \propto n_f^{-0.85}W_f^{-1.5}L_f^{-0.75}$ and $R_b \propto n_f^{-0.7}W_f^{-0.55}L_f^{-0.22}$ respectively for PMOS.
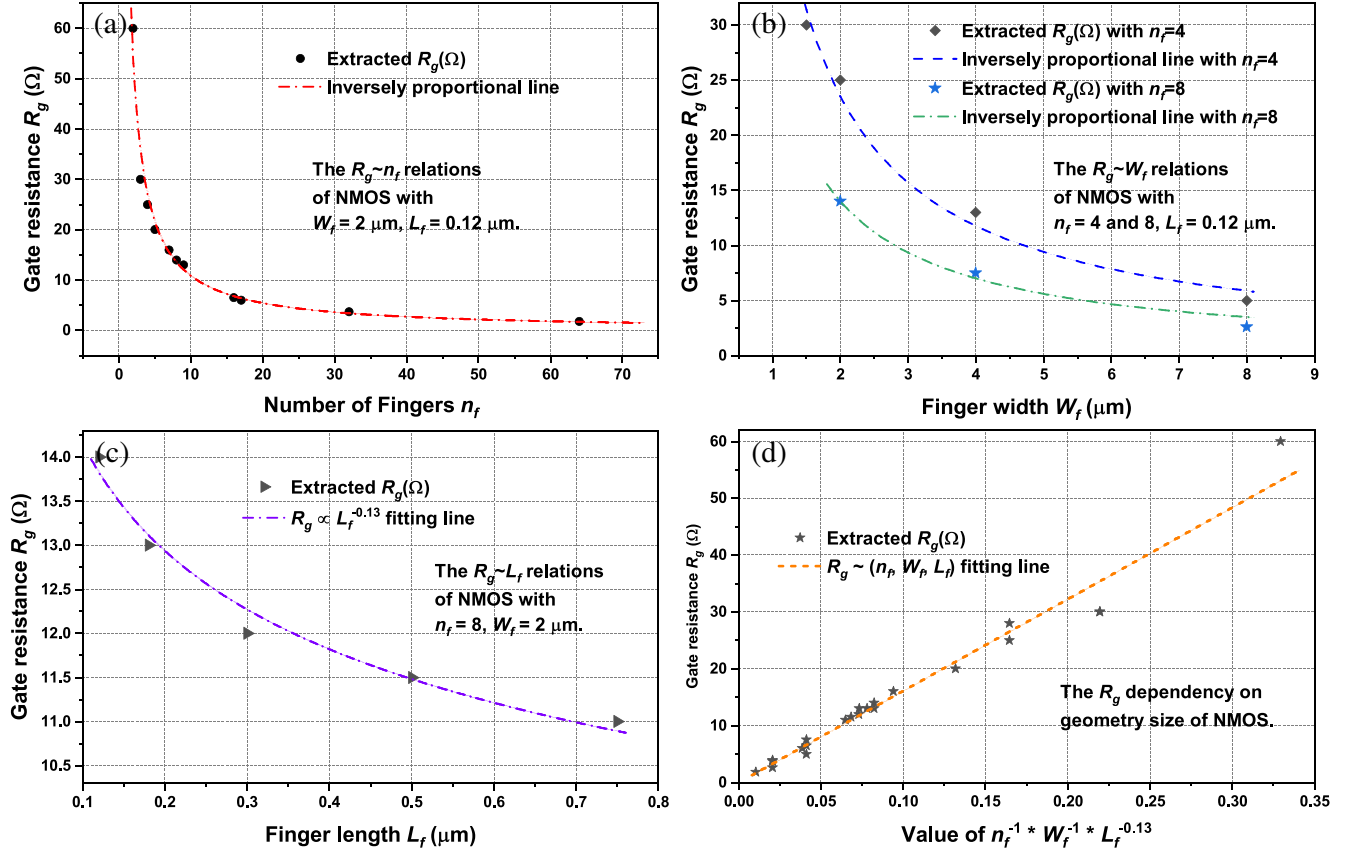
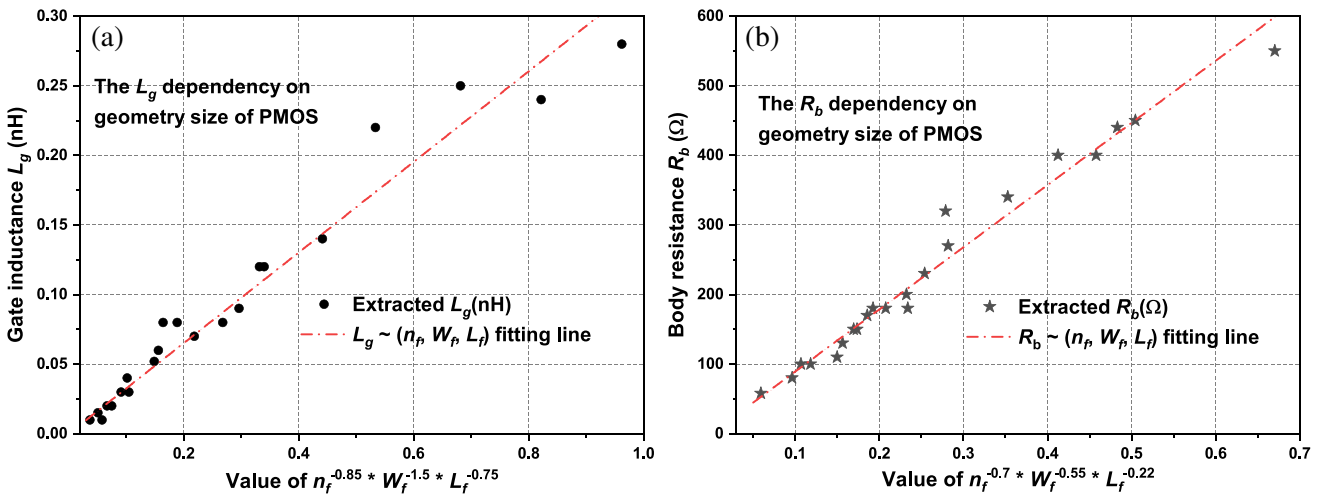**Figure 8.** The gate resistance $R_g$ dependency on the geometry size of NMOS.



**Figure 9.** The gate inductance $L_g$ and body resistance $R_b$ dependency on the geometry size of PMOS.

## 4. CONCLUSION

A scalable PSP RF model is extracted and verified in 0.11 μm CMOS process. The PSP RF model equivalent circuit is constructed by a PSP core model and other related parasitic components which need be considered and extracted for high frequency behaviors modeling. For the parasitic components' extraction, $S$ parameters are measured and de-embedded before model parameters extraction. The open-short de-embedding technique is applied to the raw measured data. The zero bias extraction method is used for the RF parameters extraction. By combining the parameters' dependency on every single geometry quantity, the scalable expression with all geometry quantities is obtained. The scalable method is meaningful for the RF model parameters extractions. The scalable model has advantages of universality and computational efficiency.

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