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Optimization of Bus Capacitance of Six-Phase Permanent Magnet Power Generation System Based on PWM Modulation

Zhigang Zhang, Jiamian Chang, Mengdi Li*, Pengcheng Zhang, and Wenjuan Zhang

Abstract—The reliability of DC-bus capacitors in six-phase drives is an important issue in multi-phase drive systems, and the influence of symmetrical and asymmetrical motor winding loads on the lifetime of DC-bus capacitors is essential. This article uses the SVPWM modulation algorithm to analyze the current and voltage ripple of DC-bus capacitors in a six phase voltage source inverter. Then, by optimizing the capacitance value when searching for the maximum stress point, the capacitance range of the DC-bus capacitors is determined. At a power factor of 0.6 and modulation ratios of 0.4, 0.7, and 0.9, considering the changes in ESR, current, and voltage ripple in the capacitor, taking 80% of the rated lifespan as an example, it is found that the lifespan of the DC-bus capacitors in symmetrical configuration of the motor winding is increased by 0.20%, 1.80%, and 10.08% compared to that in asymmetric configuration, respectively. Finally, the analytical and experimental results were compared with existing methods, and the experimental results verified the effectiveness of the proposed method.

1. INTRODUCTION

Thanks to the development of modern power electronics technology, the application of multiphase motors in industry has also shifted from theory to reality.

Compared with the general three-phase motor drive system, multiphase motor drive system has significant advantages. Firstly, the increase in the number of phases in the system enables the effective distribution of motor output power among multiple motor windings, enabling low-voltage and high-power control on the basis of existing power devices. Secondly, as the number of phases increases, the system has a richer spatial voltage vector, and the segmentation of voltage space tends to be more refined, which can significantly reduce the frequency of motor torque ripple and the harmonic content of the DC-bus [1–4]. The redundancy of phase numbers allows for reduced load operation without the need to shut down in the event of system phase loss, thereby improving the reliability of the system.

Currently, many industries choose multiphase drive over three-phase drives. Six-phase drive is one of the most popular multi-phase drives. In order to control the voltage of a six-phase inverter with a sinusoidal waveform output, pulse width modulation (PWM) is usually used even in cases of load asymmetry. Some PWM techniques for inverters have been proposed to achieve sinusoidal output voltage and improve other performances [5–8]. Due to certain requirements for volume, weight, and cost of DC-bus capacitors, excessive design of DC-bus capacitors should be avoided. On the other hand, if DC-bus capacitors are too small, high DC-bus voltage ripple will occur and affect the PWM process, which may cause distortion of the output voltage and reduce the service life of the capacitor. Therefore, conducting ripple analysis on the current and voltage of the DC link is crucial for optimizing the design of DC-bus capacitors [9–11].

In [12, 13], modulation methods such as Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM), and Discontinuous PWM (DPWM) were studied, and spectral analysis techniques were used to select

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capacitors for the three-phase inverter DC-bus based on ripple rating and lifespan prediction. However, this has not been extended to the study of multi-phase inverters. Reference [14] analyzed control techniques based on synchronous input and output AC power to reduce low-frequency AC power and voltage fluctuations in the DC-bus. However, additional circuits and control schemes will generate new potential faults in the DC-bus section, and there has been no effective evaluation of capacitor life. The influence of electrical stress on DC-bus capacitors was analyzed in [15], but the impact of thermal stress caused by changes in Equivalent Series Resistance (ESR) and temperature on the lifespan of capacitors on DC-bus was not considered. In [16, 17], the frequency spectrum analysis of DC current ripple was performed using double Fourier series method for continuous and discontinuous modulation schemes in two-stage and multi-stage three-phase voltage source inverters. This method is commonly used to determine the output harmonics generated by the PWM processes. Reference [18] studied the adverse effects of harmonic currents on the temperature rise of capacitors and evaluated their lifespan, but did not consider the range of capacitor capacity selection.

In most of the aforementioned literature, the current and voltage analysis and calculation of DC-bus capacitors are generally assumed to be symmetrical loads. So far, there has been insufficient research on the current and voltage ripple of DC-bus capacitors under asymmetric loads. Similarly, the life assessment of DC-bus capacitors under two different load configurations is also insufficient. Therefore, this article will conduct further research on the above situation.

The remaining part of this article is as follows. In the second section, the configuration of the six phase motor winding is introduced. The third section analyzes the current and voltage ripple of DC-bus capacitors. The fourth section analyzes the capacitance design range of capacitors. It optimizes the capacitance of the capacitor based on the analysis of the maximum stress point. The fifth section evaluates the lifespan of DC-bus capacitors under symmetrical and asymmetric motor winding loads. The sixth section conducts simulation and experimental verification. Finally, the seventh section draws a conclusion.

2. SIX-PHASE VOLTAGE SOURCE INVERTER AND LOAD WINDING CONFIGURATION

A schematic diagram of the six-phase voltage source inverter structure is shown in Figure 1, while Figure 2 shows the symmetrical ($\delta = pi/3$) and asymmetrical ($\delta = pi/6$) configurations of the six-phase motor windings ABC1 and ABC2. V_{dc} is used to provide power.

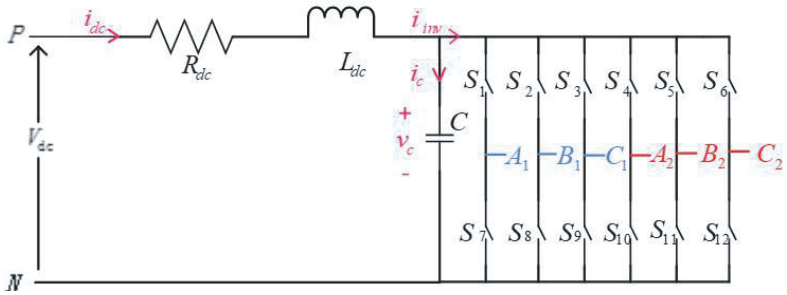
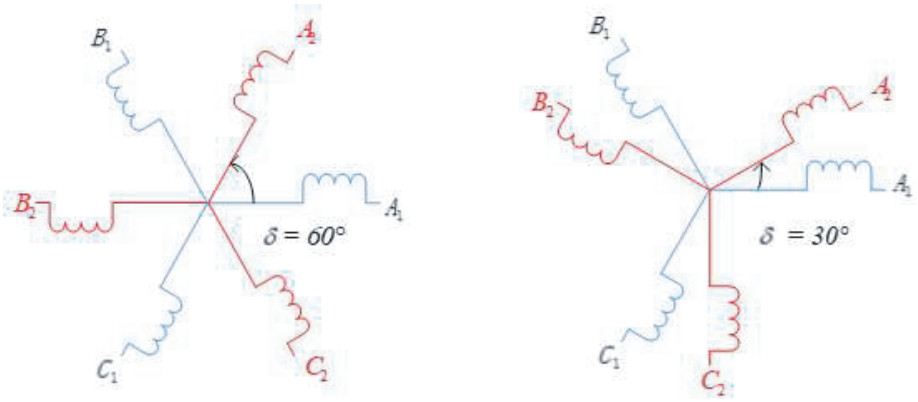


Figure 1. Structure of six-phase voltage source inverter.

The modulated voltage signal of the six-phase inverter is shown in (1):

$$\begin{cases} v_{A1} = M\sin\theta + v_0 \\ v_{B1} = M\sin(\theta + 120^\circ) + v_0 \\ v_{C1} = M\sin(\theta + 120^\circ) + v_0 \\ v_{A2} = M\sin(\theta - \delta) + v_0 \\ v_{B2} = M\sin(\theta - 120^\circ - \delta)) + v_0 \\ v_{C2} = M\sin(\theta + 120^\circ - \delta) + v_0 \end{cases} \tag{1}$$



(a) Symmetrical configuration (b) Asymmetrical configuration

Figure 2. Six-phase motor winding configuration.

where $\theta = 2\pi f_1 t$, f_1 is the fundamental frequency; δ is the phase shift angle between the two three-phase windings ($\delta = pi/3$ and $\delta = pi/6$ for the symmetrical and asymmetrical windings, respectively); M is the modulation index; and v_0 is the zero-sequence voltage. The six-phase output current of the inverter bridge is shown in (2):

$$\begin{cases} i_{A1} = \sqrt{2} I_L \sin(\theta - \varphi) \\ i_{B1} = \sqrt{2} I_L \sin(\theta - \frac{2}{3}\pi - \varphi) \\ i_{C1} = \sqrt{2} I_L \sin(\theta + \frac{2}{3}\pi - \varphi) \\ i_{A2} = \sqrt{2} I_L \sin(\theta - \varphi - \delta) \\ i_{B2} = \sqrt{2} I_L \sin(\theta - \frac{2}{3}\pi - \varphi - \delta) \\ i_{C2} = \sqrt{2} I_L \sin(\theta + \frac{2}{3}\pi - \varphi - \delta) \end{cases} \tag{2}$$

where I_L is the load current; φ is the power factor angle (PF angle).

If the capacitance of the DC-bus is large enough, then most of the ripple on the DC side can be filtered out, $\tilde{i}_{dc} = 0$. At this point, $\tilde{i}_c = -\tilde{i}_{inv}$, then one can use i_{inv} to analyze the current ripple of DC-bus capacitors.

3. CURRENT AND VOLTAGE RIPPLE OF DC-BUS CAPACITORS IN SIX-PHASE INVERTERS

According to the circuit in Figure 1, the input current of the inverter i_{inv} is determined by the load current and switch $S_1 - S_{12}$. A switch function is used to define the state of the switch tube. The switch function is 1 or 0, where 1 represents that the switch tube is on, and 0 represents that the switch tube is off. Therefore, the expression for i_{inv} is:

$$i_{inv} = \sum\nolimits_x i_x \times S_x \tag{3}$$

where i_x is the output current of the inverter, and S_x is a Boolean function that simulates the switching state and can be expressed as:

$$S_x = \begin{cases} 1, & top\ switch\ is\ ON \\ 0, & bottom\ switch\ is\ ON \end{cases} \tag{4}$$

Each half switching cycle can be divided into seven time periods T_0, T_1, T_2, T_3, T_4, T_5, and T_6, and

the values of each time period T_0, T_1, T_2, T_3, T_4, T_5, and T_6 are shown in (5):

$$\begin{cases} T_0 = \dfrac{T_s}{4}\left(1 - M\sin\theta - v_0\right) \\ T_1 = \dfrac{T_s}{4}M\left[\sin\theta - \sin\left(\theta + 120^\circ - \delta\right)\right] \\ T_2 = \dfrac{T_s}{4}M\left[\sin\left(\theta + 120^\circ - \delta\right) - \sin\left(\theta - \delta\right)\right] \\ T_3 = \dfrac{T_s}{4}M\left[\sin\left(\theta - \delta\right) - \sin\left(\theta + 120^\circ\right)\right] \\ T_4 = \dfrac{T_s}{4}M\left[\sin\left(\theta + 120^\circ\right) - \sin\left(\theta - 120^\circ\right)\right] \\ T_5 = \dfrac{T_s}{4}M\left[\sin\left(\theta - 120^\circ\right) - \sin\left(\theta - 120^\circ - \delta\right)\right] \\ T_6 = \dfrac{T_s}{4}\left[1 + M\sin\left(\theta - 120^\circ - \delta\right) + v_0\right] \end{cases} \tag{5}$$

When the six-phase voltage source inverter is connected to a symmetrical motor winding load, i_{inv} is uniformly distributed into 12 modes at $\pi/6$ intervals, and the waveforms of PWM, switching states, i_{inv}, and v_c at $\pi/3$ to $\pi/2$ intervals are shown in Figure 3.

The inverter DC-bus input side current is shown in (6):

$$i_{inv} = \begin{cases} 0, & for\ t_0 \le t \le t_1 \\ i_{A1}, & for\ t_1 \le t \le t_2 \\ i_{A1} + i_{C2}, & for\ t_2 \le t \le t_3 \\ i_{A1} - i_{B2}, & for\ t_3 \le t \le t_4 \\ -\left(i_{B1} + i_{B2}\right), & for\ t_4 \le t \le t_5 \\ -i_{B2}, & for\ t_5 \le t \le t_6 \\ 0, & for\ t_6 \le t \le t_8 \\ -i_{B2}, & for\ t_8 \le t \le t_9 \\ -\left(i_{B1} + i_{B2}\right), & for\ t_9 \le t \le t_{10} \\ i_{A1} - i_{B2}, & for\ t_{10} \le t \le t_{11} \\ i_{A1} + i_{C2}, & for\ t_{11} \le t \le t_{12} \\ i_{A1}, & for\ t_{12} \le t \le t_{13} \\ 0, & for\ t_{13} \le t \le t_{14} \end{cases} \tag{6}$$

The current ripple value on the input side of the six phase voltage source inverter under symmetrical motor winding is:

$$\tilde{I}_{inv} = I_L \left\{ \frac{M}{\pi}\left[3 + 3\sqrt{3} - \frac{9\pi}{4}M + \left(4 + 2\sqrt{3} - \frac{9\pi}{4}M\right)\cos 2\varphi\right]\right\}^{1/2} \tag{7}$$

When the six-phase voltage source inverter is connected to an asymmetric motor winding load, i_{inv} is unevenly distributed in 18 patterns at $\pi/6$ and $\pi/12$ intervals. The current ripple value on the input side of the inverter in a six-phase voltage source inverter under asymmetric motor winding load is:

$$\tilde{I}_{inv} = I_L \left\{ \frac{M}{2\pi}\left[2\left(\sqrt{3} - \sqrt{2}\right) + \sqrt{6} + \left(4\sqrt{2} + 8\sqrt{3} + 4\sqrt{6} - 9\pi M\right)\cos^2\varphi\right]\right\}^{1/2} \tag{8}$$

From [19], $\tilde{I}_{inv}$ of the three-phase inverter connected to the motor winding is given as follows:

$$\tilde{I}_{inv} = I_L \left\{ 4M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{8}M\right)\right]\right\}^{1/2} \tag{9}$$

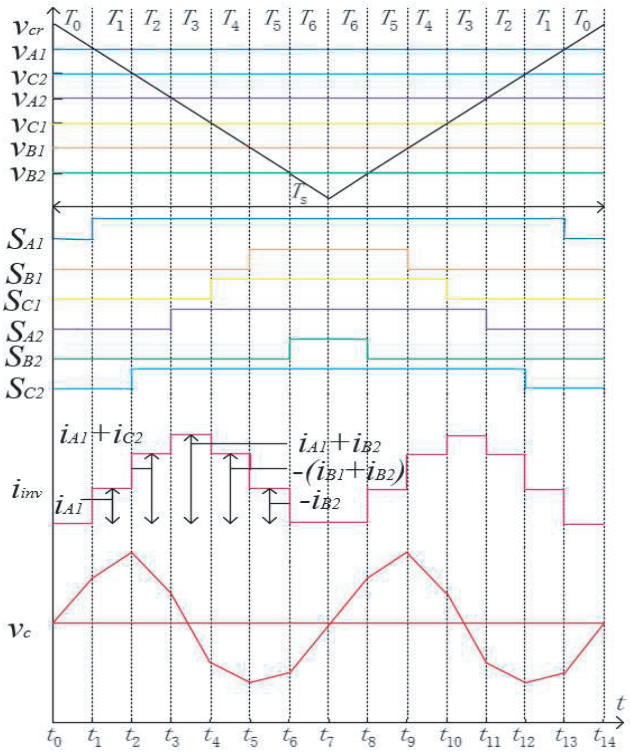


Figure 3. The switching pulse signal, i_{inv}, and v_c during the next cycle of the $\pi/3$ to $\pi/2$ interval at symmetrical motor winding load.

When the windings of a six phase motor are connected in symmetrical and asymmetric configurations, the voltage ripple value of DC-bus capacitors can be expressed as:

$$\tilde{V}_C = \frac{I_L}{8Cf_s}M\sqrt{\frac{1}{60}M + \left(6 - \frac{65}{2\pi}M + \frac{9}{2}M^2 + 18v_0^2\right)\cos^2\varphi} \tag{10}$$

$$\tilde{V}_C = \frac{I_L}{8Cf_s}M\left\{3 - \frac{24}{5}M + \frac{9}{4}M^2 + 9v_0^2 - \frac{16}{5\pi}Mv_0\sin 2\varphi + \left(3 - \frac{21}{4}M + \frac{9}{4}M^2\right)\cos 2\varphi\right\}^{1/2} \tag{11}$$

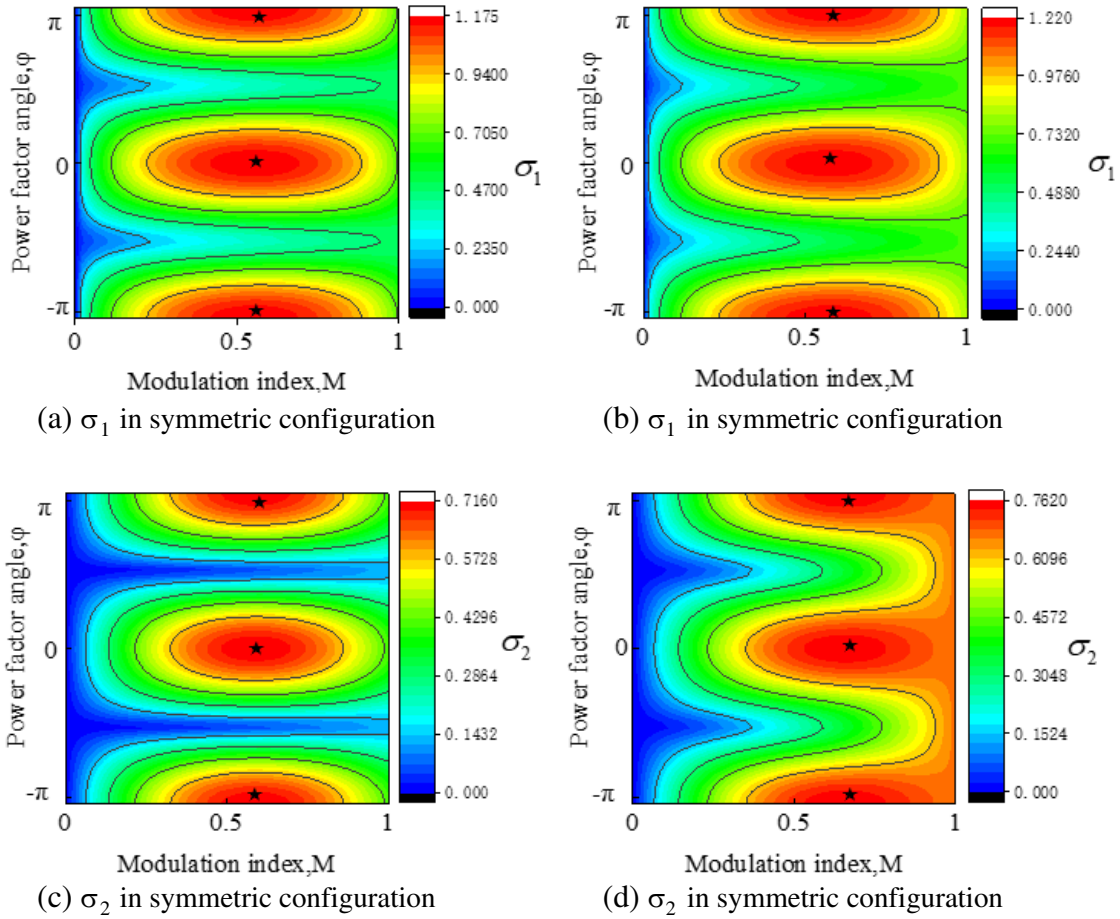
4. OPTIMIZATION RESEARCH BASED ON MAXIMUM STRESS POINT TIME CAPACITY VALUE

The modulation ratio is determined by the DC input voltage and output voltage. Through formulas (7), (8), (10), and (11), it can be concluded that the main factors affecting the current and voltage ripple of DC-bus capacitors include M_φ. Regarding the selection of the capacitance value of DC-bus capacitors, on the one hand, the rated current that the capacitor passes through should be greater than the current ripple it bears, and on the other hand, it can withstand voltage ripple below 10% of the rated voltage.

Therefore, this article proposes an optimized design for the capacitance value of the busbar based on the maximum stress point. So the study of current and voltage stress related to current and voltage ripple is particularly important. By using formulas (7), (8), (10), and (11), the current and voltage stresses of two types of motor winding configurations can be expressed as $\sigma_I = \tilde{I}_{inv}/I_L$, $\sigma_2 = 8Cf_s\tilde{V}_c/I_L$. The definition of the maximum stress point is shown in formula (12):

$$x^* = \arg\max_x f(x) \tag{12}$$

where $f(x)$ is σ_I, σ_2, $x = [x_1 x_2]^T = [M_\varphi]^T$. As shown in Figure 4, $\star$ provides a more intuitive representation of M_φ at the maximum stress point affected.



(a) σ_1 in symmetric configuration (b) σ_1 in symmetric configuration

(c) σ_2 in symmetric configuration (d) σ_2 in symmetric configuration

Figure 4. M_φ situation at the maximum stress point affected.

It can be seen that when the power factor angle $\varphi = k\pi$, $k = -1, 0, 1$, there exists a maximum stress point, which is independent of the configuration of the motor winding. Under the influence of M, the maximum stress points for symmetric and asymmetric motor winding configurations are shown in Table 1.

Table 1. M at maximum stress point in two configurations.

	Symmetric configuration	Asymmetric configuration
σ_1	$M = 0.51$	$M = 0.55$
σ_2	$M = 0.60$	$M = 0.72$

Substituting M and φ at the maximum stress point into (7) and (8), the rated current ranges of DC-bus capacitors for the six phase permanent magnet power generation system in symmetrical and asymmetric motor winding configurations can be obtained, which are $I_1 \geq 6I_L/5$, $I_2 \geq 5I_L/4$. To ensure that the total harmonic distortion of the output voltage after PWM modulation is relatively small, the voltage of the DC-bus must be relatively stable. Therefore, M and φ are substituted into (10) and (11), respectively. As shown in (13), the capacitance range of the DC-bus capacitors for two configurations

is obtained.

$$C \geqslant \begin{cases} \dfrac{3\sqrt{3}I_L}{16f_s\Delta V_{\max}}, & symmetric\ configuration \\ \dfrac{4\sqrt{3}I_L}{16f_s\Delta V_{\max}}, & asymmetric\ configuration \end{cases} \tag{13}$$

Among them, $\Delta V_{\max}$ is the maximum voltage ripple value of the busbar capacitor. The capacitance value of the capacitor calculated in this way can effectively reduce the loss of bus capacitance, greatly reducing costs.

5. LIFETIME ASSESSMENT

The current stress caused by $\tilde{I}_{inv}$ is an important stress source that affects the lifespan of DC-side capacitors. Throughout the entire frequency range, $\tilde{I}_{inv}$ has an impact on the thermal load of the capacitors, which also greatly reduces the reliability of the capacitor. At a certain frequency, the power loss is a function of ripple current and ESR, while the total power loss is the sum of the power losses over the entire frequency range, as shown in (14):

$$P_{loss} = \sum\nolimits_{i=1}^{n} \left[ESR\left(f_i\right) \times I_{rms}^2\left(f_i\right)\right] \tag{14}$$

Among them $ESR(f_i)$ is the equivalent series resistance at frequency f_i, and $I_{rms}(f_i)$ is the root mean square value of current ripple at frequency f_i. The relationship between ESR and frequency for model LGR2G820MELZ35 electrolytic capacitor is shown in Figure 5.

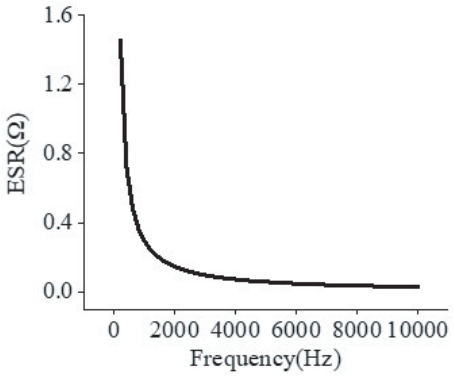


Figure 5. Relationship between ESR and frequency of electrolytic capacitors.

Thermal stress is the key stress source for capacitor failure. The ESR of the anodic oxide film that forms the aluminum electrolytic capacitor is relatively large in the low frequency range. As the frequency increases, it decreases inversely proportional to the frequency, and the capacitance also decreases inversely proportional to the frequency. The failure of the electrolytic capacitors used in this system is mainly caused by electrochemical reactions in the oxide layer and electrolyte evaporation. Both of these factors will increase the ESR over time.

The hot spot temperature of capacitors is affected by current stress and environmental temperature, as shown in (15):

$$T_h = T_a + R_{ha} * \sum\nolimits_{i=1}^{n} \left[ESR\left(f_i\right) \times I_{rms}^2\left(f_i\right)\right] \tag{15}$$

where T_h is the hot spot temperature, T_a the ambient temperature, and R_{ha} the equivalent thermal resistance from the hot spot to the ambient. For electrolytic capacitors, this system will be calculated with $R_{ha} = 1W/^{\circ}\mathrm{C}$.

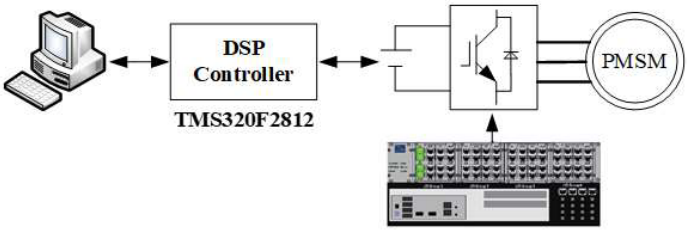
Therefore, a lifetime model is proposed as shown in (26):

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-p_1} \times 2^{\frac{T_a - T_h}{p_2}} \tag{16}$$

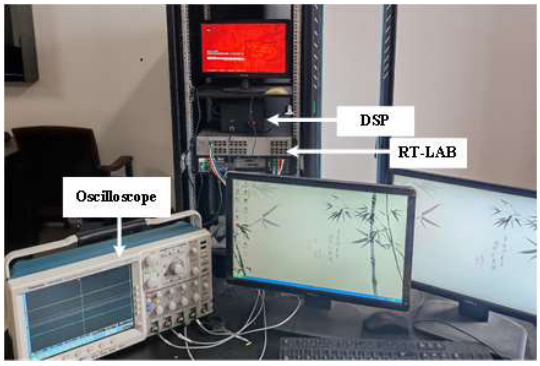
where L_0, V_0, V, T_a, and T_h are the rated life, rated voltage, true voltage, ambient temperature, and hot spot temperature of the capacitor. As for electrolytic capacitors, $p_1 \in [3, 5]$ and $p_2 \in [9, 11]$, this system will be calculated with $p_1 = 4$ and $p_2 = 10$.

6. SIMULATION AND EXPERIMENTAL VALIDATION

In order to verify the correctness of the above theoretical analysis, a Simulink simulation model was established and downloaded to RT-LAB (OP5600) to implement a semi-physical system of a six-phase permanent magnet drive system. The TMS320F2812 was used for the controller, and RT-LAB was used for the inverter and other components. Figure 6(a) shows the schematic of the RT-LAB hardware-in-the-loop system, and Figure 6(b) shows the RT-LAB platform. Figure 7 depicts the RT-LAB hardware



(a) Systemin-the-loop configuration



(b) Semi-physical composition

Figure 6. RT-LAB semi-physical experimental platform.

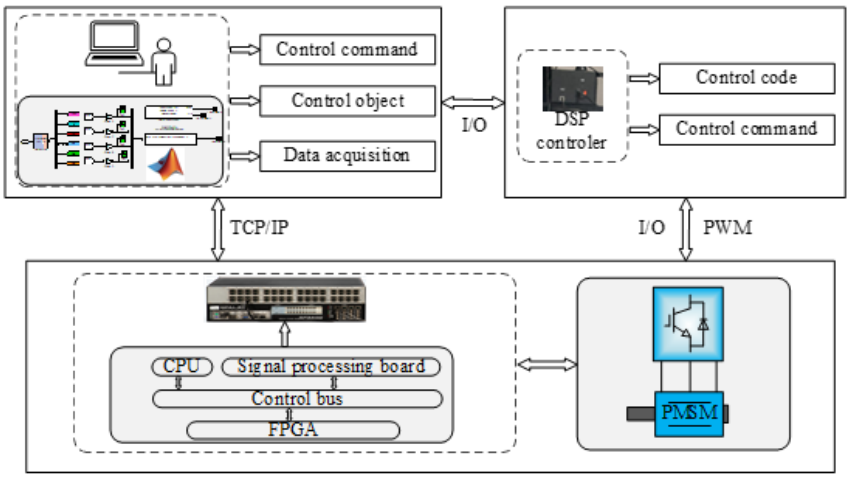


Figure 7. RT-LAB hardware system block diagram.

Table 2. Experimental setup and simulation parameters.

Parameter	Symbol	Value	Unit
Dc-link voltage	V_{dc}	100	V
Dc-link capacitor	C	80	μF
Dc-link resistance	R_{dc}	30	mΩ
Dc-link inductance	L_{dc}	10	μH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_s	10	kHz
Switching dead time	t_d	2	μs

Table 3. RL load parameters per phase.

PF ($f_1 = 50\,\text{Hz}$)	0.6	0.8	0.9
$R\Omega$	1.1	2.2	4.4
L (mH)	5.0	5.0	5.0

Table 4. Simulated current and voltage ripple values of DC-Bus capacitors in six phase voltage source inverters under SPWM modulation algorithm.

Configuration	Symbol	Unit	$M = 0.4$	$M = 0.7$	$M = 0.9$
Symmetrical	$\tilde{v}_c$	V	1.9000	4.0000	4.2000
	$\tilde{i}_{inv}$	A	5.1000	10.2000	11.1000
Asymmetrical	$\tilde{v}_c$	V	3.0000	9.0000	17.0000
	$\tilde{i}_{inv}$	A	5.3000	10.9000	12.2000

system diagram. Table 2 lists the basic parameters of this inverter, while Table 3 shows the RL parameters and power factor (PF) values of each phase motor winding load.

Figure 8 shows the simulated waveform of the inverter input-side current ripple $\tilde{i}_{inv}$ in one cycle, from which it can be seen that $\tilde{i}_{inv}$ is a pulsating current with a profile similar to a six-pulse wave.

Figure 9(a) depicts the simulation results of DC-bus capacitors current and voltage ripple under two motor winding configurations, $PF = 0.6$ and $M = 0.4$. Figure 9(b) depicts the simulation results of DC-bus capacitors current and voltage ripple under two motor winding configurations, $PF = 0.6$ and $M = 0.7$. Figure 9(c) depicts the simulation results of DC-bus capacitors current and voltage ripple under two motor winding configurations, $PF = 0.6$ and $M = 0.9$. It can be observed that when $PF = 0.6$, the current and voltage ripple of DC-bus capacitors increase with the increase of modulation ratio. Under the same modulation ratio, when the winding load of a six phase motor is symmetrically configured, there are lower current and voltage ripple on DC-bus capacitors. Among them, when $PF = 0.6$, $M = 0.4$, $M = 0.7$, and $M = 0.9$, the peak voltage ripple of DC-bus capacitors under symmetrical motor winding load is reduced by 15.63%, 33.33%, and 50.40% compared to the asymmetric configuration, respectively.

According to Tables 4 and 5, it can be seen that under the SVPWM modulation algorithm, the capacitor current and voltage ripple are significantly reduced.

Figure 10 depicts the experimental results of the current and voltage ripple of DC-bus capacitors in a six-phase voltage source inverter under symmetrical and asymmetrical motor winding loads. It can be

Table 5. Simulated and experimental values of current and voltage ripples of DC-Bus capacitors in six phase voltage source inverters under SVPWM modulation algorithm.

Configuration	Type	Symbol	Unit	$M = 0.4$	$M = 0.7$	$M = 0.9$
Symmetrical	Simulation	$\tilde{v}_c$	V	1.3500	2.5000	3.1000
		$\tilde{i}_{inv}$	A	4.1233	9.4713	10.4969
	Experimental	$\tilde{v}_c$	V	1.2000	2.8400	2.8400
		$\tilde{i}_{inv}$	A	4.8000	10.0000	10.3800
Asymmetrical	Simulation	$\tilde{v}_c$	V	1.6000	3.7500	6.2500
		$\tilde{i}_{inv}$	A	4.4695	10.6934	12.7136
	Experimental	$\tilde{v}_c$	V	1.2800	3.7600	5.3200
		$\tilde{i}_{inv}$	A	4.7000	10.3600	11.9800

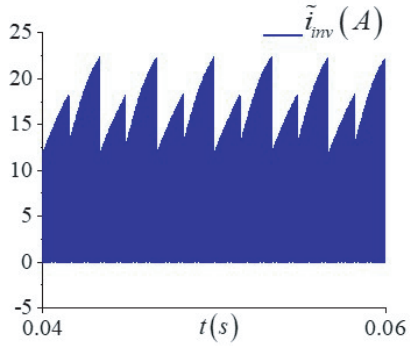
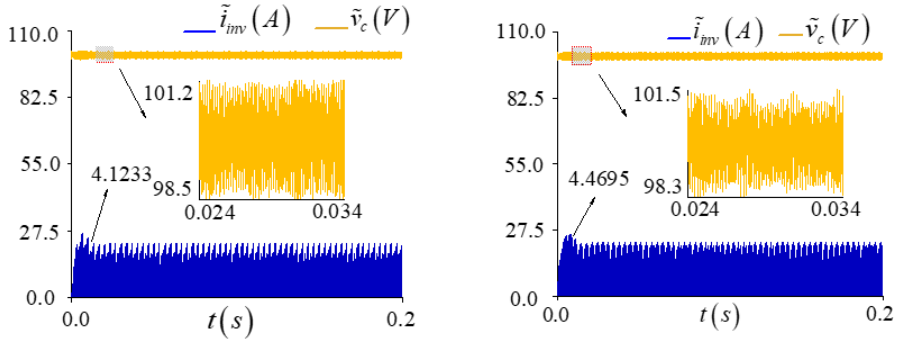
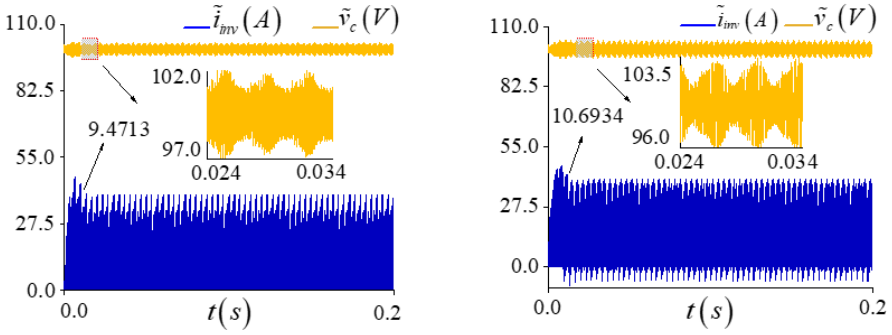


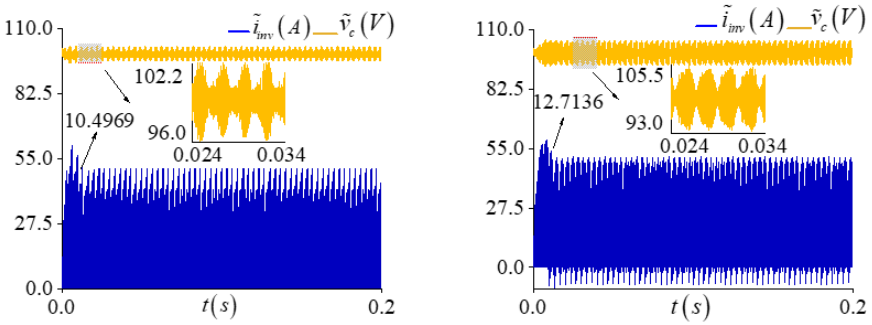
Figure 8. $\tilde{i}_{inv}$ simulation waveform.



(a) PF = 0.6, M = 0.4

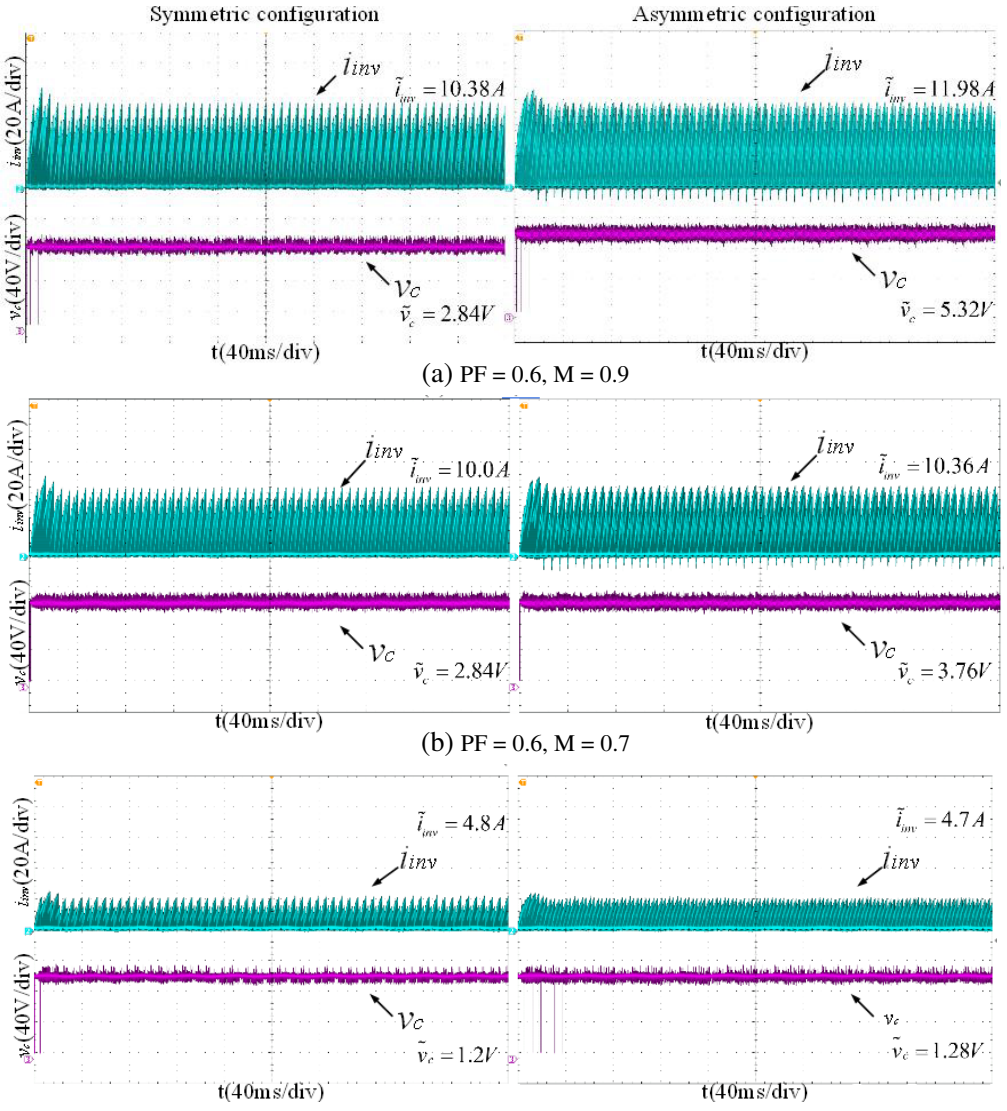


(b) PF = 0.6, M = 0.7



(c) PF = 0.6, M = 0.9

Figure 9. Simulation results of current and voltage ripple of DC-bus capacitors in a six-phase voltage source inverter with symmetrical (left column) and asymmetrical (right column) motor winding loads.



(a) PF = 0.6, M = 0.9

(b) PF = 0.6, M = 0.7

(c) PF = 0.6, M = 0.4

Figure 10. Experimental results of current and voltage ripple of DC-bus capacitors in a six-phase voltage source inverter with symmetrical (left column) and asymmetrical (right column) motor winding loads.

seen that the current ripple of DC-bus capacitors under symmetrical motor winding is generally smaller than that under asymmetric conditions. When PF remains constant, the voltage ripple of DC-bus capacitors increases with the increase of M, and the voltage ripple under the same symmetrical motor winding load decreases compared to the asymmetric load, which also fully verifies the consistency with the simulation results.

Figure 11 shows the Cumulative Distribution Function (CDF) diagram for evaluating the lifespan of DC-bus capacitors in the six-phase voltage source inverter under symmetrical and asymmetrical motor winding loads. It can be seen that when $PF = 0.6$ and $CDF = 0.8$, the critical life values of DC-bus capacitors under symmetrical motor winding load at $M = 0.4$, $M = 0.7$, and $M = 0.9$ are approximately 10180 h, 9589 h, and 8281 h, respectively. When $PF = 0.6$ and $CDF = 0.8$, the critical life values of DC-bus capacitors under asymmetric motor winding load at $M = 0.4$, $M = 0.7$, and $M = 0.9$ are approximately 10160 h, 9419 h, and 7523 h, respectively. Therefore, the critical values for reaching 80% of the rated life probability of DC-bus capacitors under symmetrical motor winding are increased by 0.20%, 1.80%, and 10.08%, respectively, compared to those under asymmetric motor winding.

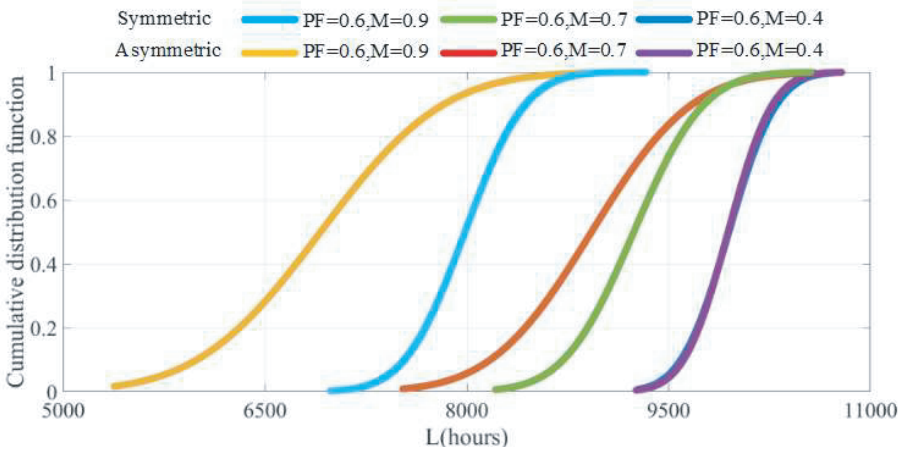


Figure 11. CDF diagram for life assessment of DC-bus capacitors in a six-phase voltage source inverter under symmetrical and asymmetrical winding motor winding loads.

7. CONCLUSION

This article analyzes the current and voltage ripple on DC-bus capacitors in a six-phase voltage source inverter under symmetrical and asymmetrical motor winding loads. When SVPWM modulation method is used, compared with asymmetric winding loads, the current and voltage ripple of DC bus capacitors under symmetric motor winding loads are significantly improved. Subsequently, the range of bus capacitor capacitance values is optimized through analysis at the maximum stress point. Finally, at a power factor of 0.6 and CDF of 0.8, it was found that the lifespan of DC-bus capacitors under symmetrical motor winding loads at $M = 0.4$, $M = 0.7$, and $M = 0.9$ is increased by 0.20%, 1.80%, and 10.08%, respectively, compared to asymmetric loads. In this article, the impact of changes in ESR at high frequencies on the power loss of DC-bus capacitors is not considered, and the next step will focus on this issue.

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REFERENCES

1. Salem and M. Narimani, "A review on multiphase drives for automotive traction applications," *IEEE Trans. Transp. Electrif.*, Vol. 5, No. 4, 1329–1348, Dec. 2019.
2. Levi, E., F. Barrero, and M. J. Duran, "Multiphase machines and drives — Revisited," *IEEE Trans. Ind. Electron.*, Vol. 63, No. 1, 429–432, Jan. 2016.
3. Taha, W., P. Azer, A. D. Callegaro, and A. Emadi, "Multiphase traction inverters: State-of-the-art review and future trends," *IEEE Access*, Vol. 10, 4580–4599, 2022.
4. Abdel-Khalik, A. S., M. S. Abdel-Majeed, and S. Ahmed, "Effect of winding configuration on six-phase induction machine parameters and performance," *IEEE Access*, Vol. 8, 223009–223020, 2020.
5. Taylor, J., D. F. Valencia Garcia, W. Taha, M. Mohamadian, D. Luedtke, B. Nahid-Mobarakeh, B. Bilgin, and A. Emadi, "Dynamic modelling of multiphase machines based on the VSD transformation," *SAE Int. J. Adv. Curr. Pract. Mobil.*, Vol. 3, No. 4, 1620–1631, 2021.
6. Abdelrahman, A., Y. Wang, D. Al-Ani, and B. Bilgin, "Comparative analysis of two rotor topologies for a high-power density dual three-phase IPM propulsion motor," *2021 IEEE Transp. Electrific. Conf. Expo (ITEC)*, 1–5, Chicago, IL, 2021.
7. Feng, G., C. Lai, W. Li, Z. Li, and N. C. Kar, "Dual reference frame based current harmonic minimization for dual three-phase PMSM considering inverter voltage limit," *IEEE Trans. Power Electron.*, Vol. 36, No. 7, 8055–8066, Jul. 2021.
8. Sun, J., Z. Liu, Z. Zheng, and Y. Li, "An online global fault-tolerant control strategy for symmetrical multiphase machines with minimum losses in full torque production range," *IEEE Trans. Power Electron.*, Vol. 35, No. 3, 2819–2830, Mar. 2020.
9. Zeng, Z., X. Zhang, F. Blaabjerg, H. Chen, and T. Sun, "Stepwise design methodology and heterogeneous integration routine of air-cooled SiCinverter for electric vehicle," *IEEE Trans. Power Electron.*, Vol. 35, No. 4, 3973–3988, Apr. 2020.
10. Chowdhury, S., E. Gurpinar, and B. Ozpineci, "Capacitor technologies: Characterization, selection, and packaging for next-generation power electronics applications," *IEEE Trans. Transp. Electrif.*, Vol. 8, No. 2, 2710–2720, Jun. 2022.
11. Guo, J., J. Ye, and A. Emadi, "DC-link current and voltage ripple analysis considering antiparallel diode reverse recovery in voltage source inverters," *IEEE Trans. Power Electron.*, Vol. 33, No. 6, 5171–5180, Jun. 2018.
12. Mariscotti, A., "Analysis of the dc-link current spectrum in voltage source inverters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, Vol. 49, No. 4, 484–491, Apr. 2002.
13. McGrath, B. P. and D. G. Holmes, "A general analytical method for calculating inverter dc-link current harmonics," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 5, 1851–1859, Sep./Oct. 2009.
14. Freitas, I. S., C. B. Jacobina, and E. C. dos Santos, "Single-phase to single-phase full-bridge converter operating with reduced ac power in the dclink capacitor," *IEEE Trans. Power Electron.*, Vol. 25, No. 2, 272–279, Feb. 2010.
15. Pelletier, P., J. M. Guichon, J. L. Schanen, and D. Frey, "Optimization ofa dc capacitor tank," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 2, 880–886, Mar./Apr. 2009.
16. Bierhoff, M. and F. Fuchs, "DC-link harmonics of three-phase voltage source converters influenced by the pulse width-modulation strategy — An analysis," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 5, 2085–2092, May 2008.
17. McGrath, B. and D. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 5, 1851–1859, 2009.
18. Lee, K., T. M. Jahns, G. Venkataramanan, and W. E. Berkopec, "DC-Bus electrolytic capacitor stress in adjustable-speed drives under input voltage unbalance and sag conditions," *IEEE Transactions on Industry Applications*, Vol. 43, No. 2, 495–504, March–April 2007.
19. Kolar, J. W., T. M. Wolbank, and M. Schrodl, "Analytical calculation of the RMS current stress on the DC link capacitor of voltage DC link PWM converter systems," *Electrical Machines and Drives, 1999. Ninth International Conference on (Conf. Publ. No. 468)*, 1999.