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Bi-CMOS Design of a*exp($-j$*φ_0) Phase Shifter as Miniature Microwave Passive Circuitusing Bandpass NGD Resonant Circuit

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Abstract—The purpose of this paper is to study the RF/microwave constant phase shift (CPS) designed as an integrated circuit (IC) in 130-nm Bi-CMOS technology. The CPS understudy is constituted by a bandpass (BP) negative group delay (NGD) passive cell combined in cascade with a positive group delay (PGD) circuit. The CPS real circuit is represented by a CLC-network associated in cascade with a BP-NGD passive cell. The CPS characterization is based on the S-parameter modelling. The CPS is analytically modeled by the frequency independent transmission phase modelling by the mathematical relation $\varphi(f) = a * \exp(-j * \varphi_0) =$ constant around working frequency $[f_n - \Delta f/2, f_n + \Delta f/2]$ by denoting center frequency f_n and frequency band Δf. The analytical principle of the constant PS is explored by means of the RLC-network based NGD cell. The design formula of the NGD and CLC passive circuit parameters in function of desired operation frequency is established. The validity of the developed theory is verified with a proof-of-concept (POC). A CPS miniature IC having physical size 1.15 mm × 0.7 mm is designed and implemented as POCin 130-nm Bi-CMOS technology. The ADS® and layout versus schematic of Cadence® simulation results from 130-nm Bi-CMOS CPS POC confirms the theoretical investigation feasibility. The simulated results of the obtained CPS IC POC layout show $\varphi_0 = -67° +/- 1°$ phase shift around $f_n = 0.85$ GHz within the frequency band delimited by $f_1 = 0.73$ GHz to $f_2 = 0.984$ GHz or $\Delta f = f_2 - f_1 = 254$ GHz. The CPS robustness designed in 130-nm Bi-CMOS IC technology is stated by Monte Carlo statistical analysis from 1000 trials with respect to the component geometrical parameters. It was reported that the phase shift and insertion loss flatness's of the CPS IC is guaranteed lower than 5% in $\Delta f/f_n = 30\%$ relative frequency band around f_n.

1. INTRODUCTION

Today, the everyday life in the megalopolis depends more and more on the development of wireless communication system [1]. To satisfy the societal challenging needs, the wireless network must progress following the 6G technology roadmap [2–4]. Nevertheless, the design and implementation of 6G wireless networks require considerable technological challenges [3, 5]. High-performance antenna array constitutes one of the key elements constituting the 6G wireless network transceiver to generate accurate beam steering for wireless sensor network system. For example, innovative communication and control technique for wireless drone-based antenna array was proposed [6]. A linear beamforming and RF impairment suppression were developed for massive antenna array [7]. An innovative coupled phase locked loop array topology was introduced to design beam-steering and switching antenna array [8]. To improve the mobile wireless communication system, analysis approaches of beam-steering and

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characterization of directivity dedicated to adaptive and p-i-n diodes controlled reconfigurable antenna arrays have been studied [9, 10].

In the last two decades, remarkable antenna array topologies designed by using metamaterial (MTM) base phase shifters (PSs) were deployed [11, 12]. Various unfamiliar antenna array topologies using negative group delay (NGD) function inspired from MTMs were progressively developed as alternative solution for beam steering [13–15]. One of particularity of innovative NGD-based antenna array is the ability to operate with squint-free beamforming [14, 15]. In addition, the NGD circuits can also be potentially exploited to improve different RF and microwave devices and systems [16–28]. So far, it should be emphasized that various topologies of RF and microwave NGD circuits [16–18] were proposed in the literature. A lot of effort is required to develop the wireless communication system NGD application. In fact, the NGD circuit (NGDC) was used to design analog reflection topology building blocks for adaptive microwave signal processing applications [16]. The broadband NGD networks were also exploited for compensating microwave component effects for communication systems [17]. The effectiveness of NGD circuit for linear-phase bandpass (BP) filter was equalized by NGDCs [18]. More general NGD RF and microwave engineering as the improvement of microwave amplifiers [19], non-Foster elements [20–22], interconnection equalization [23], power dividers and phase shifters (PSs) is overviewed in [23–27]. Further wireless system application was also introduced with tri-band NGD circuits [28]. Based on the NGD delay equalization principle, the innovative design of NGD-PS operating with constant phase shift (CPS) working independently to the frequency is this decade hot topic of NGD RF/microwave engineering application [23–27]. The CPS topology is basically composed by two blocks operating with positive group delay (PGD) and NGD effect connected in cascade [23–27].

In brief, the NGD effect was discovered by physicists from negative group velocity media [29, 30]. Then, the NGV effect was experimented with split ring resonator (SRR) based MTMs [31] and also resistive lossy MTM based microwave circuits [32]. Various topologies of NGD microwave circuits as open-end transmission line (TL) [33], absorptive bandstop filter [34] and signal interference techniques [35] based structures were suggested. The design feasibility of dual-band NGD microwave circuits using different topologies as multi-coupling and defected ground structures was introduced [36–38]. One of the NGD circuit design challenges is one the application development [16–28] and miniaturization [38–41]. Despite the progressive research work on the NGD RF and microwave circuit design, the meaning and familiarity to this counterintuitive function for the non-specialist wireless communication engineers remain an open question. To enlighten the shadow around the NGD electronic engineering, a simple and fundamental theory of NGD circuit enabling to classify the different types of topologies inspired from filter theory is initiated [42]. Among the fundamental topologies, the bandpass (BP) and stop-band (SB) type NGDCs were identified [42]. Among the different types, the BP-NGD topologies are widely explored in the literature [13–41].

To tackle problem of application, the present study is particularly focused on the miniaturization by CMOS design of microwave PS devices using BP-NGD circuit [23–27]. A microstrip PS using afield effect transistor based active NGDC based distributed topology was proposed [24]. By exploiting more complex distributed NGDC, it was shown that the CPS can be designed to operate in broad frequency band [25]. An innovative application using SB-NGD topology for designing stair PS was recently introduced [27]. However, the integration issue of CPS in front-end microwave transceiver [1, 43] requires miniature circuits. To overcome the biggest challenges on NGD CPS design,further research work on the feasibility of CPS integrated circuit (IC) must be raised. By exploring an innovative LCL-network based topology [26], a 130-nm Bi-CMOS technology-based quadrature CPS was recently introduced to operate with particular value of phase shift $\varphi_0 = -90^\circ$ [44].

In the present paper, the feasibility study of CPS design to operate with non-trivial phase shift in 130-nm Bi-CMOS technology by is developed. Different from the PS study introduced in [44], we tackle the CPS design challenge of non-trivial arbitrary chosen phase value $\varphi_0 \neq \{+/-90^\circ, 180^\circ\}$ by establishing the constituting component design formulas. The proposed CPS topology under study is composed by a CLC-network circuit acting as a PGD block connected in cascade with a BP-NGD passive cell constituted by an RLC-series resonant network. This paper is organized in five main sections.

- Section 2 focuses on the description of the CPS topology operation principle constituted by PGD and NGD ideal blocks. The CPS analysis and characterization are analytically defined by the S-parameters. The ideal model of CPS is illustrated by the appropriate expression of phase shift

and transmission/reflection coefficients.

- Section 3 develops the CPS circuit theory from lumped passive cell topology which explains how to characterize the PS. The synthesis formulas allowing to determine the constituting component parameters from the CPS specification goal are established. The methodology of proposed topology CPS IC designed in Bi-CMOS technology is presented.
- Section 4 examines the proof-of-concept (POC) analysis by designing a CPS implemented in 130-nm Bi-CMOS technology. The theoretical approach and design feasibility will be verified by results from commercial tools simulation which is compared by the calculated ones from analytical model.
- Section 5 is the sensitivity analyses of phase shift, insertion and reflection losses of the 130-nm Bi-CMOS CPS IC POC based on the Monte Carlo (MC) statistic method.
- Then, the final section is the conclusion of the paper.

2. ANALYTICAL INVESTIGATION ON BP-NGD NETWORK BASEDCPS

This section introduces the topological principle and the microwave circuit theory of CPS design including the constituting PGD and BP-NGD blocks. The analytical expressions enabling to synthesize the CPS from the expected specifications are formulated. Then, the proposed CPS IC design methodology is explained.

2.1. Basic Definition Necessary for the CPS Analysis

The theoretical modelling of the CPS topology proposed in the present paper is determined from the impedance or Z-matrix operation. Acting as a two-port system, the CPS can be represented by the diagram as introduced by Fig. 1.

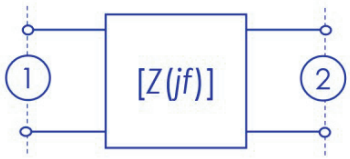

Figure 1. Two-port Z-matrix block diagram.

According to the circuit and system theory, for the case of symmetric topology, the frequency dependent Z-matrix model can be expressed by the equation:

$$[Z(jf)] = \begin{bmatrix} Z_{11}(jf) & Z_{21}(jf) \\ Z_{21}(jf) & Z_{11}(jf) \end{bmatrix}. \tag{1}$$

By means of Z-to-S matrix transform and by denoting $R_0 = 50\,\Omega$ the terminal load reference impedance, the equivalent S-parameters can be obtained by the matrix relationship:

$$[S(jf)] = \left\{ [Z(jf)] - \begin{bmatrix} R_0 & 0 \\ 0 & R_0 \end{bmatrix} \right\} \times \left\{ [Z(jf)] + \begin{bmatrix} R_0 & 0 \\ 0 & R_0 \end{bmatrix} \right\}^{-1} \tag{2}$$

with $j^2 = -1$. It yields the associated frequency domain parameters:

- Reflection and transmission parameter magnitudes: $S_{pq=\{11,21\}}(f) = |S_{pq}(jf)|$;
- Transmission phase: $\varphi(f) = \arg[S_{21}(jf)]$
- And more importantly the associated GD defined by:

$$GD(f) = \frac{-\partial\varphi(f)}{\partial(2\pi f)}. \tag{3}$$

By using this notion, we can develop the CPS topological principle as described in the following paragraph.

2.2. Topological Principle of the Developed CPS

Figure 2 represents the f-frequency dependent CPS two-port topology. The basic principle of CPS under study is based on the constituting PGD circuit represented by middle block and NGD identical circuits as lateral input/output blocks. Acting as RF and microwave circuit, the analysis is based on the S-parameters.

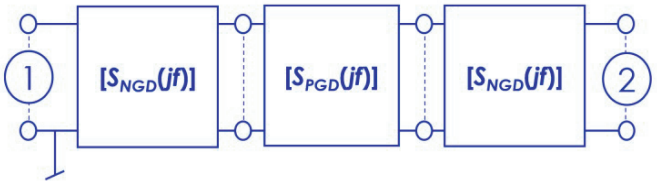

Figure 2. CPS constituting blockdiagram.

In the working frequency band $[f_1, f_2]$, the PGD and NGD blocks are ideally specified by, respectively:

$$\begin{cases} GD_{PGD}(f) = t_p > 0 \\ GD_{NGD}(f) = t_n < 0 \end{cases}. \tag{4}$$

By means definition (3), the passive circuit PGD and NGD S-matrices can be ideally written as:

$$\left[S_{x=\{PGD,NGD\}}(jf)\right] = \begin{bmatrix} B & A_x \exp\left[j(\varphi_x - 2\pi f\, t_x)\right] \\ A_x \exp\left[j(\varphi_x - 2\pi f\, t_x)\right] & B \end{bmatrix} \tag{5}$$

with the transmission coefficient magnitudes $A_{x=\{PGD,NGD\}}$:

$$\begin{cases} |S_{21,PGD}(j\omega)| = A_{PGD} < 1 \\ |S_{21,NGD}(j\omega)| = A_{NGD} < 1 \end{cases}. \tag{6}$$

We should choose the PGD and NGD blocks as well-matched access circuits. This is why the reflection coefficients must be:

$$|S_{11PGD}(jf)| = |S_{11NGD}(jf)| = A \ll 1. \tag{7}$$

2.3. *S*-Parameter Ideal Model and Characteristics of the Proposed CPS

As a matter of fact, according to the S-matrix theory, the CPS ideal model established from the diagram introduced by Fig. 2 can be written as:

$$[S_{CPS}(jf)] = [S_{NGD}(jf)] \times [S_{PGD}(jf)] \times [S_{NGD}(jf)]\,. \tag{8}$$

Because of PGD and NGD block access matching, within the frequency band $[f_1, f_2]$, we should have:

$$|S_{11CPS}(jf)| \ll 1. \tag{9}$$

Moreover, within the frequency band $[f_1, f_2]$, the CPS transmission coefficient can be ideally expressed as:

$$S_{21CPS}(jf) = A_{NGD}^2 A_{PGD} \exp\left\{j\left[2\varphi_n + \varphi_p - 2\pi f(2t_n + t_p)\right]\right\} \tag{10}$$

where:

$$\varphi_{CPS}(f) = 2\varphi_n + \varphi_p - 2\pi f(2t_n + t_p). \tag{11}$$

In the frequency band of the study $[f_1, f_2]$, the PS behaves as a constant or frequency independent phase shift if:

$$\arg[S_{21CPS}(j\omega)] = Cst \Rightarrow GD_{CPS} = 0. \tag{12}$$

The corresponding GD diagrams are depicted by Fig. 3(a). Knowing the previous constant phase hypothesis, the PGD and NGD GDs can be expressed by:

$$GD_{NGD}(f) = -GD_{PGD}(f)/2 \Rightarrow t_n = -t_p/2. \tag{13}$$

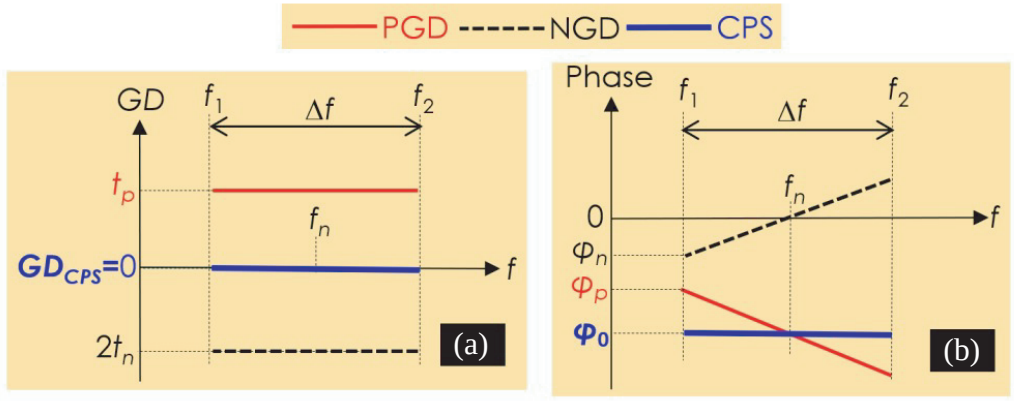

Figure 3. (a) GD and (b) phaseresponses of PGD, NGD, and CPS ideal topologies.

We remark from Fig. 3(b) that the PGD phase is plotted with negative slope, and the NGD phase is oppositely plotted in positive slope. By means of the analytical definition (3), the associated PGD and NGD phases can be modelled by:

$$\begin{cases} \varphi_{21,PGD}(f) = \varphi_{21,PGD}(f_1) - 2\pi f\, t_p = \varphi_p - 2\pi f\, t_p \\ \varphi_{21,NGD}(f) = \varphi_{21,NGD}(f_1) - 2\pi f\, t_n = \varphi_n - 2\pi f\, t_n \end{cases}. \tag{14}$$

Knowing condition (13), the overall topology proposed by Fig. 2 should present phase shift written by:

$$\varphi_{CPS}(f) = 2\varphi_{NGD} + \varphi_{PGD}. \tag{15}$$

Finally, the main goal of the study is achieved by expressing the CPS S-parameter model:

$$S_{21CPS}(jf) = a \cdot \exp(j\,\varphi_0) \tag{16}$$

with magnitude and phase given by:

$$\begin{cases} a = A_{NGD}^2 A_{PGD} \\ \varphi_0 = 2\varphi_n + \varphi_p \end{cases}. \tag{17}$$

To materialize the BP-NGD circuit-based CPS topological principle, a concrete circuit theory is introduced in the next section.

3. CIRCUIT THEORY ANALYSIS OF CPS

The circuit analysis of the proposed CPS is theoretically studied in the present section. The synthesis formulas of resistor, inductor, and capacitor components constituting the PGD and BP-NGD cells are established.

3.1. CPS Circuit Introduction

The design solution of the CPS consists in identifying the constituting real circuits able to generate the characteristics defined by the previous section. Fig. 4 depicts the adopted topology of CPS passive lumped circuit under study including the three basic constituting blocks. We can identify from this diagram the constituting blocks of the CPS.

The constituting lateral NGD topology is represented by the BP-NGD cell using an RLC-series resonant network. In the middle blocks, we have the PGD topology represented by the π-cell of a $C_pL_pC_p$-network. After the Z-matrix expression and Z-to-S matrix transform defined by Equation (2), we established the S-parameter models $[S_{PGD}(jf)]$ and $[S_{NGD}(jf)]$ of the PGD and NGD blocks,

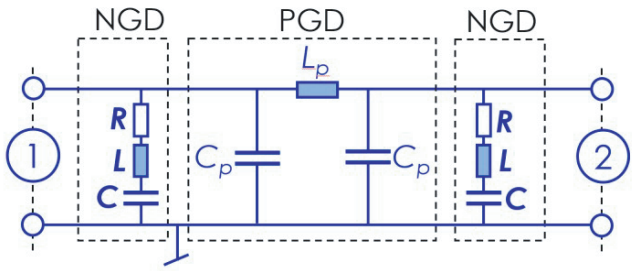

Figure 4. Lumped passive circuit of CPS topology.

respectively. Consequently, we analytically demonstrated the following S-matrix models:

$$[S_{PGD}(jf)] = \frac{\begin{bmatrix} Z_l(jf) - R_0^2 Y_c(jf)[2 + Z_l(jf)Y_c(jf)] & 2R_0 \\ 2R_0 & Z_l(jf) - R_0^2 Y_c(jf)[2 + Z_l(jf)Y_c(jf)] \end{bmatrix}}{D_{PGD}(jf)} \quad (18)$$

$$[S_{NGD}(jf)] = \frac{\begin{bmatrix} -R_0 & 2Z_{rlc}(jf) \\ 2Z_{rlc}(jf) & -R_0 \end{bmatrix}}{R_0 + 2Z_{rlc}(jf)} \quad (19)$$

where:

$$D_{PGD}(jf) = 2R_0 + Z_l(jf) + R_0 Y_c(jf)[\{R_0 + Z_l(jf)[2 + R_0 Y_c(jf)]\} \quad (20)$$

with the PGD and NGD impedance and admittance defined by:

$$\begin{cases} Z_l(jf) = j2\pi f L_p \\ Y_c(jf) = j2\pi f C_p \\ Z_{rlc}(jf) = R + j2\pi f L + \dfrac{1}{j2\pi f C} \end{cases}. \quad (21)$$

The design formulas of each components constituting the CPS circuit are derived from the S-parameter analysis. The established equations are described in the following paragraphs.

3.2. Design Formulas of the CPS PGD Circuit Components

The PGD phase shift was calculated from the transmission coefficient S_{21PGD}. We emphasize that the present CPS study is originally considering the non-trivial arbitrary chosen phase value $\varphi_0 \neq \{+/-90°, 180°\}$ different from the work done in [44]. The PGD cell is synthesized in function of the desired phase value $\varphi(f = f_n) = \varphi_0$ around the operation frequency f_n. which can be chosen as:

$$f_n = \frac{1}{2\pi\sqrt{2L_pC_p}}. \quad (22)$$

When $f = f_n$, we can analytically demonstrate the PGD phase:

$$\tan[\varphi_{PGD}(f_n)] = \frac{-(3R_0^2 + 16\pi^2 L_p^2 f_n^2)}{8\pi R_0 f_n L_p}. \quad (23)$$

The solution of equation $\tan[\varphi_{PGD}(f_n)] = \tan(\varphi_0)$ enables to express the expected values of PGD inductor. It yields the inductor value:

$$L_p = \frac{R_0[\tan(\varphi_0) + \sqrt{\tan^2(\varphi_0) - 3}]}{4\pi f_n}. \quad (24)$$

By using Equation (22), we can extract the PGD capacitor value:

$$C_p = \frac{1}{8\pi^2 f_n^2 L_p}. \quad (25)$$

The theoretical approach to determine the design formulas of NGD circuit constituting the CPS is described in the next subsection.

3.3. Design Formulas of the NGD Circuit Components Constituting the CPS

different from the PDG previous analysis, the NGD circuit design is established from the parameters at the NGD center frequency:

$$f_n = \frac{1}{2\pi\sqrt{L\,C}}. \tag{26}$$

The reflection coefficient $S_{11NGD}(f_n)$ and especially the GD $GD_{NGD}(f_n)$ are the essential NGD circuit parameters to be exploited to determine the design formulas. The NGD component design equations are established from the access matching $S_{11NGD}(f_n) < B$ and GD Equation (13) at the work frequency. Based on the RLC-series network-based BP-NGD theory, it implies the design equation system:

$$\begin{cases} S_{11NGD}(f_n) = B \\ GD_{NGD}(f_n) = -t_p \end{cases}. \tag{27}$$

We remind that the PGD GD $GD_{PGD}(f_n) = t_p$ derived from S_{21PGD} is given by:

$$t_p = \frac{4R_0L_p(7R_0^2 + 48\pi^2L_p^2f_n^2)}{9R_0^4 + 256\pi^4L_p^4f_n^4 + 160\pi^2R_0^2L_p^2f_n^2}. \tag{28}$$

The NGD cell resistor and inductor values are the solutions of equation system (27). It implies subsequently the following design formulas respectively:

$$R = \frac{R_0(1+B)}{2B} \tag{29}$$

$$L = \frac{R_0t_p(1+B)}{4B^2}. \tag{30}$$

By inverting Equation (26), we have the capacitor value:

$$C = \frac{1}{4\pi^2f_n^2L}. \tag{31}$$

After elaboration of the theoretical concept, it would be important to have a design guide. Knowing the component design formulas, the CPS design methodology is presented in the following subsection.

3.4. Design Methodology of CPS IC Designed inBi-CMOS Technology

The design method of the lumped passive CPS IC can be performed by the following four principal phases containing different technical steps:

- PHASE I: Specifications and ideal analysis
  - Step 1: Targeted specifications working frequency f_n, phase value φ_0 and access matching B of PGD and NGD cells
  - Step 2: Calculations of components L_p, C_p, R, L and C from analytical formulas (24), (25), (29), (30) and (31), respectively
  - Step 3: Schematic design and S-parameter simulations with CPS POC constituted by ideal lumped components
- PHASE II: Ideal result analysis
  - Step 4: MATLAB® calculation of CPS lumped circuit S-parameter model
  - Step 5: Commercial tool S-parameter simulation of CPS lumped circuit
  - Step 6: Analysis and comparison of phases and S-parameters from CPS IC schematic and model
- PHASE III: Bi-CMOS IC design
  - Step 7: Identification of equivalent R, L and C components constituting the CPS IC susceptible to be designed in 130-nm Bi-CMOS technology
  - Step 8: Schematic design of CPS IC in Bi-CMOS technology with respect to the constraints of component nominal values

- PHASE IV: Verification results
  - Step 9: Optimization with respect to the layout imperfection
  - Step 10: Layout versus schematic (LVS) from the CPS layout design
  - Step 11: Design rule checking (DRC) result analyses
  - Step 12: Post-layout simulation (PLS) and CPS IC validation result with respect to the expected specifications given in Step 1
  - Step 13: Robustness assessment with MC statistical method applied to the IC parameter variations

The validity of the CPS IC design methodology is verified by POC design feasibility examined in the following section.

4. DESIGN FEASIBILITY VERIFICATION RESULTS OF CPS IC IN 130-nm BI-CMOS TECHNOLOGY

The present section is focused on the validation results of the previously introduced CPS theory using BP-NGD topology. To do this, the design schematics and layout of the classical and Bi-CMOS CPS lumped circuits are described. Then, the verification results referring on the comparison of analytical calculations and two different commercial tools will be discussed.

4.1. Description of CPS POC Design

The design approach of the CPS is based on the S-parameter goals similar to all RF and microwave circuits. By reminding that different from [44], the present CPS works with an arbitrarily chosen non-trivial phase shift φ_0 around the operation frequency f_n. The present design is performed from the different networks constituting the CPS lumped circuit. Fig. 5 displays the considered schematics of the simulated circuits assumed as the first and ideal POC with ADS® commercial tool from Keysight Technologies®. These POCs of PGD, NGD, and CPS lumped circuits are designed in the environment of RF and microwave electronic circuit ADS® simulator. The CPS POC S-parameter simulation is performed from $f_{\min} = 0.7\,\text{GHz}$ to $f_{\max} = 1\,\text{GHz}$.

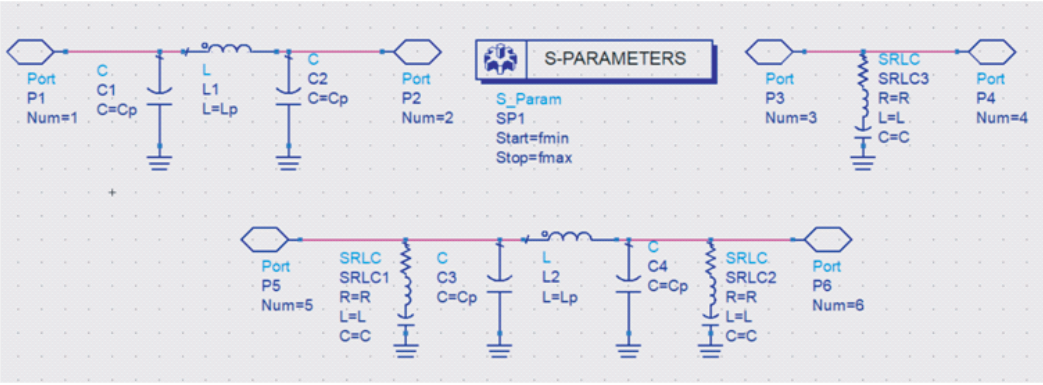

Figure 5. ADS® schematic design of PGD, NGD and CPS POCs.

The used designer is an electronic simulation environment of commercial tool familiar to microwave engineers. The proposed CPS POC is designed following the methodology developed by previous Subsections 3–4. The targeted and considered specifications are presented by Table 1.

Starting from the specifications indicated by Table 1, the POC resistor, inductor, and capacitor components were calculated and optimized. Therefore, we obtain the component values of PGD and NGD networks constituting the CPS POC indicated by Table 2.

In addition to the ideal lumped circuit design, the design of the second CPS POC more challengingly designed as an IC implemented in 130-nm Bi-CMOS technology is described in the following subsection.

Table 1. Targeted specifications during the CPS POC.

Circuit	Description	Parameters	Desired specifications
CPS	Work frequency	f_n	850 MHz
	Phase shift	φ_0	$-67°$
	Transmission coefficient	S_{21}	> -6 dB
NGD and PGD	Reflection coefficients	$S_{11} = S_{22}$	< -20 dB

Table 2. Component values of design CPS constituting blocks.

Block	Description	Name	Value
PGD	Inductor	L_p	7.6 nH
	Capacitor	C_p	2.33 pF
NGD	Resistor	R	77 Ω
	Inductor	L	25.8 nH
	Capacitor	C	1.04 pF

4.2. Description CPS IC as POC Designed 130-nm Bi-CMOS Technology

Another very expanded and popular commercial tool for miniature electronic circuit design engineering is used for the second POC of CPS. The schematic of the simulated IC CPS is highlighted by Fig. 6. As aforementioned in the introduction, the proposed CPS IC is designed in 130-nm Bi-CMOS technology. The second POC is designed in the Cadence VIRTUOSO® schematic environment commercial tool from Orcad®. The implemented Bi-CMOS resistor, inductor and capacitor components were chosen by taking into account the layout imperfection. The 130-nm BiCMOSunsalicidedN+active resistor referenced by name rpo1b was used for the NGD network. The inductor components are implemented by metal spiral coils using 130-nm BiCMOS symmetrical high current inductor referenced by name

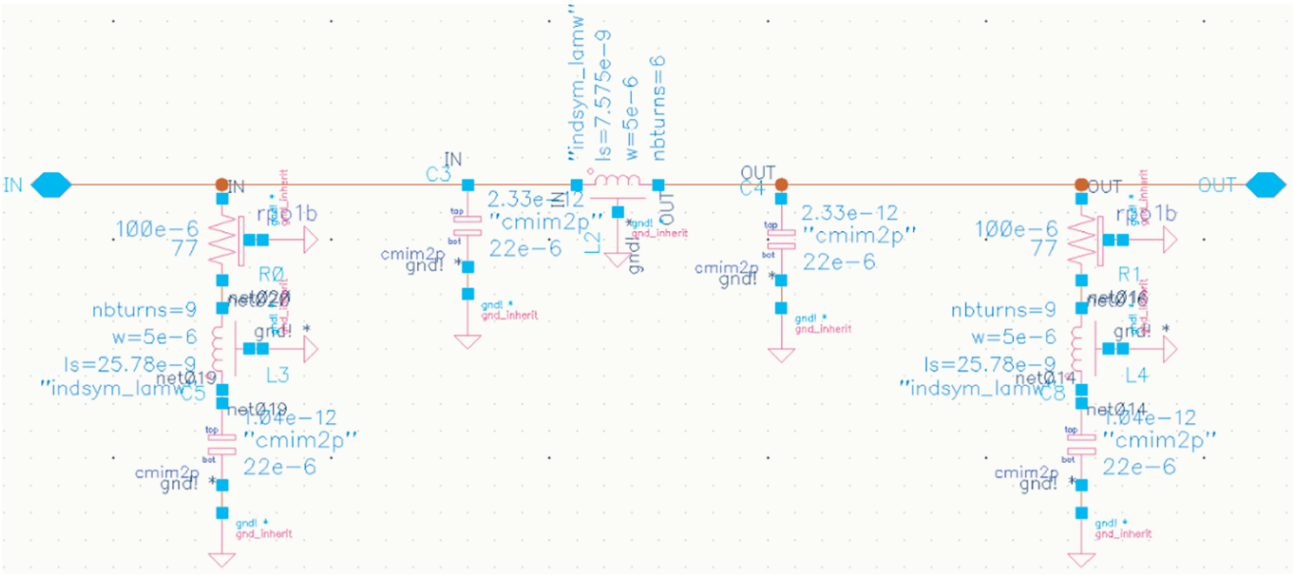

Figure 6. Schematic design of CPS IC in the Cadence VIRTUOSO® environment.

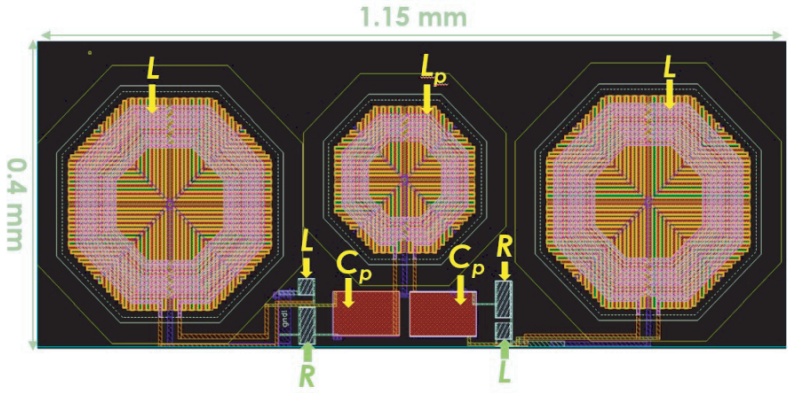

Figure 7. Layout design of miniature CPS ICin the Cadence VIRTUOSO® environment.

indsym_lamw. The capacitors were designed in metal-insulator-metal technology. The Cadence VIRTUOSO® layout design of the third POC representing a miniature circuit of the simulated CPS is highlighted by Fig. 7. The designed layout of the miniature PS has 1.15 mm × 0.7 mm physical size or 0.805 mm^2 surface. It is noteworthy that the inductors are the most cumbersome components constituting more than 90% of the layout surface.

After the DRC of the introduced layout, the CPS IS design feasibility based on the results of LVS is discussed in the next section.

4.3. Comparison of Computed and Simulated Results of the CPS IC Designed in 130-nm Bi-CMOS Technology

To verify the validity of the CPS IC design feasibility, the comparison between analytical calculation and numeric simulations is carried out. The present subsection discusses the S-parameter simulation results from MATLAB® calculated model, ADS® and Cadence VIRTUOSO® layout simulations. The frequency band of the result analysis presented in this paper is delimited by $f_{\min} = 0.7$ GHz and $f_{\max} = 1$ GHz.

4.3.1. PGD and NGD Responses

Figure 8(a) plots the comparisons of phase responses of PGD and NGD circuits from MATLAB® computation and simulation. It can be pointed out that the computed model and simulation are in very good correlation. The PGD phase shift model (plotted in solid black curve) compared to the simulated one (plotted in cyan circle curve) presents a phase shift of about $\varphi_{PGD}(f_0) = -67°$ for $f_0 = 850$ MHz. However, the computed (plotted in red dashed curve) and simulated (plotted in blue circle curve) NGD phase responses present values $\varphi_{NGD}(f_0) = 0°$. It can be underlined that the obtained responses are well-correlated to the expected ideal ones depicted by Fig. 3.

The associated GDs displayed by Fig. 8(b) show the complementarity in particular at the working frequency f_0 with $t_p = GD_{PGD}(f_0) \approx 0.224$ ns. Fig. 9(a) displays the NGD and PGD reflection coefficients from computation and simulation. As expected in the specifications of Table 1, the NGD and PGD are well matched with $S_{11\,\max}$ better than −10 dB. Then, Fig. 9(b) represents the NGD and PGD transmission coefficients. The PGD insertion loss $S_{21NGD} > -0.01$ dB can be neglected, while the NGD insertion loss is better than $S_{21NGD} > -3$ dB.

The verification results of the CPS design feasibility are more obviously understood from the examination of its phase shift and S-parameters as explored in the following paragraph.

*4.3.2. **S**-Parameter and Phase Shift Responses of the Developed CPS*

The present paragraph is dedicated to the confirmation of the design feasibility of the ideal schematic of Fig. 5 and IC layout of Fig. 7 designed in 130-nm Bi-CMOS technology. The verification results are based on the comparison of computed S-parameters from models expressed by Equation (18) and

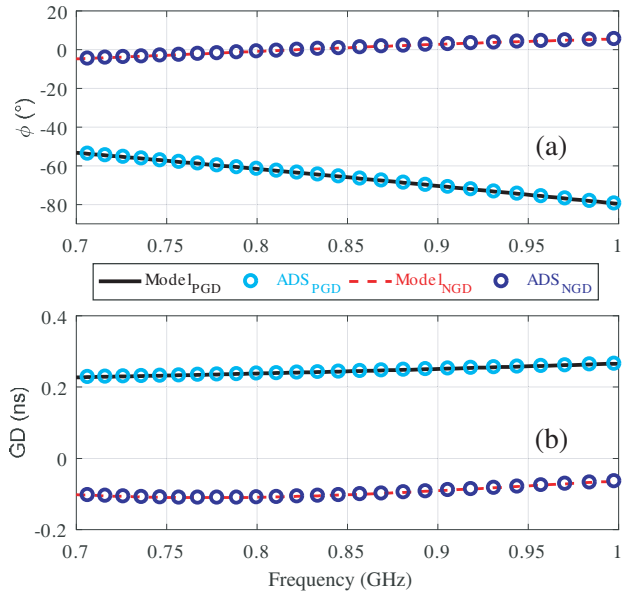

Figure 8. Comparison of PGD and NGD (a) phase, and (b) GD from modelling and ADS® simulation.

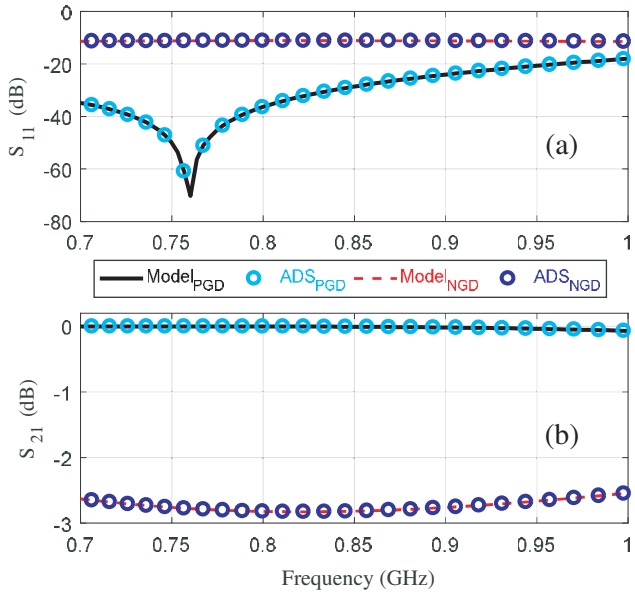

Figure 9. Comparison of PGD and NGD (a) S_{11} and (b) S_{21} from modelling and ADS® simulation.

Equation (19) and the simulations from commercial tools. The MATLAB® computed (plotted in solid black curve), ADS® (plotted in blue cyan curve) and Cadence VIRTUOSO® (plotted in dashed red curve) simulated results of CPS S_{11} and S_{21} are displayed by Fig. 10(a) and Fig. 10(b), respectively.

The designed CPS IC is well matched from $f_{\min}$ to $f_{\max}$. However, the Cadence VIRTUOSO® simulated S_{21} plotted by Fig. 10(b) presents slight differences from the ideal circuit of about 1.2 dB. More importantly, the comparison of CPS ideal circuit and IC phase responses is shown by Fig. 11(a). The computed and simulated results confirm that the constant and frequency independent behaviors around $f_0 = 0.85$ GHz are in good agreement. The obtained results reveal phase shift flatness $\varphi_{0ADS}(f_1 < f < f_2) = -67° +/- 0.25\%$ from MATLAB calculation of models against $\varphi_{0Cadence}(f_1 < f < f_2) = -67° +/- 1\%$ from Cadence VIRTUOSO® simulation within the frequency band $[f_1, f_2]$ with $f_1 = 730$ MHz and $f_2 = 984$ MHz. The associated GDs of the CPS IC which state variations lower than $\Delta GD_{ADS}(f_1 < f < f_2) = 50$ ps based on the results from MATLAB calculation and $\Delta GD_{Cadence}(f_1 < f < f_2) = 0.1$ ns based on Cadence VIRTUOSO® simulation results are sketched by Fig. 11(b). Table 3 describes the specifications of the compared CPS ideal circuit and IC. The flatnesses of the phase and transmission coefficient of the simulated CPS IC are assessed. It can be stated that around the working frequency, the CPS IC can be characterized by the relation $S_{21CPS}(jf) = a*\exp(j*\varphi_0)$ which does not depend on frequency f with insertion loss $a = 0.56 +/- 2.5\%$ and constant phase shift $\varphi_0 = -67° +/- 1\%$.

The robustness of CPS IC design in 130-nm Bi-CMOS technology is highlighted by the MC sensitivity analysis of the following section.

5. DISCUSSION ON THE CPS IC LAYOUT SENSITIVITY ANALYSES WITH RESPECT TO THE GEOMETRICAL PARAMETER VARIATIONS

The imperfection of IC layout designed in 130-nm Bi-CMOS technology with respect to the geometrical parameters is an important point for the CPS performance by varying the physical sizes. The present section studies the MC analyses of phase shift, and insertion and reflection losses with $n = 1000$ trials. Physical parameters are statistically varied in Gaussian law with $+/-5\%$ standard deviations.

Table 3. Specifications of calculated and simulated CPS.

Parameters	Calculated	ADS®	Cadence®
f_1	0.730 GHz		
f_2	0.984 GHz		
$\Delta f/f_n$	30%		
$\varphi(f_n)$	$-67°$	$-67.05°$	$-67.2°$
$\Delta\varphi$	$+/-0.25°$	$+/-0.25°$	$+/-1°$
$S_{11}(f_n)$	-13.8 dB	-13.7 dB	-13.98 dB
$S_{21}(f_n)$	-6.28 dB	-6.285 dB	-5.07 dB
ΔS_{21}	1 dB	1.04 dB	0.73 dB

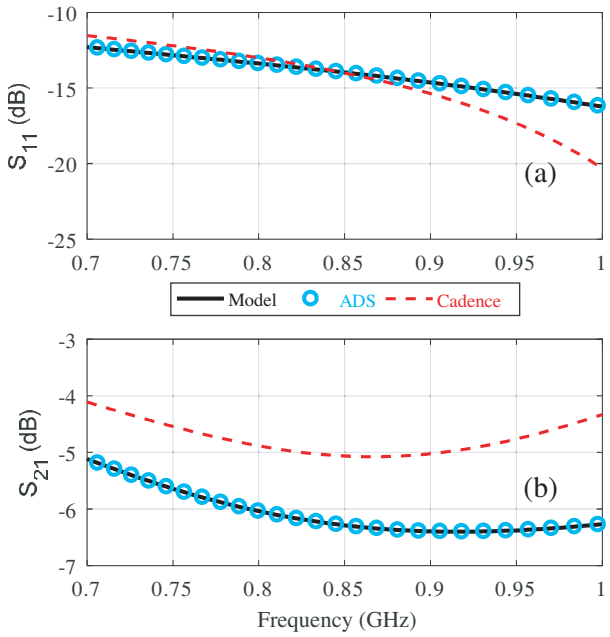

Figure 10. Comparison of CPS (a) S_{11} and (b) S_{21} from modelling, and ADS® and Cadence VIRTUOSO® simulations.

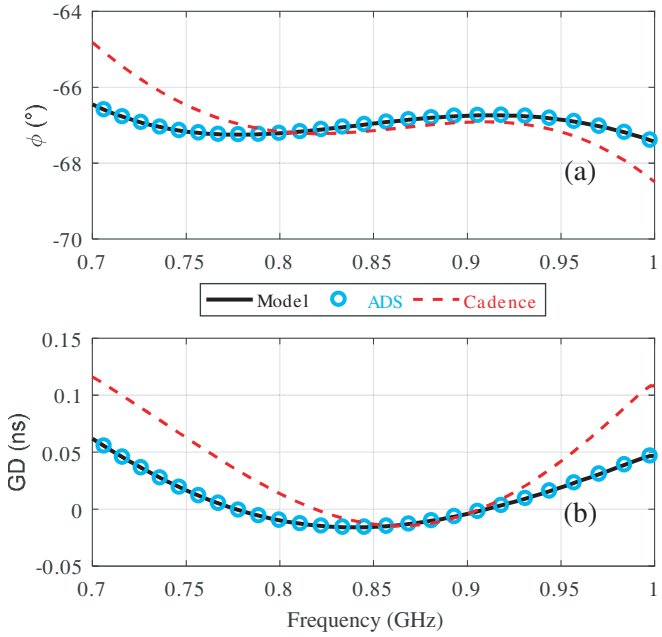

Figure 11. Comparison of CPS (a) phase and (b) GD from modelling, and ADS® and Cadence VIRTUOSO® simulation.

5.1. Ranges of Component Physical Parameters Used to Design the 130-nm Bi-CMOS CPS IC

Because of realistic physical constraints, the IC layout designed in the Cadence VIRTUOSO® environment may be sensitive to the physical real effect. The length, width, and radius of implemented components in 130-nm Bi-CMOS technology are the most sensitive geometrical parameters which are the essential aspects. For the considered design, we summarized the minimum and maximum values of resistors and inductors. Table 4 indicates the minimum and maximum values of unsalicidedN+activeresistor which are equal to $R_{\min} = 4\,\Omega$ and $R_{\max} = 13\,\text{k}\Omega$.

The sensitive component susceptible to influence significantly the CPS IC specifications is the symmetrical high current spiral inductor. The minimum and maximum values of 130-nm Bi-CMOS inductor which are $L_{\min} = 3.8$ nH and $L_{\max} = 25.8$ nH are summarized by Table 5.

Table 4. Ranges of geometrical and electrical parameters of the 130-nm Bi-CMOS resistors implemented in the CPS IC layout.

Description	Parameter	Min	Max
Width	w	1 µm	100 µm
Length	d	3 µm	100 µm
Resistor	R	4 Ω	13 kΩ

Table 5. Ranges of geometrical and electrical parameters of the 130-nm Bi-CMOS inductors used in CPS IC layout.

Description	Parameter	Min	Max
Width	w	5 µm	12 µm
Diameter	ϕ	53 µm	163 µm
Number of turns	N	2	9
Inductor value	L	3.8 nH	25.8 nH
Si area	S	0.0144 mm^2	0.0961 mm^2
Resonance frequency	f_r	3.33 GHz	91.4 GHz

To materialize the effectiveness of the proposed CPS IC layout design, the MC analysis results which highlight the worst-cases of the parameters are discussed in the following subsections.

5.2. Phase Shift MC Analysis

The MC analysis results analyzing the phase shift $\varphi_{CPS}(f_n) = \varphi_0$ of the CPS IC layout were performed with $n = 1000$ runs. The histogram of phase shift is plotted by Fig. 12. The phase mean value around the working frequency f_0 is $\varphi_0 = -67.0681°$ with standard deviation $\sigma(\varphi_0) = 0.382°$. After the carried-out MC trials, the variation of phase shift φ_0 with multiple of absolute error evolves behaving as asymmetric configuration with sample lower than 0.1% for $\Delta\varphi_0 < 1°$.

5.3. MC Analysis of CPS IC Transmission Coefficient

In addition to the phase shift, the worst case of transmission coefficient is analyzed in this paragraph with $n = 1000$ runs. The MC analysis results analyzing the minimum of transmission coefficient $S_{21\,\text{min}}$ of the CPS IC layout in the frequency band $[f_{\text{min}}, f_{\text{max}}]$ were performed. The histogram of the minimal transmission coefficient is shown by Fig. 13.

The assessed mean value is mean $(S_{21\,\text{min}}) = -4.862\,\text{dB}$ with standard deviation $\sigma(S_{21\,\text{min}}) = 0.08$. During the MC run trials, the CPS IC minimal transmission coefficient having values with multiple of standard deviation $3\sigma(S_{21\,\text{min}})$ has samples lower than 5.

5.4. Maximal Reflection Loss MC Analysis

Another S-parameter worst-case analysis of CPS IC reflection coefficient with $n = 1000$ trials is also examined in this paragraph. The MC analysis results analyzing the maximum of reflection coefficient $S_{11\,\text{max}}$ of the CPS IC layout in the frequency band $[f_{\text{min}}, f_{\text{max}}]$ were obtained. The histogram plot of the CPS IC minimal transmission coefficient is depicted by Fig. 14.

The assessed mean value is mean $(S_{11\,\text{max}}) = -10.17\,\text{dB}$ which is lower than $-10\,\text{dB}$ with standard deviation $\sigma(S_{11\,\text{max}}) = 0.256$. Based on the present statistical analysis, the CPS IC minimal transmission coefficient having values with multiple of standard deviation $3\sigma(S_{11\,\text{max}})$ has lower than 5 samples or 0.5% of total trials.

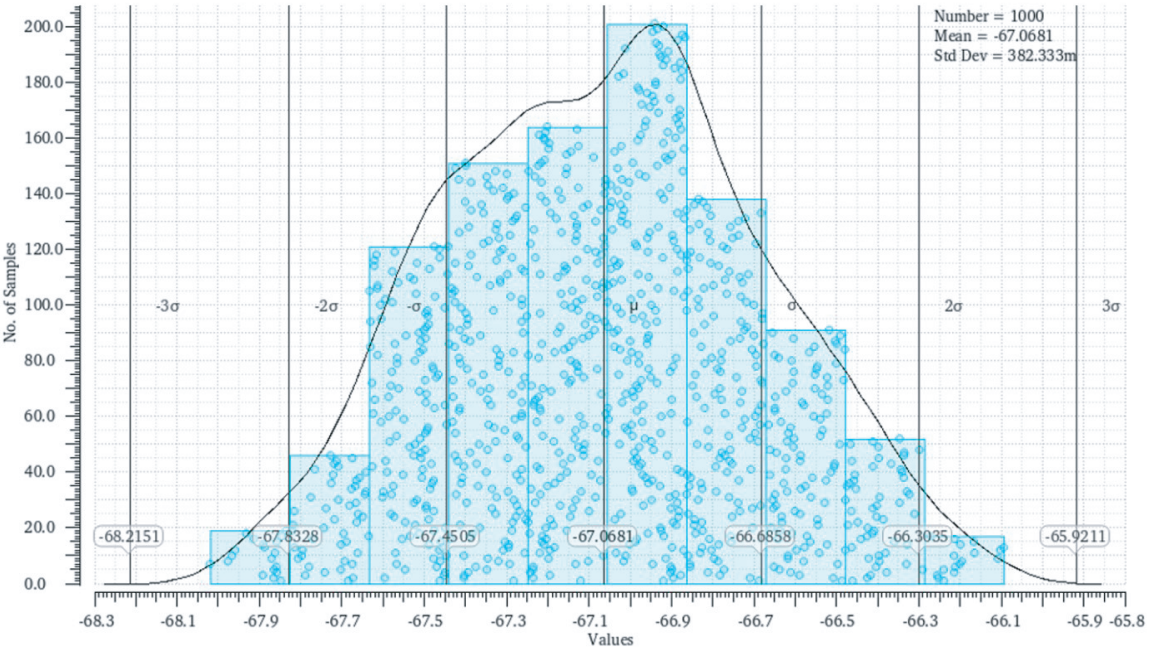

Figure 12. Histogram of CPS IC layout φ_0 from MC analysis.

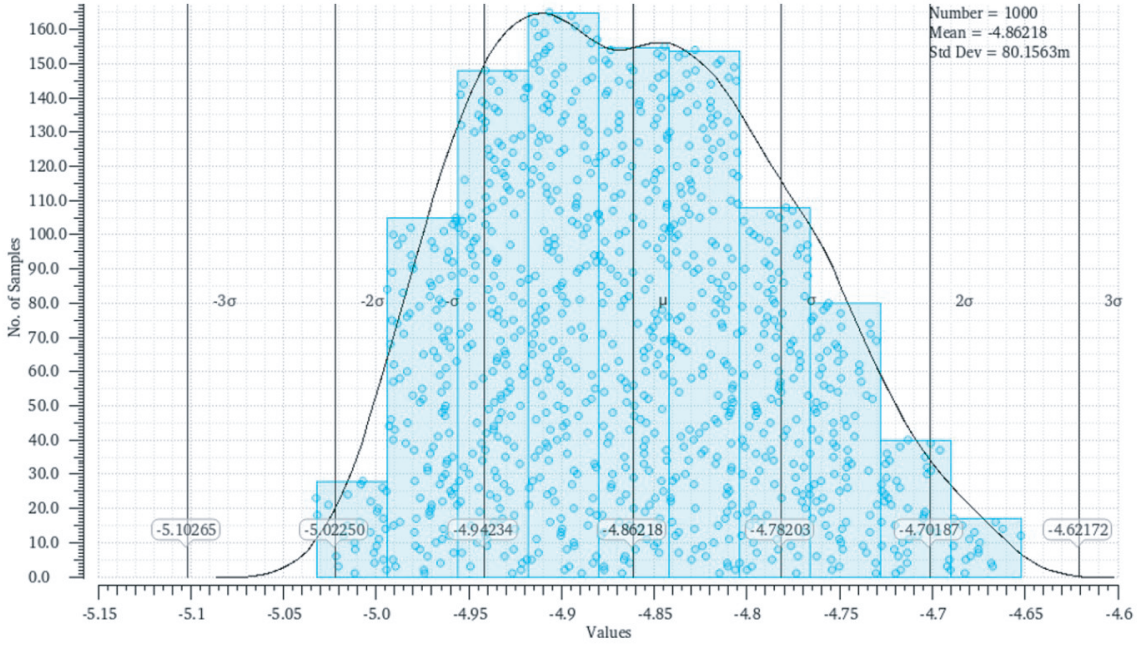

Figure 13. Histogram of CPS IC layoutmean (S_{21}) responses from MC analysis.

5.5. MC Sensitivity Analysis of the CPS IC with Respect to 10% Standard Deviation of Inductors and Capacitors

In addition to the previous MC analyses in the frequency range, one may wonder about the BP-NGD CPS sensitivity with respect to the reactive components. As an answer to such a curiosity, statistical based sensitivity of the BP-NGD CPS from S-parameter simulation with respect to the

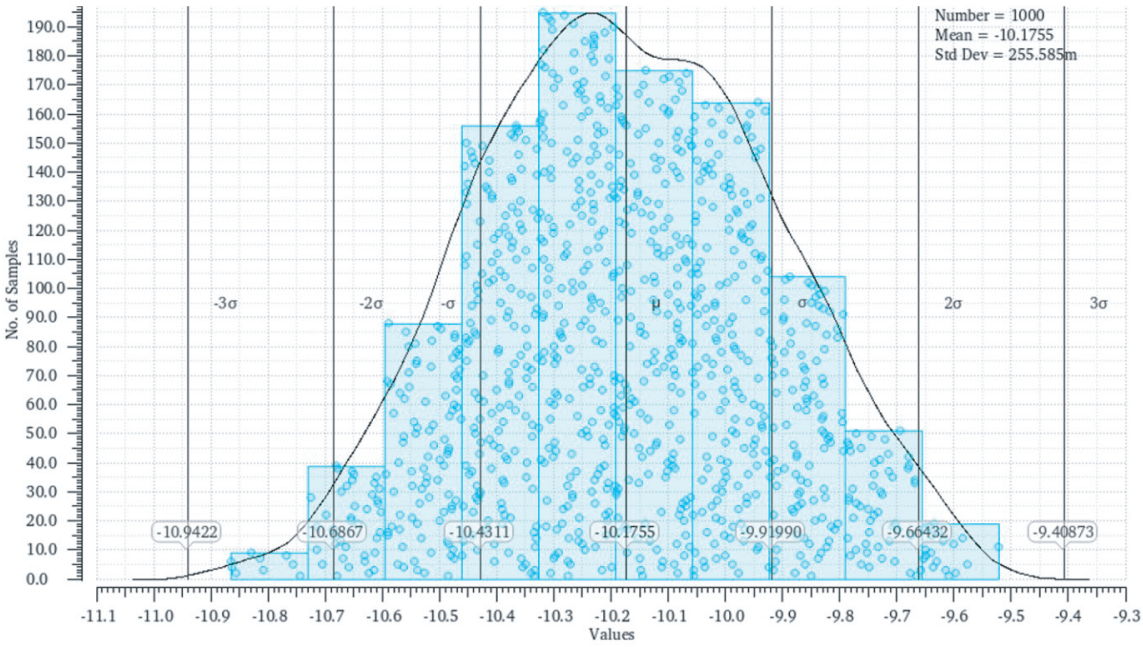

Figure 14. Histogram of CPS IC layout $S_{11\,\max}$ from MC analysis.

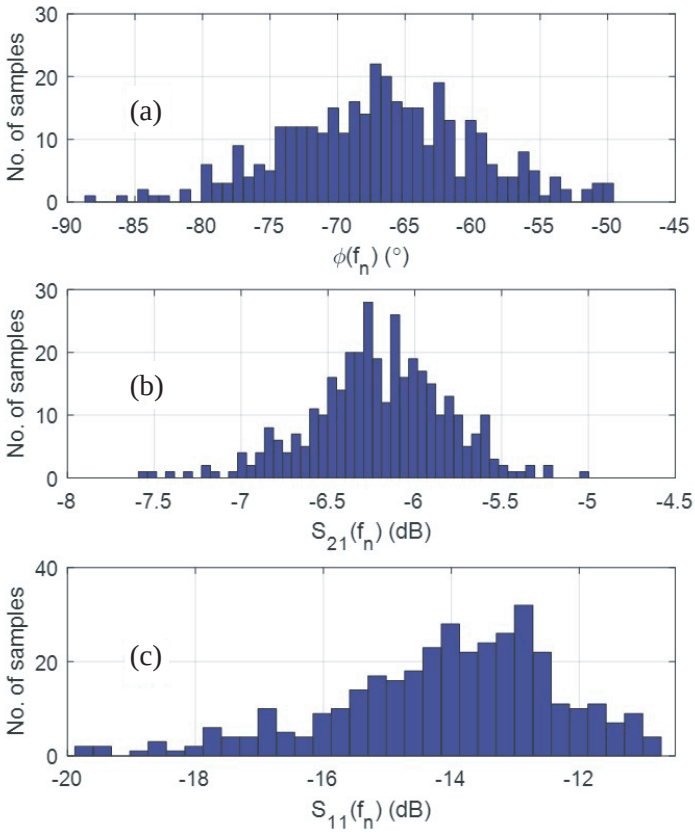

Figure 15. Histograms of (a) φ_0, (b) $S_{21}(f_n)$ and (c) $S_{11}(f_n)$ with respect to 10% standard deviations of reactive components.

reactive components L_p, C_p, L, and C was carried out. The single frequency ($f = f_n$) MC analyses over 1000 trials were performed. Therefore, we have histograms of the simulated phase shift, transmission and reflection coefficients at the operating frequencies $f = f_n$ plotted in Fig. 15(a), Fig. 15(b), and Fig. 15(c).

The assessed performances from statistical analyses of the results in terms of mean values and standard deviations are addressed in Table 6. We can see that the phase shift variation remains lower than $+/-6.92°$, and the IC CPS remains well matched.

Table 6. BP-NGD CPS performances of 10% standard deviation MC analyses applied to reactive components.

Parameter	φ_0	$S_{21}(f_n)$	$S_{11}(f_n)$
Average value	$-66.92°$	$-6.2\,\mathrm{dB}$	$-14.11\,\mathrm{dB}$
Standard deviation	$6.92°$	$0.34\,\mathrm{dB}$	$1.84\,\mathrm{dB}$

6. CONCLUDING REMARK

An innovative investigation on microwave miniature CPS by using BP-NGD circuit is developed. The originality of the study lies on the consideration of non-trivial arbitrary value of phase shift and also the IC implementation in 130-nm Bi-CMOS technology. The theoretical approach of BP-NGD CPS is elaborated from S-parameter modelling. The design formulas of lumped components constituting the CPS are established. The 130-nm Bi-CMOS design of the proposed CPS is described. The feasibility study of the microwave CPS IC design in 130-nm Bi-CMOS technology is verified by comparing analytical model and commercial tool simulation results. The schematic and layout designs are described. The obtained computed and simulated results confirm the constant phase shift independent to the frequency. The CPS IC robustness is highlighted by the statistical analysis with respect to the Gaussian variation of the geometrical parameters. The sensitivity MC analyses with 1000 trials applied to the phase shift around the working frequency, S_{11} and S_{21} worst-cases enable to state the robustness of the CPS IC design in 130-nm Bi-CMOS technology. The proposed design is potentially useful for dealing with the millimeter wave THz [43], GD issue [45] and ultra-wide band improvement [46, 47] of RF/microwave transceiver of future 5G/6G communication system. In addition, further investigation on active CPS Bi-CMOS IC design will be developed in the future by challenging the phase-metric assessment as introduced in [48, 49].

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