A Miniaturized 3-Way Power Divider Based on Bagley Polygon

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Abstract—A three-way power divider based on Bagley polygon is here reduced in dimension by applying the concept of reducing delay line length by applying open circuit stubs. Whereas this technique is known in literature, the delay line reduction is done symmetrically by placing the stub mid-line, which would imply packing issues leading to a reduced size reduction. In this contribution a theoretical development on non-symmetric reduced length delay line is carried out, allowing for a more effective size reduction of the Bagley-based power divider. Measurements on a prototype designed at 2.45 GHz occupying less than half of the area of a canonical Bagley divider with comparable performances over a slightly reduced operational bandwidth prove the validity of the approach.

1. INTRODUCTION

Bagley power dividers are a feasible alternative to Wilkinson power dividers in those applications where output port matching and isolation is not an issue. Indeed, as it is well known, in the numbering scheme of a classical 3-way Bagley power divider (Fig. 1(a)), while port 1 is perfectly matched, ports 2 to 4 are not, and the isolation between them is far from being low [1]. This is opposed to the behavior of Wilkinson-class power dividers which exhibits good matching and isolation at all ports [2].
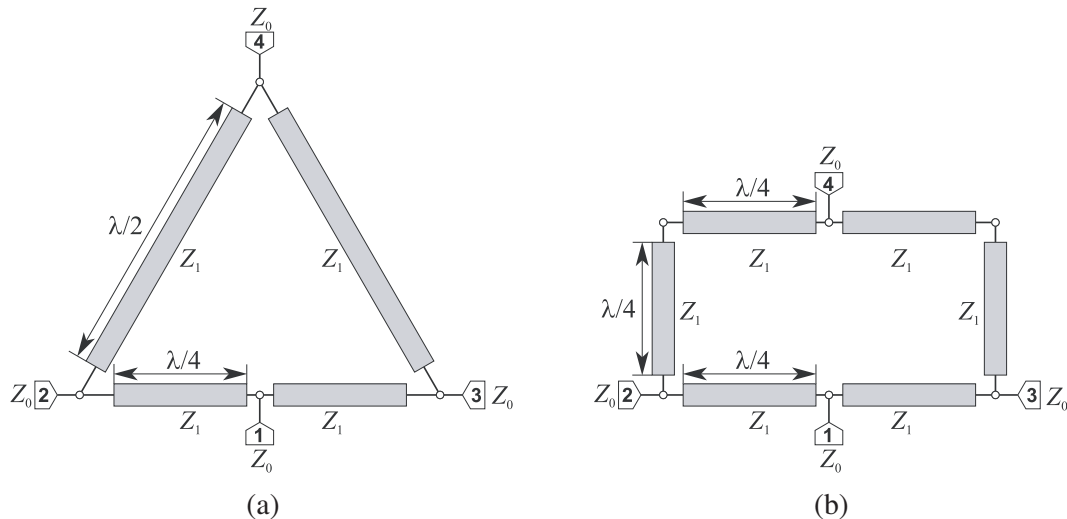

Figure 1. (a) The standard Bagley 3-way power divider and (b) its rectangular version which will be the starting point for our miniaturization.

Yet a Bagley power divider, if used as a one way dividers, with only port 1 fed and all the other closed on matched impedance so that no power enters ports 2 to 4, is a better choice with respect to a 3-way Wilkinson divider since it is fully planar and does not require soldering of any lumped resistances.

On the other hand, the canonical 3-way Bagley divider is in the shape of a triangle or a rectangle (Fig. 1). In any case, from a topological point of view, it is a ring of perimeter $3\lambda/2$ which occupies a non-negligible area on the printed circuit board [1]. In particular for the triangular shape its area is $0.108\lambda^2$ while the rectangular one, even with a better shape factor, occupies a larger area: $0.125\lambda^2$. Canonical 3-way Bagley power dividers have $Z_1 = 2Z_0/\sqrt{(3)}$. A 3-way Wilkinson divider occupies an area as little as that of a circle $\lambda/2$ in circumference [3], which corresponds to about $0.02\lambda^2$. The latter is hence much more convenient in terms of space occupation.

There are a few papers in literature dealing with miniaturized Bagley power dividers, resorting either to shorter lines between the outputs [4,5] with slightly narrower band than a conventional one, or to composite right/left handed transmission lines, which in turn requires lumped elements [6]. Interesting possibility is also that of uneven splitters, like those in [7] or multiband ones [8].

In this contribution, different from in [4,5], all lines in the Bagley polygon will be shortened applying the same technique applied in [3,9], which is via a midpoint reactive load realized with a stub, as opposed to the end-loading technique presented in [10,11].

To achieve higher degrees of compactness, stubs will be placed within the polygon. This is indeed not possible since stubs from opposite sides of the polygon would overlap. To overcame this either bent stubs must be used, as in [9] or an off-center placement of the stub, with an offset with respect to midpoint, is exploited. In this paper the latter method will be applied.

Although the technique is applied to a three-way Bagley divider with equal outputs, it can be extended to unequal Bagley power dividers like the one presented in [7,12].

The paper is hence organized as follows. Section 2 develops the theory for shortened delay lines with off-center reactive load. Section 3 will present two designs, one with centered and one with off-center reactive load, the latter with higher compactness. Section 4 will present the characterization of the built prototypes, and finally, Section 5 will draw the conclusions.

2. OFF-CENTER LOADED SHORTENED DELAY LINE

Figure 2 shows the basic idea behind the shortening of a delay line by resorting to a shunt reactive load, which in turn is realized via a stub. The shunt load is here placed at an arbitrary distance from one of the two ends of the line. In detail, with θ_0 being the electrical length of the standard delay line, we search for a delay line comprising two sections, respectively, of electrical length θ_1 and θ_2 such that $\theta_1 + \theta_2 < \theta_0$, with Z_1, Z_2, and B to be determined so that, at the design frequency f_0, matching and phase delay are equal for the two structures.
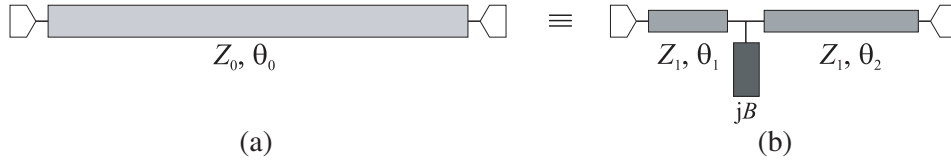

Figure 2. (a) A standard delay line and (b) an equivalent, shorter, delay line with a reactive load connected at an arbitrary position.

In a chain matrix C representation, the delay line on the left in Figure 2 is that of a line of electrical length θ_0 and characteristic impedance Z_0, that is:

$$C_0 = \begin{bmatrix} \cos\theta_0 & jZ_0\sin\theta_0 \\ j\dfrac{1}{Z_0}\sin\theta_0 & \cos\theta_0 \end{bmatrix} \tag{1}$$

While the device on the right in Figure 2 is characterized by the cascade of two delay lines, the first of of electric length θ_1 and characteristic impedance Z_1; the second of electric length θ_2 and characteristic

impedance Z_2; and a concentrated shunt load jB, respectively:

$$C_1 = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ j\dfrac{1}{Z_1}\sin\theta_1 & \cos\theta_1 \end{bmatrix} \tag{2}$$

$$C_s = \begin{bmatrix} 1 & 0 \\ jB & 1 \end{bmatrix} \tag{3}$$

$$C_2 = \begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_1 \\ j\dfrac{1}{Z_2}\sin\theta_2 & \cos\theta_2 \end{bmatrix} \tag{4}$$

The complete device chain matrix is given by $C_d = C_1 C_s C_2$ and is:

$$C_d = \begin{bmatrix} \cos\theta_2\left[\cos\theta_1 - BZ_1\sin\theta_1\right] - \dfrac{Z_1}{Z_2}\sin\theta_1\sin\theta_2 & jZ_1\cos\theta_2\sin\theta_1 + jZ_2\sin\theta_2\left[\cos\theta_1 - BZ_1\sin\theta_1\right] \\ j\cos\theta_2\left[\dfrac{1}{Z_1}\sin\theta_1 + B\cos\theta_1\right] + \dfrac{j}{Z_2}\cos\theta_1\sin\theta_2 & \cos\theta_1\cos\theta_2 - Z_2\sin\theta_2\left[\dfrac{1}{Z_1}\sin\theta_1 + B\cos\theta_1\right] \end{bmatrix} \tag{5}$$

It is possible to enforce $C_0 = C_d$, and, having chosen the device electrical lengths θ_1 and θ_2 as design parameters, the result is:

$$\begin{cases} Z_1 = Z_0 \dfrac{\cos\theta_2 - \cos\theta_0\cos\theta_1}{\sin\theta_0\sin\theta_1} \\[2ex] Z_2 = Z_0 \dfrac{\cos\theta_1 - \cos\theta_0\cos\theta_2}{\sin\theta_0\sin\theta_2} \\[2ex] B = \dfrac{\sin\theta_0\left[\cos^2\theta_0 + \cos^2\theta_1 + \cos^2\theta_2 - 2\cos\theta_0\cos\theta_1\cos\theta_2 - 1\right]}{Z_0\left[\cos^2\theta_0\cos\theta_1\cos\theta_2 - \cos\theta_0\cos^2\theta_1 - \cos\theta_0\cos^2\theta_2 + \cos\theta_1\cos\theta_2\right]} \end{cases} \tag{6}$$

The device is hence an *equivalent delay line*.

Analyzing these equations as a function of the original, standard, delay line length θ_0 and of the desired equivalent delay line length θ_1 and θ_2 would be problematic inasmuch one would have three design parameters to sweep. To obtain some insight on the behavior of the formulas, Figure 3 assumes a $\theta_0 = 90°$ line of arbitrary characteristic impedance Z_0 and shows the normalized (to Z_0) values of Z_1, Z_2, and B as a function of the total shorter line length $\theta_1 + \theta_2$, which is let to vary from 0 to θ_0 and the relative length $\theta_1/(\theta_1 + \theta_2)$, which is the ratio between the length of the first line in the shortened device and its total length.

It is apparent from Figure 3 how the shorter the first line length θ_1 is, the higher its characteristic impedance becomes and that there is an evident symmetry in Z_2, its contour plot being identical to that of Z_1 but upside-down. Furthermore, a shortened line has always a higher characteristic impedance. This will lead to limitations to shortening due to the implementation in microstrip, whose width cannot shrink beyond production process limits, and hence whose impedance cannot be arbitrarily high. Said symmetry is even more evident on the B contour plot, which is apparently symmetrical with respect to its mid horizontal axis.

Figure 4 shows similar results but for a standard line $\theta_0 = 120°$. It can be seen that Z_1 and Z_2 assume similar value in the two cases if the percentage of reduction is comparable.

Then, Figure 5 shows, in this latter case, the normalized value of the $Z_1 Z_2$ product, this graph not only shows again the symmetry already present in the B graph but also proves us that a centrally placed shunt reactance would be the optima solution since both $Z_1 = Z_2$ are smaller for a given percentage of reduction, and also B is higher, which, in a microstrip realization with open ended stubs, means the shortest possible stub.

Nevertheless, as it will be shown in the following, off-center placement of the stub is at a premium when such stubs must be placed internally within a ring device.

For a deeper insight Figure 6 shows two cases, relative to the shortening of a delay line of electrical length 120° to 100° (marked prime, or $'$) and to 40° (marked prime, or $''$) designed at a working frequency
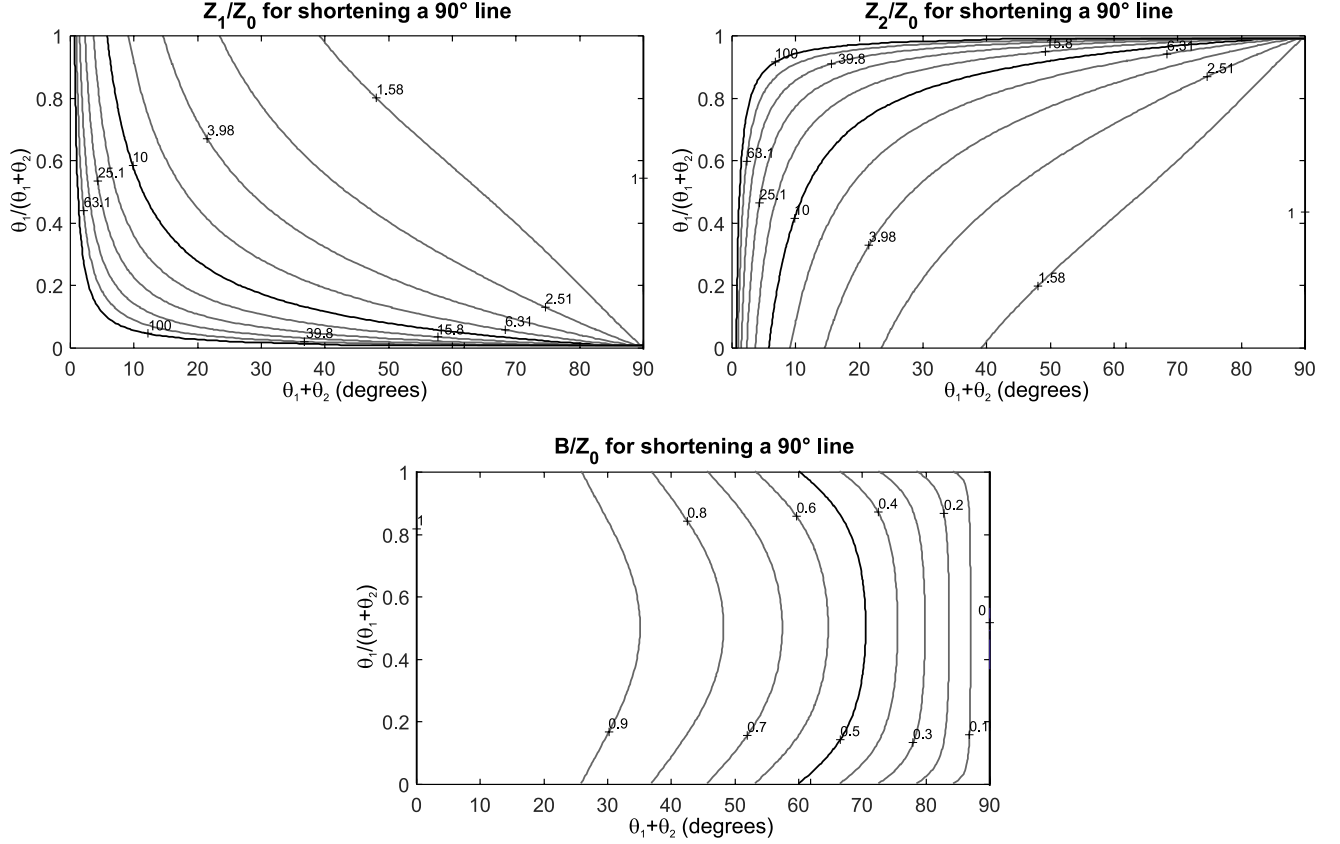
Figure 3. For a standard line $\theta_0 = 90°$ long, values of Z_1, Z_2 and B, normalized to Z_0 (from top to bottom) to attain a shortened line whose total electric length is $\theta_1 + \theta_2$ degrees (x-axis) and where the relative length $\theta_1/(\theta_1 + \theta_2)$ varies from 0 to 1 (y-axis).

of 3 GHz. It is apparent how the shorter line has a band at $|S_{11}| = -15\,\text{dB}$ from $f_1'' = 2.97\,\text{GHz}$ to $f_2'' = 3.16\,\text{GHz}$, whereas the longer line has an upper frequency limit $f_2' = 3.58\,\text{GHz}$ but no lower frequency. Since the analysis goes from $f_{\min} = 100\,\text{MHz}$ to $f_{\max} = 10\,\text{GHz}$, f_1' is effectively considered to be $f_{\min}$ for band computation. Similar considerations hold for the phase, where band is defined as the interval in which the phase delay ϕ_s of the shorter lines differs by at most 5° from the phase delay of the standard delay line ϕ_r. Figure 6 reports both ϕ_s and ϕ_r as well as their difference $\Delta\phi = \phi_r - \phi_s$. Also in this case, band limit f_1 can hit the lower frequency of analysis. It is also worth noticing that if $\theta_1 + \theta_2 \to \theta_0$ f_2 may hit the upper limit of 10 GHz.

Figure 7 reports the return loss band (at 15 dB) and the phase band (at $\pm 5°$) for the aforementioned 120° delay line for an arbitrary length reduction and as a function of the ratio $\theta_1/(\theta_1 + \theta_2)$. Band, shown with contour lines, is in both cases given as an absolute value $f_2 - f_1$ in GHz, with central frequency being $3GHz$. In Figure 7, hatched areas shows $f_1 < f_{\min}$ and $f_2 < f_{\max}$.

From Figure 7 it is apparent how the 5° band is always smaller than the $-15\,\text{dB}$ bandwidth and how the optimal choice stays the symmetric one, with the band being the largest for a given shortening.

3. COMPACT DIVIDER LAYOUT AND OPTIMIZATION

Figure 8 shows the schematic of the reduced size Bagley rectangular three way power divider with central stub placement (Layout A in the following). In this case, the six $\lambda/4$ long lines are all shrunk to $\lambda/8$ according to the theory in [9]. Each section hence exhibits two $\lambda/16$ (or 22.5°) long lines of characteristic impedance $Z_h = 120.7\,\Omega$. The central stub impedance Z_{sh} is fixed to $100\,\Omega$, and its electrical length is hence computed to be $\theta_{sh}58.9°$.
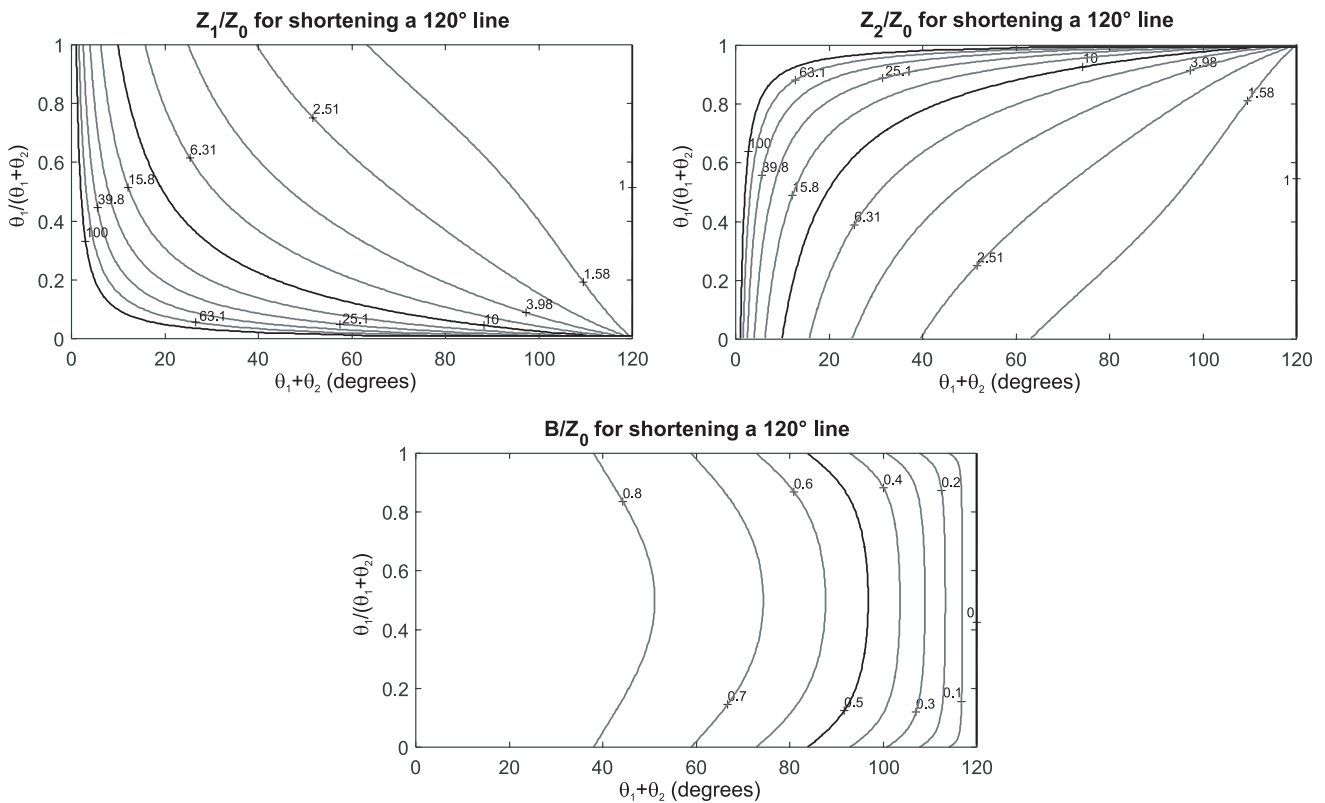
Figure 4. For a standard line $\theta_0 = 120°$ long, values of Z_1, Z_2 and B, normalized to Z_0 (from top to bottom) to attain a shortened line whose total electric length is $\theta_1 + \theta_2$ degrees (x-axis) and where the relative length $\theta_1/(\theta_1 + \theta_2)$ varies from 0 to 1 (y-axis).
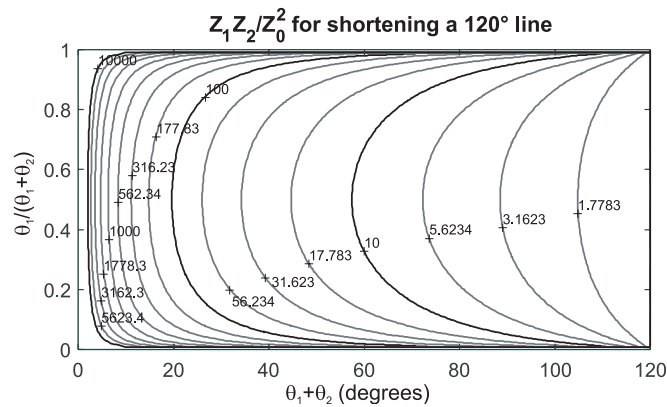
Figure 5. Normalized product $Z_1 Z_2$, for the shortening of a 120° line, showing how, for a given shortening, the lowest value for $Z_1 Z_2$ is for $\theta_1 = \theta_2$.

Figure 9, on the other hand, shows the schematic for the case in which vertical lines are shortened with an off-center stub to allow for positioning the stub inside the ring. Line lengths are still halved, which means that the horizontal lines are the same as in the previous case, while the vertical ones are shortened so as to split the desired total length $\lambda/8$ in a $1 : 2$ ratio, which is $\theta_{v2} = 2\theta_{v1}$. Theoretical formulas give $Z_{v1} = 167.3\,\Omega$ and $Z_{v2} = 96.6\,\Omega$. The $100\,\Omega$ stub length is $58.5°$.

Table 1 summarizes these dimensions. The first two rows in table is applied to both designs, and the last two rows describe the off-center shortening of the second design (Layout B in the following).

Please note that the stubs are nearly $60°$ or $\lambda/6$ long, hence $\theta_{sv} > \theta_h$, which is why it is essential to have $\theta_{v1} \neq \theta_{v2}$; otherwise, stubs would overlap in the final design.
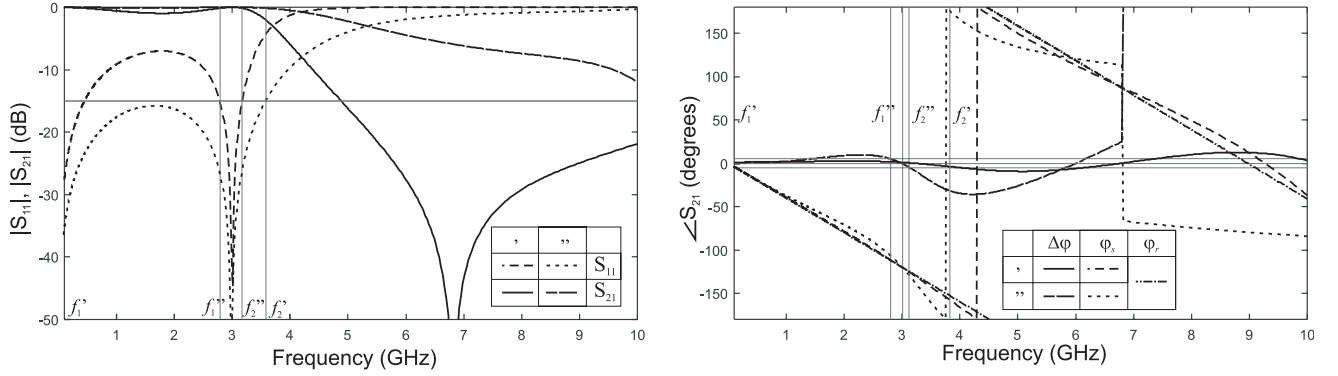

Figure 6. Two possible reduction for a $120°$ delay line, one shortened to $100°$ (prime, $'$) and one to $40°$ (second, $''$).
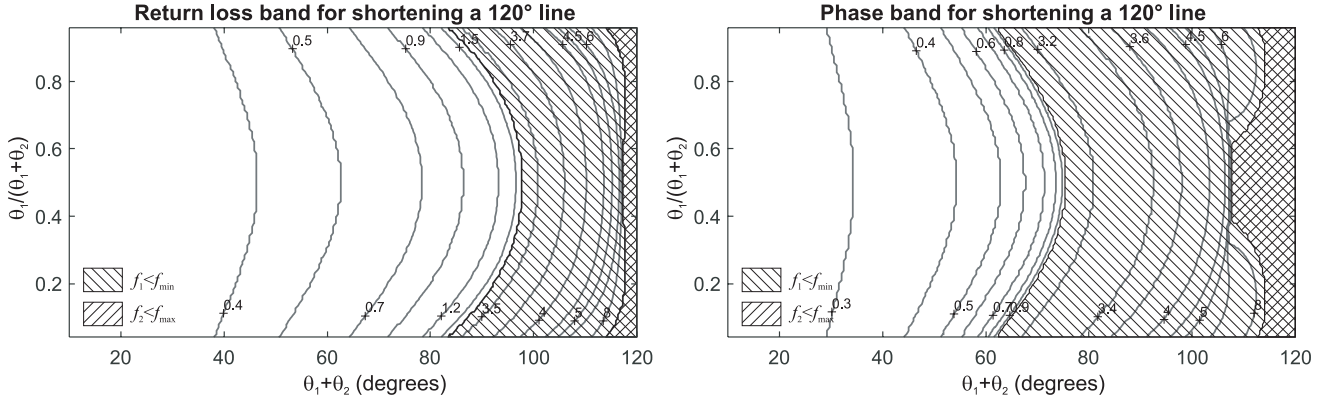

Figure 7. Normalized product $Z_1 Z_2$, for the shortening of a $120°$ line, showing how, for a given shortening, the lowest value for $Z_1 Z_2$ is for $\theta_1 = \theta_2$.
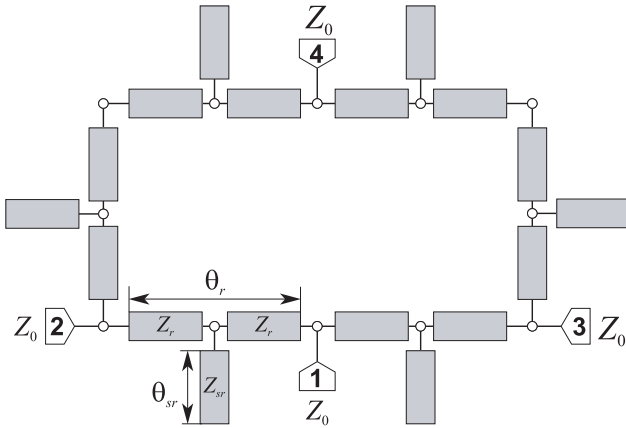

Figure 8. Geometry of the compact Bagley divider, for centered stub (case A). Blocks of the same shade of gray are identical.
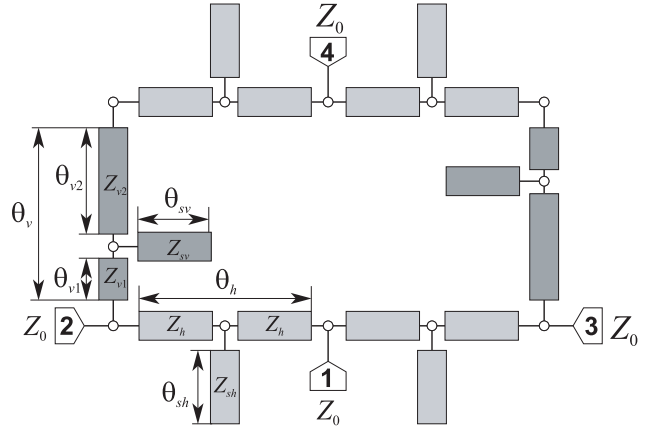
Figure 9. Geometry of the compact Bagley divider, for off-center stubs (case B). Blocks of the same shade of gray are identical. Darker ones are shortened asymmetrically to accommodate the stubs inside.
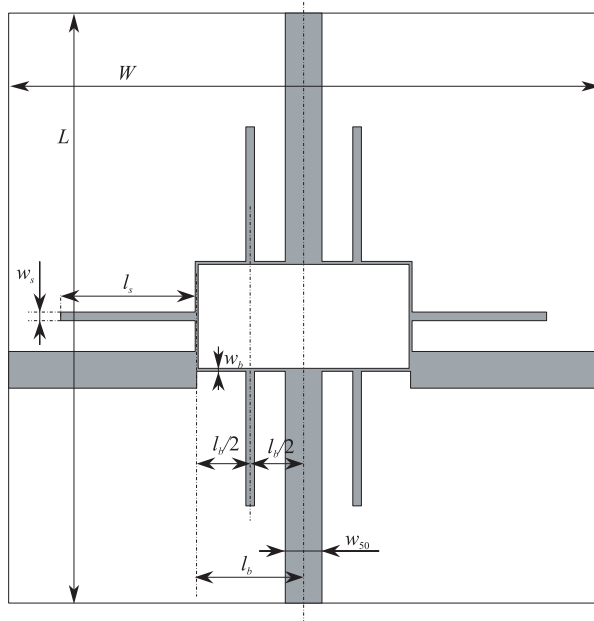
Figure 10. Microstrip realization of the reduced size Bagley divider, final A layout.
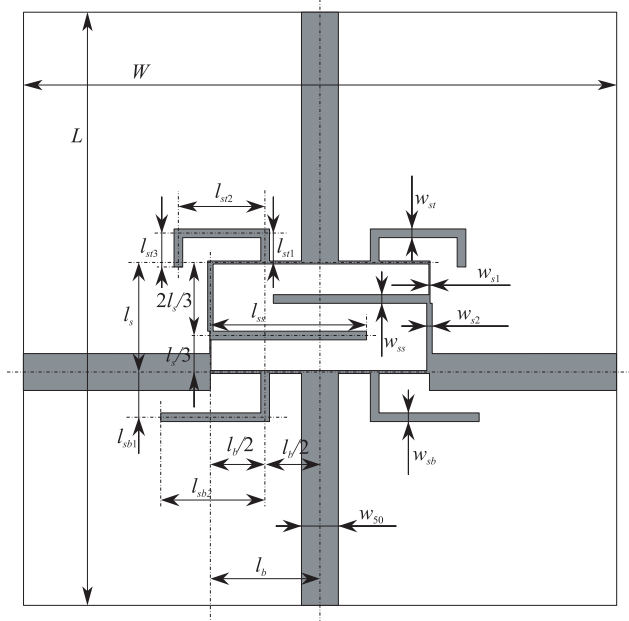
Figure 11. Microstrip realization of the reduced size Bagley divider, final B layout.

Table 1. Dimensions for the theoretical reduction.

θ_h	Z_h		θ_{sh}	Z_{sh}
22.5°	120.7 Ω		58.9°	100 Ω

θ_{v1}	θ_{v2}	Z_{v1}	Z_{v2}	θ_{sh}	Z_{sh}
15°	30°	167.3 Ω	96.6 Ω	58.5°	100 Ω

Table 2. Dimensions for the microstrip implementation, A layout (mm).

	W	L	w_{50}	
General	50	50	3.11	
	l_b	w_b	l_s	w_s
All branches	9.06	0.25	11.40	0.73

The microstrip implementations of both designs, on an FR408 substrate (detailed in §5) are shown in Figures 10 and 11. In the latter, the necessity of an off-center placement of the shortening stub for at least two vertical lines is apparent. The other 4 stubs are placed outside and bent for minimum footprint. It is worth noticing that a numerical optimization based on a full wave solution has been applied to both designs starting from the theoretical computations, hence lines are a little longer than that in the ideal model, and the effective length reduction of the horizontal and vertical branches is 54% rather than the desired 50%. It is worth mentioning that bent microstrip close to straight one causes additional parasitic effects [13].

Optimized dimensions are in Tables 2 and 3, respectively. The rectangular ring is hence $18.38 \times 9.19 = 168.9\,\text{mm}^2$ for the A layout and $18.75 \times 9.49 = 177.9\,\text{mm}^2$ for the B layout, to be compared with the standard rectangular Bagley divider which, for this same substrate and central

Table 3. Dimensions for the microstrip implementation, B layout (mm).

General	W	L	w_{50}			
	50	50	3.11			
Lower horizontal branch	l_b	w_b	l_{sb1}	l_{sb2}	w_{sb}	
	9.23	0.25	3.68	8.80	0.73	
vertical branch	l_s	w_{s1}	w_{s2}	l_{ss}	w_{ss}	
	9.23	0.097	0.458	12.49	0.73	
Upper horizontal branch	l_b^*	w_b^*	l_{st1}	l_{st2}	l_{st3}	w_{st}
	9.23	0.25	2.33	7.32	2.83	0.73

frequency, has $41.76 \times 22.01 = 922.7\,\text{mm}^2$. These are the outer rectangle dimension, taking into account microstrip line width. Area of the reduced rectangular ring is hence about 5 times smaller than the canonical ring. This reduction exceeds the 4 time smaller expected, due to microstrip line width. Since reduced rectangle lines have much higher impedance, their width is much smaller than that in the canonical implementation.

This comparison is anyway unfair, since the outer stubs do take space on the circuit board on both designs. A fairer comparison should take into account the envelope of the devices, which is indeed rectangular for the canonical device and is of a more complex shape for the two proposed layouts. With reference to Figure 12, A layout has a complex envelope covering $559.3\,\text{mm}^2$, while B layout has a rectangular envelope equaling $26.84 \times 16.21 = 435.1\,\text{mm}^2$. Compared with the $922.7\,\text{mm}^2$ occupation of a canonical Bagley divider, the reduction in area is 1.54 for the A layout and 2.12 for the B layout. It must be noted that outer stubs can be bent so as to reduce this area further in both cases, possibly choosing shape so as to fit within a given layout of neighboring components to achieve higher packing.

(a)   (b)
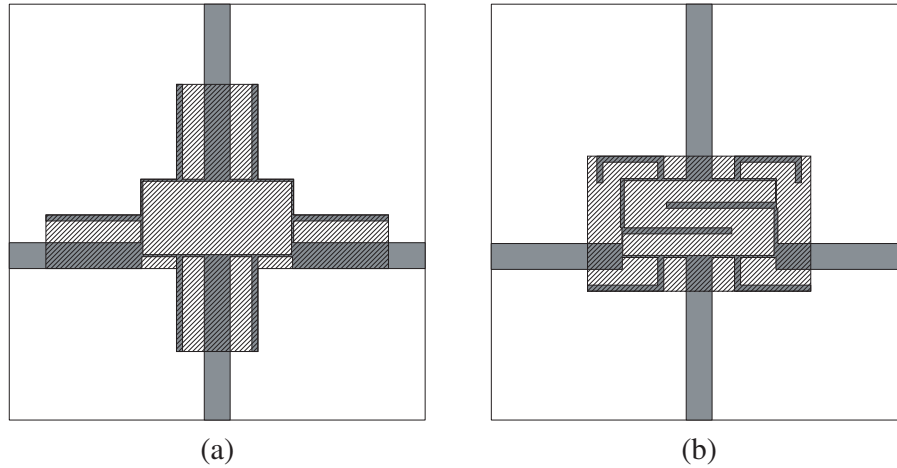
Figure 12. Envelopes (Hatched area) of the (a) A layout and (b) B layout reduced Bagley power divider, for estimation of the space occupied over a PCB.

4. CHARACTERIZATION

The two layouts have been printed by photo-etching procedure on a commercial "off-the-shelf" FR408 substrate ($\varepsilon_r = 3.4$, $\tan\delta = 0.01$, thickness $= 1.6\,\text{mm}$), Figure 13, and measured with a Keysight N5242A VNA working in the 10 MHz–26.5 GHz range.
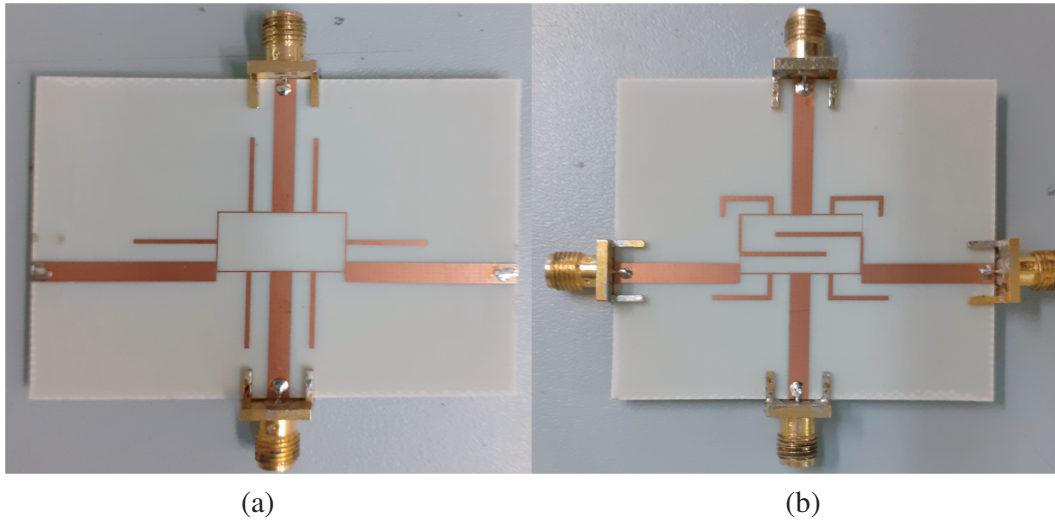
(a)   (b)

Figure 13. Photos of the two prototypes: (a) A layout; (b) B layout.

Figures 14 and 15 show both the results of full wave CST simulations (gray lines) and measurements (black lines). For the A layout device, S_{21} and S_{31} are of course identical due to symmetry, and curves in Figure 14 overlap, whereas this is not the case for the B layout device, hence in Figure 15 the two curves are distinct.
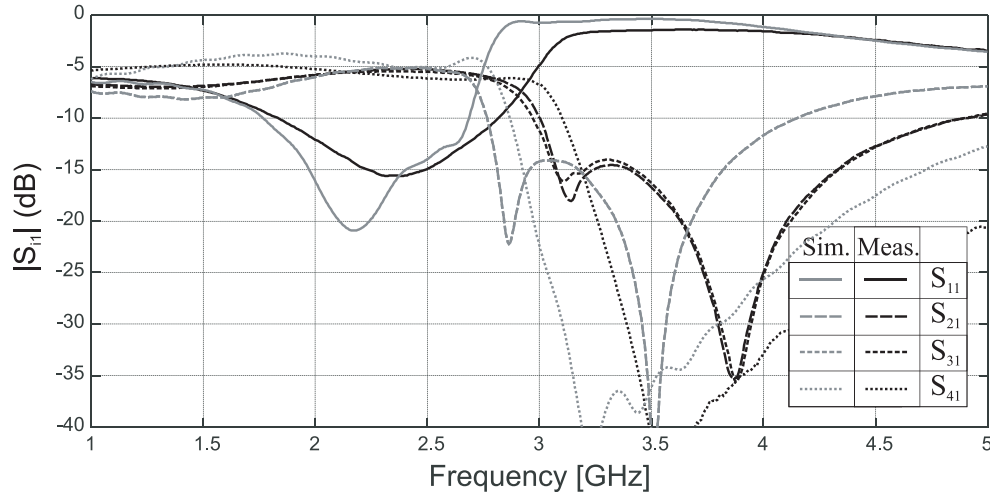

Figure 14. Full wave analysis (gray lines) and characterization over a prototype (black lines) for the symmetrical case.

A very good agreement between simulations and measurements is apparent. Table 4 shows the absolute bandwidth, computed over measured data, for the prototypes. Bands are defined as the frequency span, in GHz, in which the following limits hold:

$$|S_{11}| < -10\,\text{dB}; \qquad ||S_{i,1}| - |S_{i,1}(2.45\,\text{GHz})|| < 1\,\text{dB with } i \neq 1 \qquad (7)$$

Table 4 also shows band computed on CST simulated data for the canonical Bagley power divider. Port 1 matching band for B Layout is 62.3% of the corresponding band of the canonical layout, while the transmission parameter bands are, in the worst case, 79.7% of the corresponding parameter band in the canonical layout. Such a band reduction is of course due to the limited validity in frequency of the shortened delay lines, and with the band reduction over 60% and area reduction over 50% for B layout, it is an acceptable compromise.
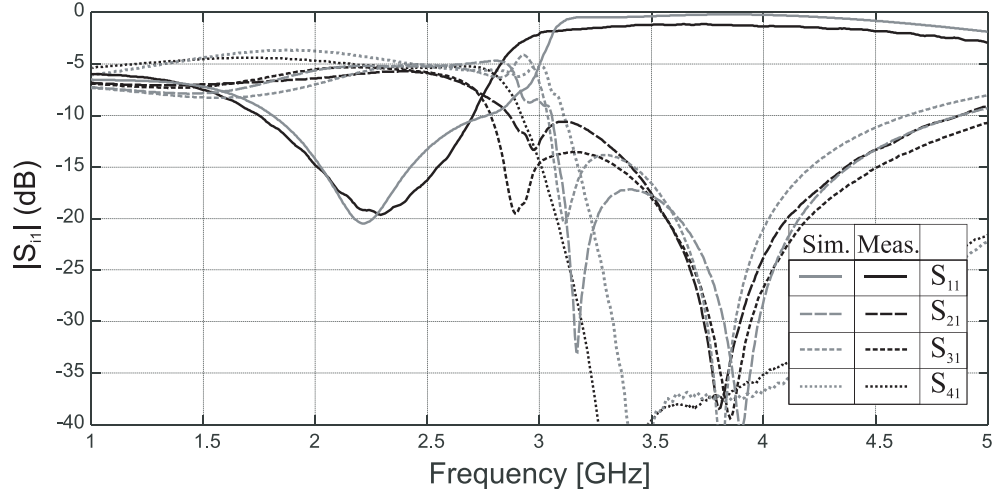
Figure 15. Full wave analysis (gray lines) and characterization over a prototype (black lines) for the non symmetrical case with inner stubs case.

Table 4. Absolute bandwidths (GHz) for reflection and transmission coefficients, measured data.

	Parameter	$|S_{11}|$	$|S_{21}|$	$|S_{31}|$	$|S_{41}|$
A Layout	Modulus@2.45 GHz (dB)	−15.25	−5.19	−5.45	−6.03
	Band (GHz)	0.977	0.989	1.088	1.126
B Layout	Modulus@2.45 GHz (dB)	−17.15	−5.73	−5.64	−5.31
	Band (GHz)	0.950	0.945	0.977	2.809*
Canonical+	Modulus@2.45 GHz (dB)	−22.64	−4.96	−5.03	−4.96
	Band (GHz)	1.524	1.186	1.186	1.124

* In this case the transmission parameter stays within ±1 dB with respect to its value at 2.45 GHz since the beginning of the measurements span, at 10 MHz.
+ Simulated data.

It is wort noticing that, while simulation leads to $S_{21} = S_{41}$ measured data shows a slight asymmetry due to the tolerances in the production process and connector solderings.

Finally, Table 5 shows, for a comparison with other solutions in cited literature, percentual bandwidths and occupied area in terms wavelength on a 50 Ω microstrip squared for the chosen substrate.

Table 5. Comparison with cited literature.

	Canonical+	A Layout	B Layout	[4]+	[6] a*	[6] b*
Band $|S_{11}|$	62.2%	39.9%	38.8%	78.2%	24.9%	24.3%
Band $|S_{i1}|$	48.4%	40.4%	38.6%	137%	51.3%	50.6%
Area	$0.125\lambda^2$	$0.0758\lambda^2$	$0.0589\lambda^2$	$0.0151\lambda^2$	$0.0915\lambda^2$	$0.0140\lambda^2$

+ Simulated data.
* Computed at the lower of the two working frequency.

5. CONCLUSIONS

A compact design for three-way Bagley power dividers attained by stub-loaded shortened delay lines has been presented. With respect to applications of this technique already published, in this paper a full theory for shortened delay lines with the stub placed in a generic position has been presented. This allowed for an easy placement of the stubs within the power divider ring.

The design and characterization of a prototype prove the validity of the design, with a band only slightly reduced with respect to a standard Bagley divider and a PCB area occupied which is less than a half.

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