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Affordable Satellite on the Move Antenna Based on Delay-Line-PLL Phase Shifting

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Abstract—This paper presents the design methodology, simulation, and affordable implementation of a mobile digital satellite broadcasting receiver with 64 elements. The speed and range of electronic beamforming are also obtained. The proposed methodology including techniques and architecture are defined by concerning cost, commercial off-the-shelf and components, and avoidance of high-frequency circuit designs by Delay-line-PLL for phase shifting, instead of expensive RF phase shifters with complicated control buses. Choosing this architecture results in using available elements and home receivers for antenna implementation. The design results in 6-bit resolution phase shifters and ± 16 degrees 2D half power electronic beam scanning range. For practical implementation feasibility, a prototype of the array is fabricated and tested, successfully. Obtaining the phase shifters' resolution and sampling of the array output power are also described. A simple and effective algorithm is proposed for grating lobes elimination, and SNR maximizing which performs the tracking task under the platform movement conditions.

1. INTRODUCTION

Demands for mobile reception of high definition (HD) video and broadcasting services are rapidly increasing. The wide area coverage of satellite broadcasting is deniable. Satellite on the move antenna (SOTM) receivers are not commonly used for economic solutions. These intelligent antennas are used for expensive platforms such as airplanes, trains, vessels, and vehicles. In contrast with mechanical gimbals, these smart antennas are planar and have very agile tracking under perturbation circumstances. In contrast with mechanical gimbals, these smart antennas are planar and have very agile tracking under perturbation circumstances by using electronic beamforming. The calibration process for this system is very critical, where algorithms should try to eliminate dependencies such as temperature, pressure, and manufacturing inaccuracies.

A phased array system is a relatively expensive product. Recent advances in solid-state technology have made the dream of cheap phased arrays a reality [1]. Here, an affordable design of a SOTM antenna is proposed based on the Delay-Line Phased Locked Loop (PLL) phase shifting technique step by step. The substantial two features of this design are described as follows:

The first key feature of this design is using the universal low noise blocks (LNBs) as array elements, common intermediate frequency (IF) combiners, and home satellite receivers. For a low-cost solution and a fast implementation approach, component-level design is avoided. Consequently, observing the compatibilities and standards is inevitable. Considering these compatibilities for using commercial off-the-shelf (COTS) elements keeps the efforts in system-level design; otherwise, it is unavoidable to deal with serious concerns from scratch, especially in RF circuit designs such as mutual coupling, cross-talk, system linearity, signal isolation, and resonance [1]. In [2], the authors encountered the

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mentioned concerns. To accomplish this goal and avoid these concerns, we use the Delay-line-PLL phase shifting approach described in [5–13] as a local oscillator (LO) phase shifting architecture, which is implementable easily over COTS elements.

The second key feature of the design is a proposed electronic two-dimensional searching and tracking algorithm that eliminates the fast gyro sensor and agile azimuth mechanical tracking control used in one-dimensional hybrid models [4]. To advance the systems' performance in hostile environments in terms of noise, interference, various weather conditions, and sharp maneuvers, [3] introduces an electronic beamforming algorithm with analog phase shifters. Although the proposed method is introduced for SOTM applications, it can be used for the sum-difference reconfigurable patterns in digital domain such as the one presented in [14].

2. DELAY-LINE-PLL PHASE SHIFTING THEORY

The first step in any phased array antenna project is determining the suitable architecture. Fig. 1 demonstrates different types of phased array receiving architectures.

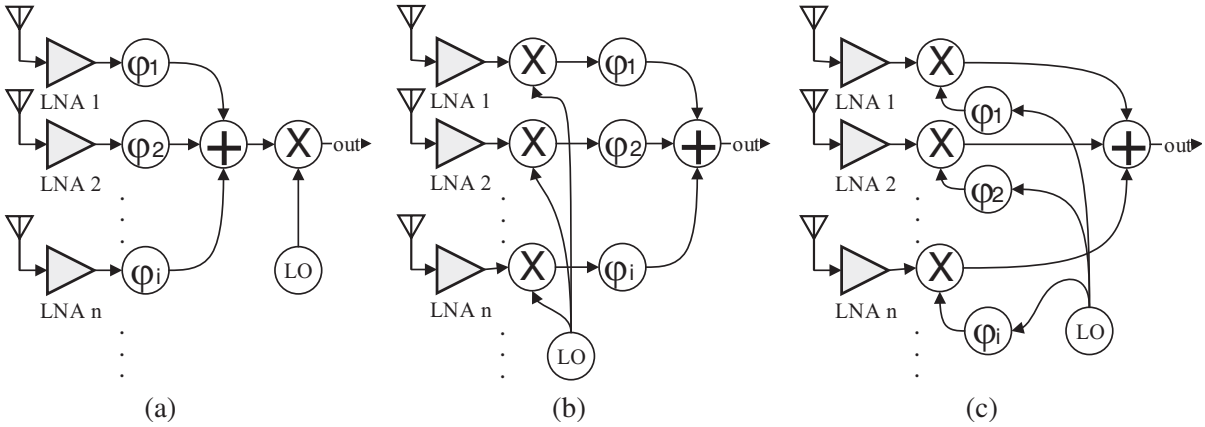


Figure 1. Types of phase array receiving architectures according to phase shifting path: (a) RF phase shifting, (b) IF phase shifting, and (c) LO phase shifting.

In addition to these, there is also a fourth digital array architecture. Each RF path is down-converted to a suitable IF frequency. A Digital Signal Processing (DSP) unit then performs all beamforming tasks and recovers the desired signal from the undesired interferences after digitizing the IF signal. The IF sampling requires very high-speed analog-to-digital converters and spatial processing, which leads to complicated processing hardware. Therefore, this architecture is not economical. For instance, [15] introduces an anti-jamming technology with the same architecture for satellite communication that can cancel terrestrial jammers.

These phased array antenna architectures require low noise amplifiers (LNAs) to maintain a high Noise Figure (NF). For a system with an element, LNA power consumption is not significant (about 0.5 Watt), but it is significant for an array with many elements. Low power consumption and high gain are two challenges that CMOS and SiGe technologies face in the Millimeter Wave (MMW) frequency band [16].

As mentioned earlier, we decided to use universal LNBs as array elements. In other words, each LNB consists of an LNA and a mixer with a selectable 9.75 GHz or 10.6 GHz local oscillator frequency, and its output is IF frequency in the range of 950 MHz to 2150 MHz. Therefore, the choice becomes narrowed down to one of the IF phase shifting or LO phase shifting architectures, shown in Figs. 1(b) and (c). Because of the large number of array elements, the high price of IF phase shifters, and the complicated control buses, we have to find an approach to eliminate them. This approach is direct data synthesizer phased locked loop (DDS-PLL) phase shifting or its revised version, called Delay-line-PLL derived from LO path phase shifting architecture. On the other hand, phase shifting is applied in

this approach to the whole spectrum; therefore, this architecture is suitable for ultra-wideband (UWB) applications [17–19].

LNBs mostly have a 25 MHz internal crystal; therefore, we replaced these crystals with 25 MHz external clocks as shown in Fig. 2, to control the phase of the local oscillators. Notice that PTW stands for phase tuning word, and the phase relationship between PTWs and the LOs will be considered. In this approach, phase shift is applied to clocks instead of LOs.

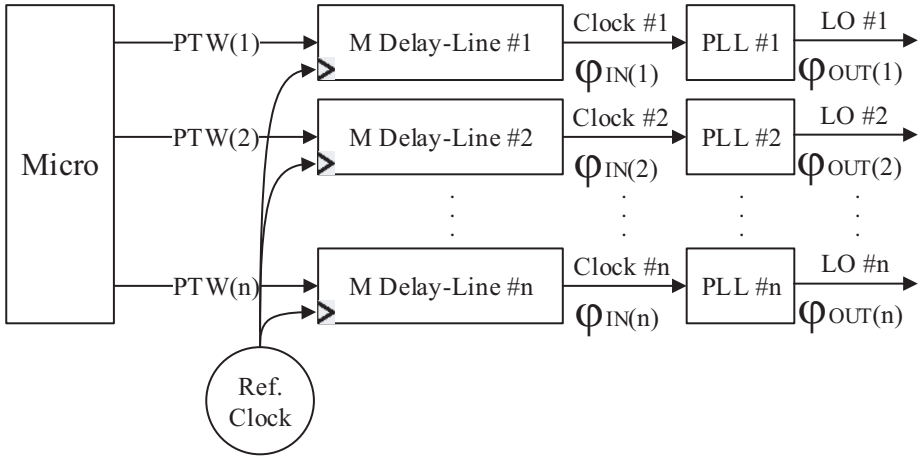


Figure 2. Delay-line-PLL block diagram architecture.

There is a well-established theory about DDS [20]. This theory is also true for Delay-Line-PLL. According to this theory, the DDS signal next to the feedback output signal after passing through the phase-detector generates an error voltage that is suitably filtered, and forces the voltage-controlled oscillator (VCO) instantaneous phase divided by an integer factor, N_{PLL}, to be equal to the DDS reference phase. Thus, in DDS-PLLs, the DDS block allows the control of a digital PTW to continuously vary the reference phase produced at its output, and therefore, it acts as the phase control unit (PCU) of the PLL output. This allows combining the PLLs' ability to generate stable high-frequency clocks with the exceptionally high phase resolution of DDSs.

Suppose that $\varphi_{IN(n)}$ is the nth input phase of the nth PLL relative to the first input phase of the first PLL ($\varphi_{IN(1)}$) as zero phase reference clock. The relation between $\varphi_{IN(n)}$ and $PTW(n)$ is expressed

$$\phi_{IN}(n) = PTW(n) \times \frac{2\pi}{M} \tag{1}$$

where M is the clock division number of the delay line.

There are two key parameters in the Delay-line PLL approach which are necessary to obtain and should be considered: the first is effective phase of the nth PLL output relevant to the first PLL output phase, and the second is phase resolution.

The effective phase of the nth PLL output (nth local oscillator) is as (2).

$$\phi_{OUT}(n) = \mathrm{mod}(N_{PLL} \times \phi_{IN}(n),\, 2\pi) \tag{2}$$

The effective phase of PLL output depends on the greatest common divisor (GCD) of N_{PLL} and M, so output phase resolution (OPR) of a Delay-line-PLL is preserved (avoid the phase overlap) if and only if one of the N_{PLL} or M is an odd number. The mathematical expression of OPR is as (3).

$$OPR = \frac{M}{GCD(N_{PLL}, M)} \tag{3}$$

For a given output phase, obtaining the corresponding PTW can be done through a lookup table (LUT), because analytically obtaining the invert of (2) due to *mod* operand is impossible.

3. DESIGN AND SIMULATION

3.1. System Design

After reviewing the desired architecture, we start designing and simulating step by step. By using off-the-shelf parts, this system avoids the complexity of RF design. Achieving this goal will not sacrifice quality. IF combiners and commercially available LNBs are also used for this purpose.

As shown in Fig. 3, the IF outputs of LNBs are combined by 8-to-1 combiners and connected to a 1-to-2 divider to feed a receiver and a power detector. After passing through an anti-aliasing low-pass filter, the power detector's output is sampled by the microcontroller's internal analog to digital converter (ADC). To control the azimuth and elevation motors, the microcontroller calculates the satellite's position using GPS and a compass. Therefore, the antenna array is pointed to the desired satellite direction with an acceptable accuracy. After receiving the signa, SAT-ID is checked. The mechanical slow control loop is searching to receive the maximum power. A high speed electronic beamforming

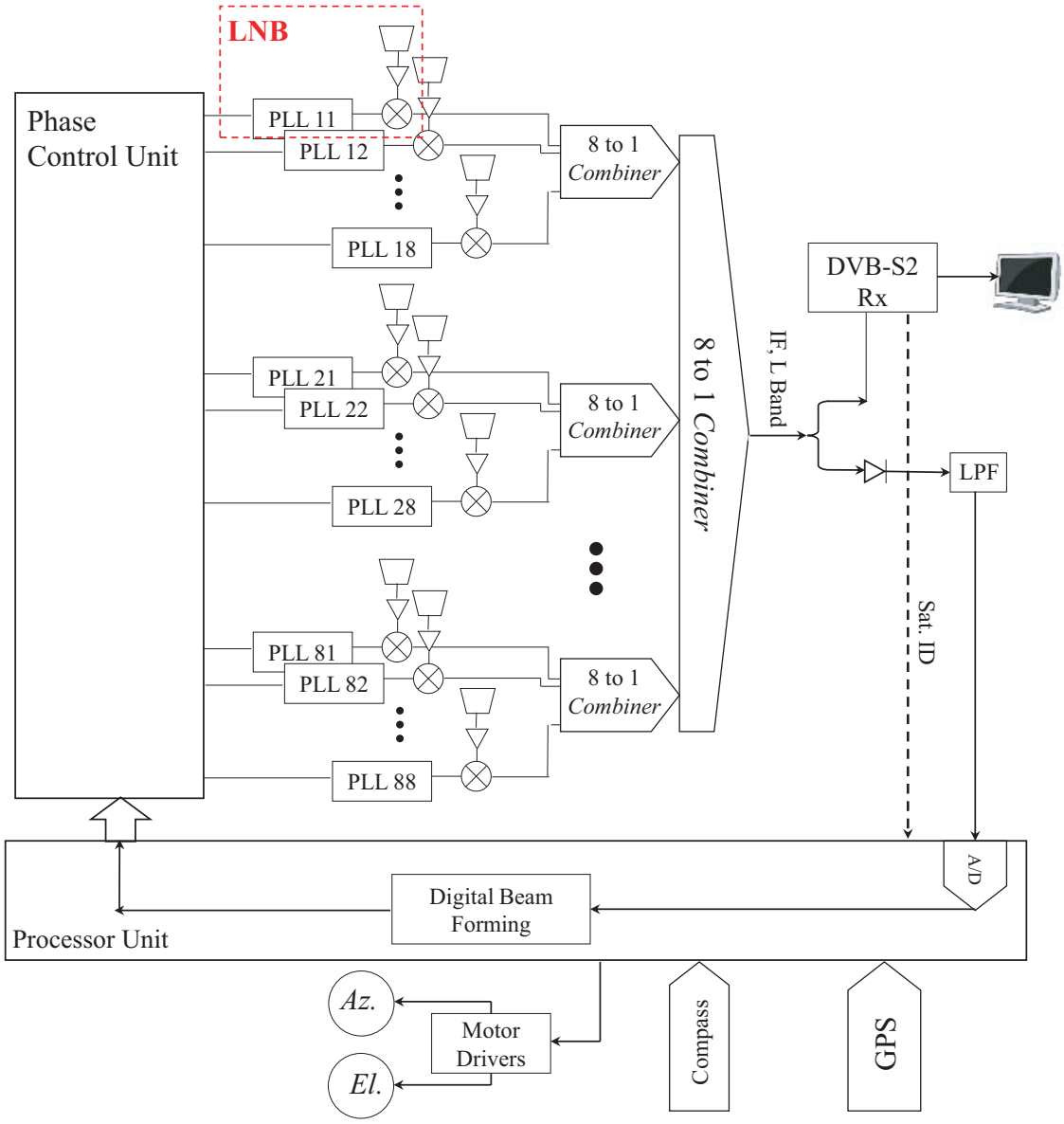
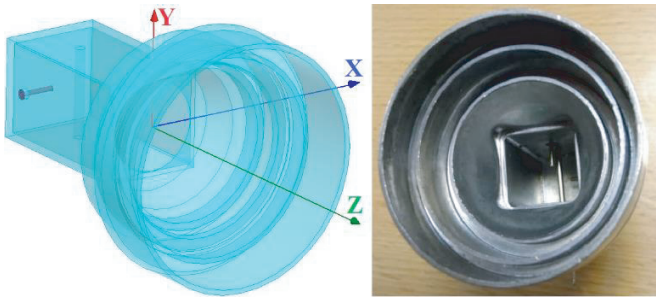


Figure 3. Proposed SOTM configuration.

or signal-to-noise ratio (SNR) optimization algorithm always performs tracking to grab the signal as quickly as possible.

3.2. Antenna Design

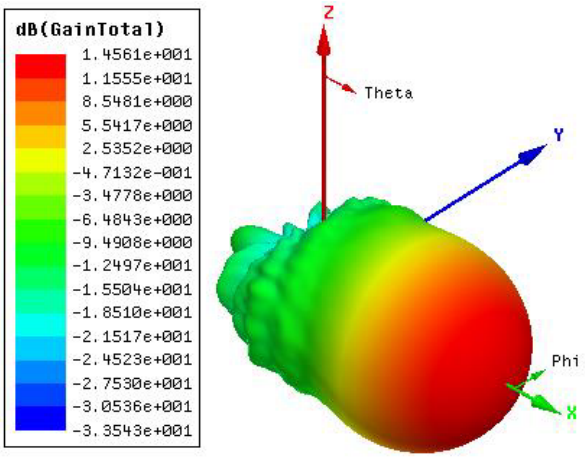
The horn antenna used in a commercial LNB structure and its end waveguide with vertical and horizontal polarization excitation probes are shown in Fig. 4. It is worth noting that the center bar is built in to provide better isolation, and the concentric rings increase the S_{11} bandwidth at the desired frequency range, 10.7 GHz to 12.7 GHz.



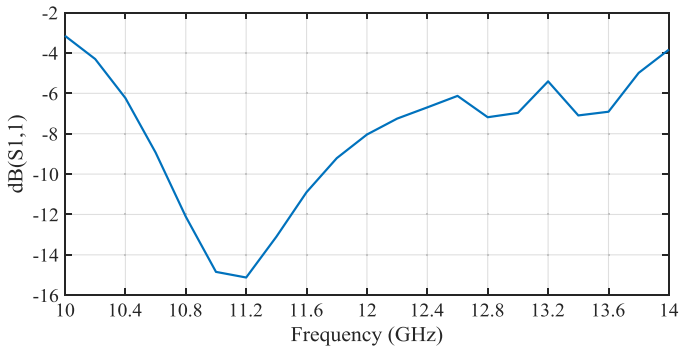
(a) (b)

Figure 4. LNB feed and horn antenna. (a) Simulated scheme. (b) Real picture.

The HFSS software is used to simulate the antenna, using real values derived from a commercial sample. Fig. 5(a) shows the horn antenna gain patter, and Fig. 5(b) depicts $|S_{11}|$. The antenna gain and half power beam width (HPBW) are about 1.5 dB and $\pm 16°$, respectively.



(a)



(b)

Figure 5. Results of full-wave simulation of LNB feed and horn antenna. (a) 3D gain pattern, and (b) $|S_{11}|$ vs. frequency.

According to the principle of antenna arrays and considering that the coupling of adjacent antennas is negligible, the antenna array is simulated in MATLAB using (4) [21], which is very fast and accurate instead of full-wave simulating, which is time-consuming as

$$AF = \sum_{m_a=1}^{M_a} \sum_{n_a=1}^{N_a} e^{j[(n_a-1)(kd\sin\theta\cos\varphi)+(m_a-1)(kd\sin\theta\sin\varphi)+x(n_a,m_a)]} \tag{4}$$

where M_a and N_a are the array dimensions; k is the wave number; d is the element spacing; and x is the initial phase of each element which is selected by m_a and n_a indices.

Before starting the simulation, it is necessary to define an optimal distance between the elements, which according to the LNB horn aperture and array physical structure, is considered 2.5 times of wavelength [22].

Figure 6 shows the array pattern. Grating lobes are created due to the non-observance of typical 0.5λ element spacing.

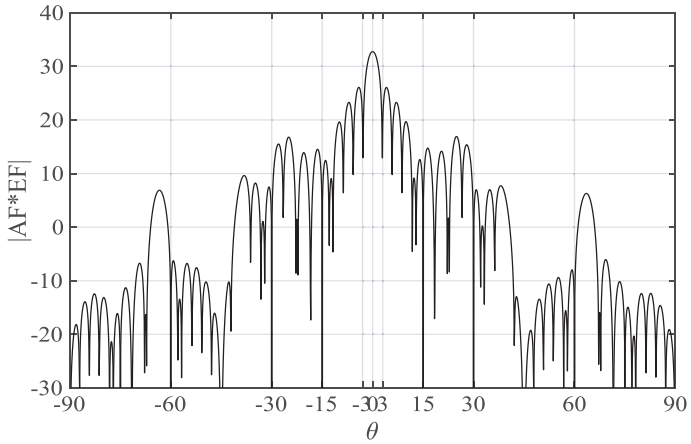


Figure 6. Simulated 2D radiation patter.

The commercial LNB works with horizontal and vertical polarizations obtained by the fed DC voltage through the IF output, whereas 13 V and 18 V indicate vertical and horizontal polarizations. Because the receiver is on the move, the reception polarization should be circular. The circular polarization can be accomplished by using 2×2 subarrays with 0, 90°, 180°, and 270° LO phase shifting.

3.3. Phase Shifters Resolution

The phase shifters resolution determines the entire system price. Therefore, this part of calculation is one of the most significant sections of the design. The relationships between beam angle and phase shifters are expressed in (5).

$$\Delta\phi = \left(\frac{2\pi d}{\lambda}\right)\sin\theta \tag{5}$$

where $\Delta\varphi$ is the phase difference between adjacent phase shifters, and θ is the beam angle relevant to the vertical axis.

Now, by taking the differential from both sides of (5), (6) is achieved.

$$d\Delta\phi = \left(\frac{2\pi d}{\lambda}\right)\cos\theta \times d\theta \tag{6}$$

The following facts are achieved from (6).

- Beamforming in the broadside ($\theta = 0°$): the cosine is replaced with a unit value. In this case, the cosine coefficient is approximately 1, so for 6-bit phase shifting (5.7° steps), beam-steering accuracy becomes 0.4°. In the range of ±16° HPB, this accuracy remains constant approximately.
- Beamforming in end-fire: the cosine tends to zero, and the resolution tends to infinite.
- Increasing the space between array elements causes the growth of number of grating lobes. Consequently, the width of the main beam or range of beamforming decreases.
- The beamforming resolution is independent of the number of array elements.

3.4. IF Combiners and Power Measurement

Available IF combiners are applied to aggregate the output of the LNBs. An 8-to-1 combiner can be a good choice for any array row. The aggregated signal of these combiners goes to a 1-to-2 power divider; one goes to the receive, and another to the power detector module to measure the instantaneous output power.

The autocorrelation function given in (7) calculates the power signal of a periodic $x(t)$ function.

$$y(t) = \int_0^T x(t)x(t-\tau)dt \tag{7}$$

The range of input IF signals in commercial receivers is -65 dBm to -25 dB. The LT5534 power detector chip is applied to generate the power signal from the array IF output. The output conversion ratio of this chip is about 1 V/10 dB, and its output voltage range is 1 to 2 volt. For example, an ARM microcontroller has a 12-bit ADC, and we intend to use most of its accuracy for the tracking algorithm.

According to the sampling theorem, an anti-aliasing filter should be applied before sampling to prevent spectral aliasing, and the input signal bandwidth shall be limited.

For an ADC with 12-bits resolution, attenuation in the twice sampling frequency is greater than $20\log_{10} 2^{12} = 72$ dB. Therefore, a low pass filter with cut-off frequency of more than 72 dB attenuation in twice the sampling frequency must be considered [23]. With 2.56 V voltage reference and a 12-bit ADC, 1.25 mV is the minimum measurable voltage (LSB), which equals 0.0125 dBm power. However, the output of the power detector fluctuates due to the noise existence, and we should try to reduce this uncertainty in the measurement as well.

Sample averaging or digital filtering is an effective technique to reduce the noise uncertainty of the measured power signal. For instance, suppose that the noise fluctuation of the measured power signal is 0.05 dB, and acceptable measuring fluctuation is 0.01 dB. In this case, we need to reduce the standard deviation of the noise five time. According to (8) proved in [24], it is accomplished with 25 samples averaging

$$\sigma_{ave} = \sigma\sqrt{\frac{1}{n_s}} \tag{8}$$

where n_s is the number of samples. This assumption supposes that we have a group of samples that are independent of identical density (iid).

3.5. Delay-Line Design

As we know from the delay line theory, one of these parameters, PLL division factor N_{PLL} or the counter number M [5] must be odd to generate all phases at the output without overlap. In this case, the PLL division factor for 10.6 GHz local oscillator frequency and 25 MHz crystal is 424 and even, so we should choose an odd counter number to prevent phase overlap. The GCD of 63 and 422 becomes one, and the maximum OPR equals 63. 63 can be a good choice, the closest odd number to accomplished 6-bit resolution. Accordingly, we can generate the LUT for finding the relevant PTWs.

The 63 counts involve 31 high-states and 32 low-states. Under these conditions, the duty cycle is a little less than 0.5, and it does not affect the proper working of PLLs. We can implement these sequences of high and low states by circular shift registers, and PTWs can be preset to the shift registers. Therefore, shift registers need a clock with a frequency 63 times of LNBs' clock frequency (25 MHz), equal to 1.575 GHz. On the other hand, the internal clock frequency of field programmable gate arrays (FPGAs) usually does not support a frequency higher than 300 MHz. For this purpose, we use $\times 8$ clock multipliers after FPGA output clocks. Therefore, instead of clocks with 25 MHz frequency, FPGA produces 3.125 MHz, and FPGA clock is reduced from 1.575 GHz to 198.875 MHz, consequently.

3.6. Jitter Constrain

At a glance, temporal vibration of the local oscillator frequency is allowed if it does not cause a phase shift or 1/63 of its periodicity (equivalent to 0.015 UI). To calculate this jitter at the clock, we need to

multiply this value by $N_{PLL} = 424$, which equals 317 ps ($\pm$158 ps) at 25 MHz. We can interpret the time vibration in the frequency domain by taking the differential from both sides of the time-frequency relationship, as shown in (9). The calculated jitter is equal to $\pm$100 kHz for a 25 MHz clock that does not restrict us practically.

$$f = \frac{1}{T} \rightarrow df = \frac{dt}{T^2} \tag{9}$$

Notice that this analysis becomes important in the case of high-resolution phase shifters [25]. We also consider frequency vibration from another perspective. The acceptable range of changes for the local oscillator frequency is called carrier frequency offset. Its allowable value is up to $\pm$1 MHz in this design case. Therefore, the maximum jitter should be less than $1/N_{PLL}$ of this value, which is something around 2.3 kHz (equal to 95 ppm). The commercial crystal oscillators and clock multipliers comply with lower jitter rates than this.

4. DIGITAL BEAM FORMING TRACKING ALGORITHM

4.1. Software Operational Modes

The algorithm of the system software is shown in Fig. 7 which has two functional modes. The first operating mode is *initialization* or *re-initialization*, when the system does not receive the satellite signal or SAT-ID is incorrect. In this mode, the system calculates azimuth and elevation by using GPS and compass, where the mechanical control loop commands the motors to adjust the direction of the antenna. This mode of operation is also called *Search Mode*. The mechanical scanning method can be called as *conical scan* method. In this method, the controller rotates the beam around an axis perpendicular to the antenna array plane to align it in the maximum receiving power direction. After finding the correct satellite, the system changes the operation mode automatically.

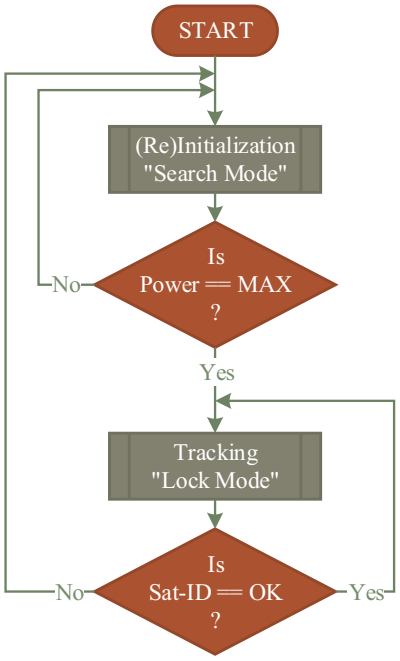


Figure 7. Flowchart of the system software.

The second operating mode is *Tracking*. When receiving the signal's power is an acceptable value, and the SAT-ID is also correct, the system comes into this mode of operation. In this mode, the SNR optimization algorithm is responsible for maximizing the desired signal and eliminating noise and mechanical vibrations. This mode of operation is also called *Lock Mode*.

It is worth mentioning that manually calibrating an array with many elements is onerous. So we strongly suggest that it can be done by a built-in calibration procedure automatically.

4.2. Beamforming in Tracking Mode

The beamforming algorithm in tracking mode is an "SNR optimization algorithm" which maximizes the desired signal strength and minimizes the noise and mechanical vibrations [3].

The number of system variables (phase of phase shifters) is remarkable here, so we need an effective method for solving this real-time optimization problem. Most multivariate optimization methods use function gradients which are also called indirect methods. The main reason for the diversity of these methods is the difference in how they determine the *search direction* and *search step size* parameters. However, we use a simple gradient-based method for this design, and we consider only these two parameters for this case. A gradient-based method approximates the function with the first two sentences' expansion of the Taylor series as follows:

$$\begin{aligned} f(\mathbf{x}+\delta\mathbf{x}) &\cong f(\mathbf{x}) + \mathbf{g}\,\delta\mathbf{x}^T + \ldots; \\ \mathbf{x} &= [x_1,\, x_2,\, \ldots,\, x_N] \\ \delta\mathbf{x} &= [\delta x_1,\, \delta x_2,\, \ldots,\, \delta x_N] \\ \mathbf{g} &= \nabla f(\mathbf{x}) + \left[\frac{\partial\, x_1}{x_1}, \frac{\partial\, x_2}{x_2}, \ldots, \frac{\partial\, x_N}{x_N}\right] \end{aligned} \tag{10}$$

Equation (10) demonstrates how the Taylor series work for multivariable functions. In the gradient or steepest ascent method, the main idea is the first derivative of the objective function. Stepping in the direction of the gradient leads to a local maximum of that function; the procedure is known as gradient ascent.

For real-time optimization, the process must be done element by element and step by step. For this purpose, the value of the perturbation is defined by StepSize which is an integer value equal to the phase shifters resolution. As obtained earlier, StepSize equals 5.7°.

After applying a perturbation, a new objective function value is calculated by (11).

$$f(x_n^{i+1}) = f\left(x_n^i \pm StepSize\right) \tag{11}$$

where i is an iterative number, and n is the number of phase shifters.

After applying a perturbation to an element, the value of the new objective function is obtained which indicates the correct direction of the optimization. Therefore, this process is done in an infinite loop, element by element and step by step. Fig. 8 shows the algorithm of this optimization process. The optimization algorithm works by perturbing the phases or applying positive and negative perturbations. In the initialization, we can choose the sign of the perturbations arbitrarily.

We modeled the desired signal, noise, and mechanical vibration for simulating the optimization algorithm. The antenna noise temperature equation is shown in (12) and demonstrates this model.

$$T_A = \frac{1}{4\pi}\iint T(\theta,\varphi)\, G(\theta,\varphi)\, \sin\theta\, d\theta\, d\varphi \tag{12}$$

For this purpose, an objective function is defined with the assumption that the main lobe is equivalent to the desired signal, and the side lobes are equivalent by the noise as

$$f(x_1,\ldots,x_N) = +|mainlobe(\mathrm{dB})| - |sidelobes(\mathrm{dB})| \tag{13}$$

where $x_1 \ldots x_N$ is the phase of phase shifter. Notice that the side lobes do not have the same noise temperature in reality, but we consider them the same here for more convenience.

Figure 9 shows the output of the optimization function in two examples of StepSize, and how to reach the optimal point with a two-sided mechanical vibration generated by rotating the antenna axes in simulation.

One of the necessities in array systems is self-testing and the impaired elements declaration in case of failure. The proposed optimization algorithm can also perform the role of self-testing with some considerations.

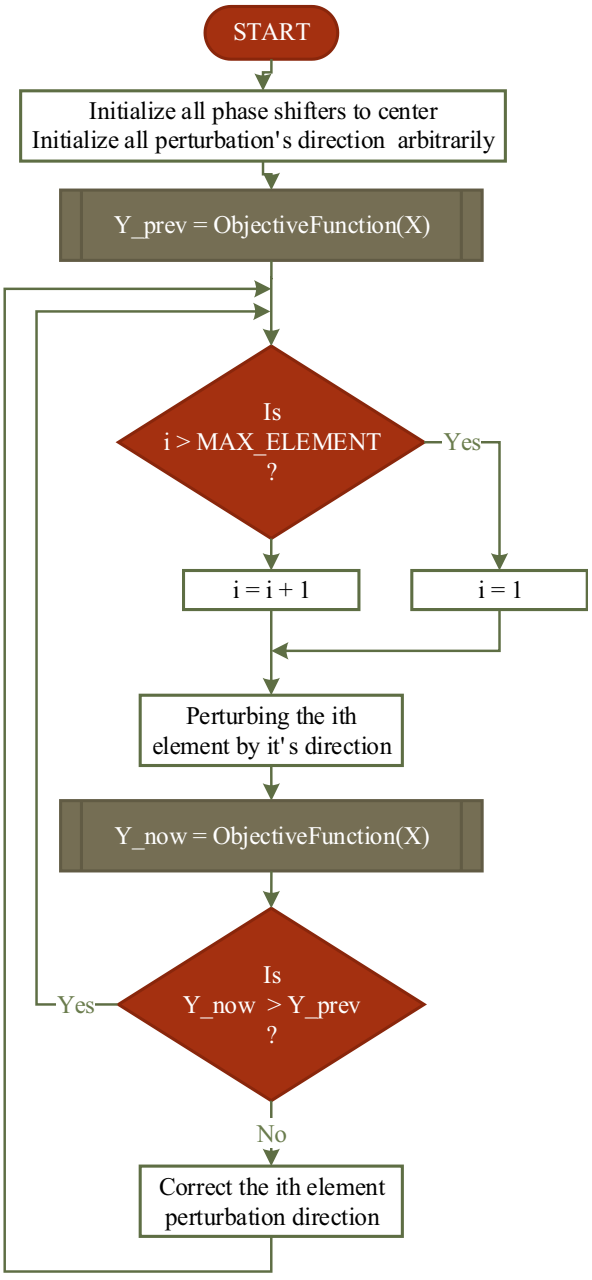


Figure 8. Flowchart of the SNR optimization (tracking) algorithm.

4.3. Electronic Beamforming Feedback Loop

After applying any perturbation in the process of SNR optimization, two factors determine the correct delay of output power signal measurement or the speed of the beamforming (tracking); the PLL lock time (settling time) and the anti-aliasing filter la. Fig. 10 shows the modeled electronic control loop. The bandwidth of these two filters determines the speed of the electronic beamforming.

The closed loop transfer function of the PLL is as

$$H(s)_{PLL}^{CL} = \frac{\frac{K_{PD}\,K_{VCO}}{N}\frac{F(s)}{s}}{1+\frac{K_{PD}\,K_{VCO}}{N}\frac{F(s)}{s}} \tag{14}$$

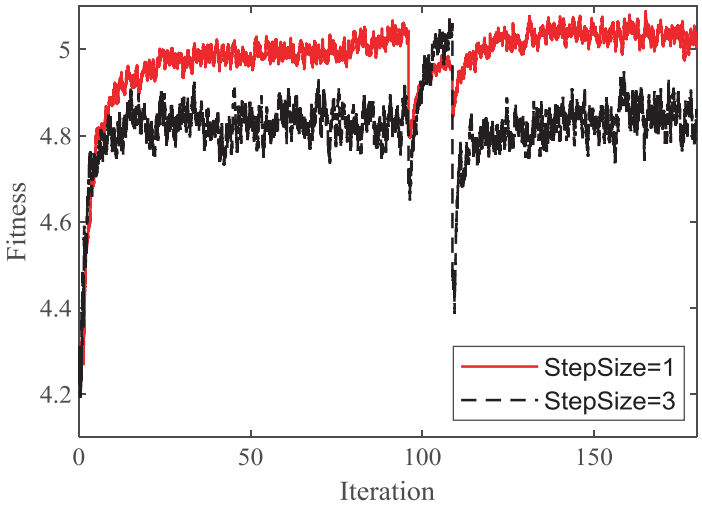


Figure 9. Learning curve of the SNR optimization objective function, 1 StepSize = 5.7°.

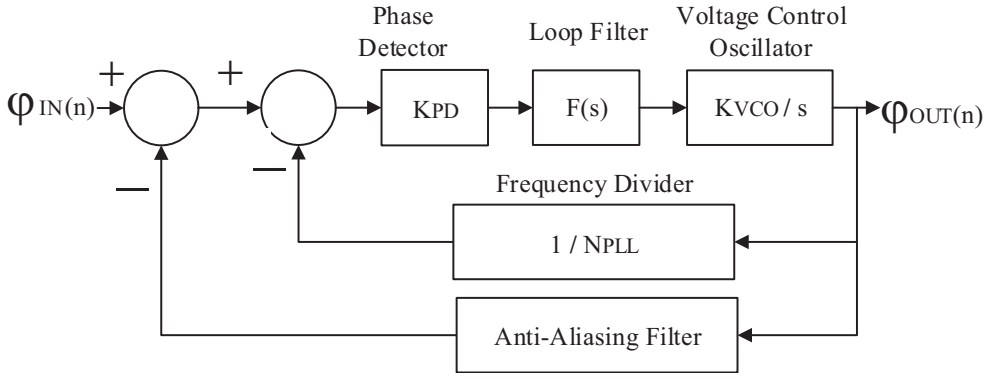


Figure 10. Block diagram of the closed-loop electronic beam-steer with a simplified linear model of the PLL and antialiasing filter.

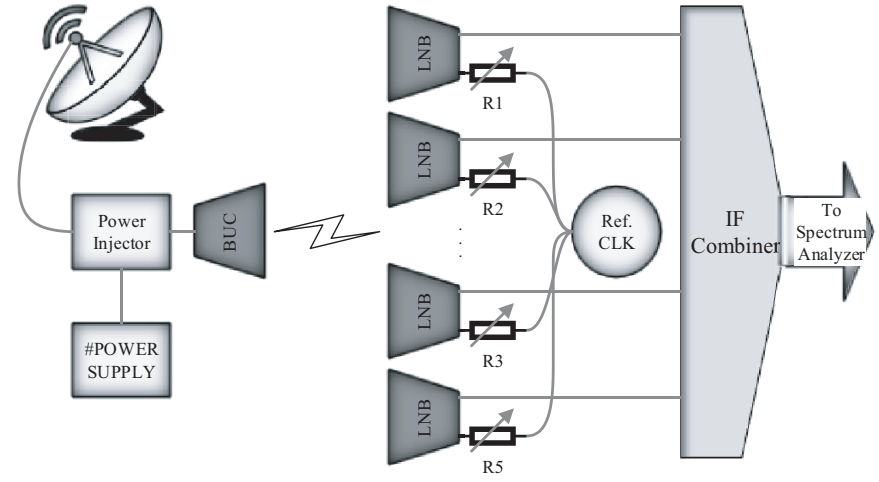
where $F(s)$ is the PLL loop filter transfer function [26, 27], and K_{PD} and K_{VCO} are the phase detector and VCO constant factors, respectively. Notice that the loop filter $F(s)$ has an important role in the PLL lock time.

5. TEST SETUP AND RESULTS

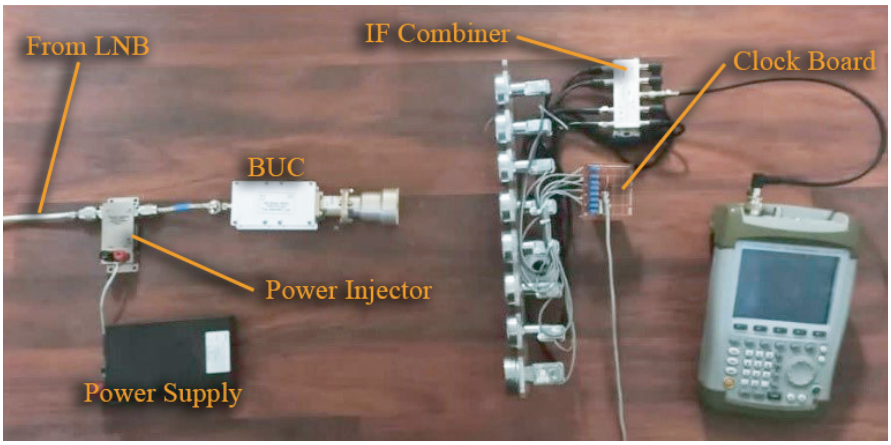
A test procedure is proposed for the feasibility assessment of LNBs coherency. For this purpose, test setup is provided with minimum components as demonstrated in Fig. 11(a). The weak signal received from the satellite necessitates a setup for testing the prototype array antenna. A customized block up-converter (BUC) with a 10.6 GHz local oscillator is used as well as a small horn antenna. A dish antenna is aligned to a desired satellite which provides an IF signal for BUC.

We observed the coherency by varying the series multi-turn 100-ohm potentiometers in the path of 25 MHz clocks of LNBs and considering their coaxial cables capacitance (100 pF per 1 m typically, as shown in Fig. 11(b).

Figure 12 demonstrates the spectrum of the aggregated power signal. This figure shows the different adjacent IF broadcasting channels. Notice that coherency occurs when the amplitude of the aggregated output power signal reaches its maximum value.



(a)



(b)

Figure 11. (a) Test setup schematie. (b) A view of the prototype LNB array and BUC, power supply, and power injector.

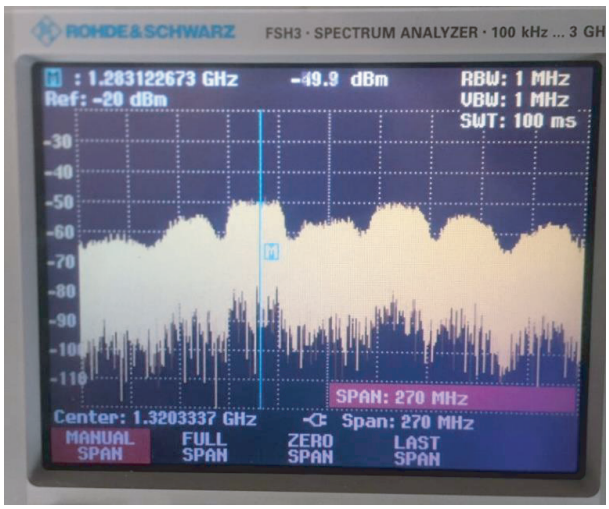


Figure 12. Output power spectral of phased array receiver prototype.

6. CONCLUSION AND FUTURE WORK

Due to the far distance of GEO satellites (36000 km altitude), their receivers need an antenna with a very high gain. This matter restricts the range of electronic scanning. For LEO satellite constellations (below 2000 km altitude), we can use antenna arrays with a wide scanning range to find satellites for both-way communication, such as the internet. Consequently, satellite communication is becoming more than ever available, and by this proposed method, mobility in satellite communication can be accessible more economically. The clock Delay-line PLL phase shifting approach is a cost-effective, easy-to-implement, ultra-wideband (UWB), portable hardware, and frequency-independent architecture, and all of these benefits are remarkable. We can apply this architecture for BUCs (instead of LNBs) to make transmitters with phased array antennas featuring high symbol rate. With the aim of this architecture, implementing the array radars becomes easier. The only bottleneck of this approach that restricts the speed of beamforming is the PLL lock time where using very fast locking PLLs would solve this problem.

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