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A Hot-Via Chip-to-Substrate Interconnect for Ultra-Compact System Package Application Up to W Band

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Abstract—A hot-via chip-to-substrate interconnect with its operation frequency up to W-band for ultra-compact radio frequency (RF) system in package (SIP) is reported in this paper. In order to improve the accuracy of the simulation model in millimeter wave bands, a trapezoidal platform model is established for modeling the RF performance of the hot-via which is formed by inductively coupled plasma (ICP) etching process. A three hot-vias structure in a gallium arsenide (GaAs) chip is employed to form a Ground-Signal-Ground (GSG) transition structure. Bumps on the Silicon substrate are designed as a half quasi-coaxial structure to make it compatible with the assembly process of SIP. A full-wave simulation model is established for a hot-via chip-to-substrate interconnect structure with HFSS, based on which structural parameters, such as the gap between the hot-vias and the radius of the quasi-coaxial structure, are optimized for the best performance over 92–96 GHz. A prototype of the hot-via chip-to-substrate interconnects in their back-to-back connected form has been fabricated. Measured results demonstrate that the overall insertion loss is less than 1.85 dB, and the return loss is better than 12 dB from 92 GHz to 96 GHz.

1. INTRODUCTION

With the development of new generation communication technology, the working frequency of communication system is moving to the higher millimeter wave band up to W-band. RF front-end modules (FEMs) are becoming increasingly complicated due to the demands of higher frequency and data throughput. To meet the needs of compactness and reliability, there is growing tendency that a large portion of millimeter wave FEMs will be integrated in compact and cost-effective packages using so called system in package technology. As recognized in the RF community, low insertion chip-to-substrate interconnection is one of the most challenging techniques in the development of SIP, especially in shorter millimeter wave bands such as W-band.

Wire-bonding is a commonly accepted technique for the interconnection between monolithic microwave integrated circuits (MMICs) and the different substrates in packaged integrated circuits (ICs), hybrid microwave integrated microwave integrated circuits (HMICs) and multi-chip modules. However, for millimeter wave applications, the inductance of the bonding wire becomes dominant and will significantly influence the performance [1, 2]. Therefore, numerous new interconnection technologies have developed to overcome this problem, among which hot-via interconnect has been proven to have superior performance in several aspects over other interconnect schemes for high frequency applications [3].

A heterogeneous integrated low noise amplifier (LNA) module at Ka band is reported in [4], where the hot-via transition has been successfully applied to realize the chip-to-substrate interconnect. A surface mount LNA chip with novel hot-via interconnection is reported in [5], of which operating frequency reaches 90 GHz. One more example of the application of the hot-via transition is reported

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in [6], where an ultra-compact, low-cost Wi-Fi FEM module is developed using the hot-via chip-scale package technology.

In this paper, a hot-via chip-to-substrate interconnect for compact RF system in package at W-band is reported. A trapezoidal platform model is established for the hot-via to improve the accuracy of simulation of its RF performance. The structural parameters' influence on the performance of the hot-via vertical transition in the GaAs chip and the matching structure on the silicon substrate is analyzed by HFSS. In particular, an eccentric open circle on the ground is designed to reduce the size of the matching structure. Finally, a prototype of the hot-via chip-to-substrate interconnects in their back-to-back connected form is fabricated, and the measurement results of S-parameters in W-band are presented.

2. MODELING OF THE TRAPEZOIDAL PLATFORM HOT-VIA

One of the key steps in the hot-via fabrication process is the backside via (BV) formation. The BV is etched from backside of the wafer to the frontside using ICP technique. The anisotropy of GaAs crystal influences longitudinal and transverse etching rates. The final shape of the hot-via is usually a trapezoidal platform. According to the data provided by the manufacturer, the Nanjing Electronic Devices Institute (NEDI), the finalized shape of a 35 μm square via in a 100 un thick GaAs wafer is a square trapezoidal platform, the side length of the upper and bottom squares is 35 μm and 75 μm, respectively.

Usually, the BVs are used as ground via in most MMIC designs and are simply modeled as a square cylinder, which neglects the change of via morphology caused by the etching process. In the hot-via application, the shape of the via model has significant influence on the RF performance, especially in millimeter wave band. A simulation is conducted to quantitatively analyze the influence of hot-via model shape.

In Fig. 1(a), the hot via is simply modeled as a square cylinder, of which the upper side is connected to the square pad and the bottom side connected to the ground. The pad is connected to simulation port with a 200 μm length micro-strip line. In Fig. 1(b), the hot via is modeled as a trapezoidal platform, and the rest of the simulation setup keeps the same as that for the model shown in Fig. 1(a).

The influence of the micro-strip line is deembedded using the port deembedding settings in the simulator, and the port plane is moved next to the edge of the pad. The S_{11} of preliminary simulation results goes up from the left endpoint along the circle in the Smith chart, which implies that the via can be represented as an inductor. Assume that the parasitic capacitance of the pad is negligible, the equivalent circuit is given in Fig. 1(c). The inductance is extracted from Y parameter Y_{11} of the simulation results using the following formula:

$$\text{imag}\,(Y_{11}) = -\frac{1}{\omega \cdot L\_via} \tag{1}$$

ω is the angular frequency, and L_via is the equivalent inductance of the via.

The extracted inductances of the square cylinder model and trapezoidal platform model are plotted in Fig. 2 for comparison. The inductance of the former is about 37 pH, and the curve rises after 80 GHz. The inductance of the latter is about 27 pH, and the curve keeps almost steady with the increase of the frequency. The difference in inductance of the two via models is about 10 pH for frequency below 80 GHz, and it increases obviously when frequency goes beyond 80 GHz, which leads to apparent RF performance discrepancy in frequency band higher than 80 GHz. Therefore, the via should be modeled as a trapezoidal platform to ensure the simulation accuracy of hot-via chip-to-substrate interconnect.

3. DESIGN AND SIMULATION OF CHIP-TO-SUBSTRATE INTERCONNECT

The SIP technology integrates several different chips in a small, compact package, while maintains good RF performance. Fig. 3 shows the diagram of a simple SIP configuration, where the RF signal flow trace within the package is also sketched. The RF signal is fed in one of the chips (such as amplifier MMIC), through which it is transferred to a silicon substrate, and then transmitted along a transmission line to the following chip. The key factor that affects RF performance in this kind of package is the

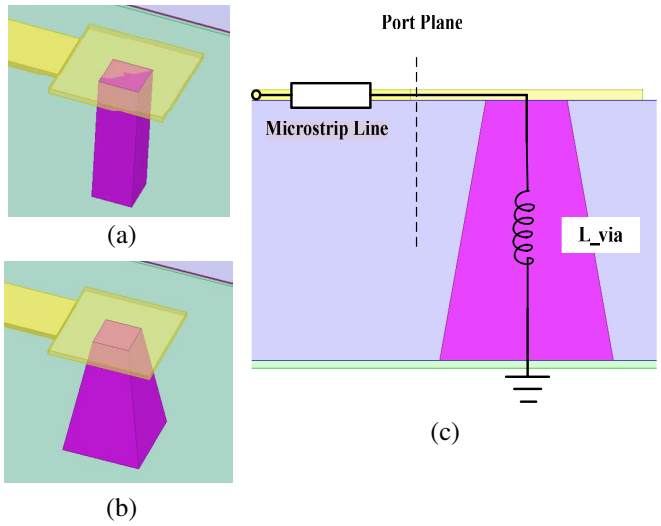

Figure 1. The via models with different shapes and the equivalent circuit. (a) Square cylinder model. (b) Trapezoidal platform model. (c) Equivalent circuit.

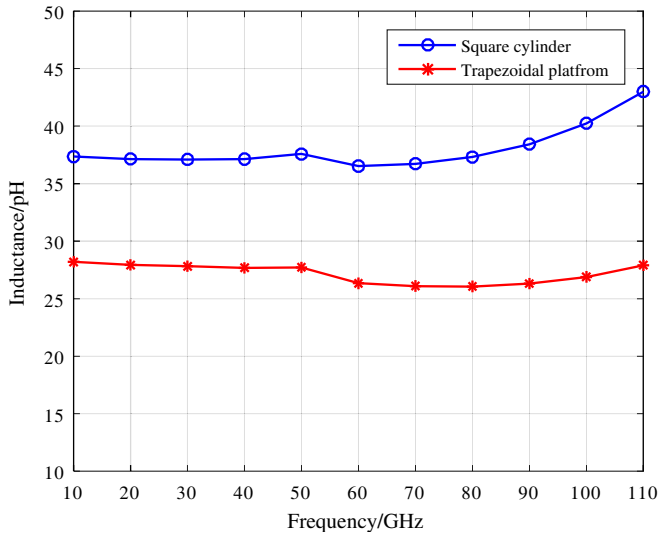

Figure 2. The inductance of the via models with different shapes.

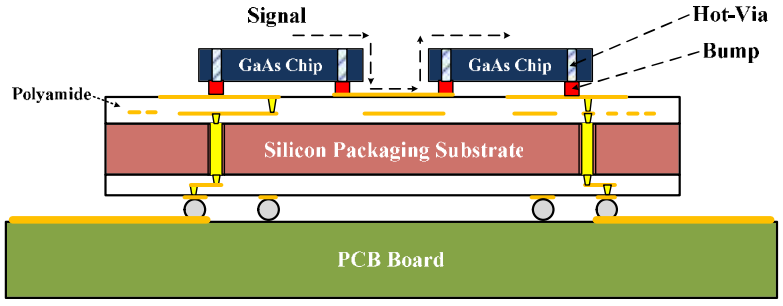

Figure 3. System in package diagram with hot-via interconnects.

interconnect between the chip and the silicon packaging substrate. In this paper, a hot-via chip-to-substrate interconnect at W-band is designed to improve RF transmission performance of traditional connection method such as wire-bonding.

The hot-via chip-to-substrate interconnect is divided into two parts, as shown in Fig. 4. One part is the hot-via vertical transition in the GaAs chip, which consists of the hot-via vertical transition in the chip and the port on the chip backside. The other part is the impedance matching structure on the silicon substrate, which consists of signal bumps and an impedance matching structure. These two parts are designed separately to simplify the design process.

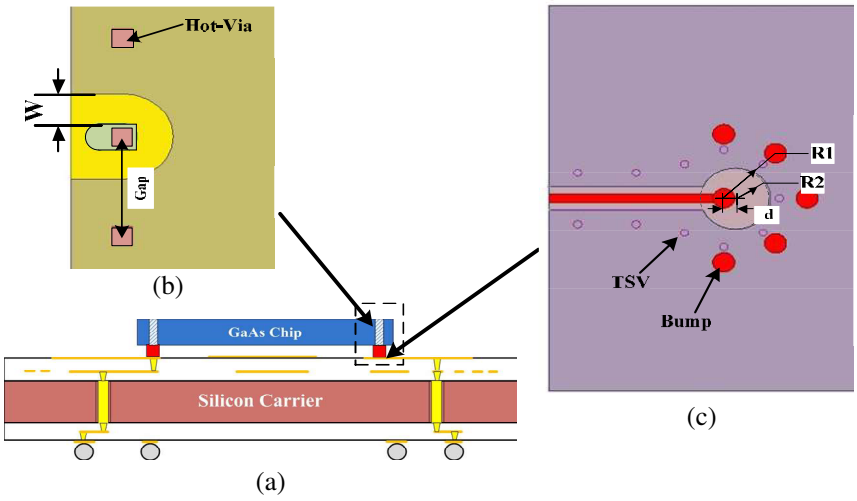

Figure 4. Hot-via chip-to-substrate interconnect structure of this work. (a) Diagram of the interconnect structure. (b) The bottom side of the chip. (c) The match structure on the substrate.

As shown in Fig. 4(b), the RF signal is transmitted from the top side to the bottom side through the three hot-vias in the chip. The hot-via in the middle connects the signal line with the pad on the bottom, and the other two hot-vias connect the ground. These hot-vias form a GSG vertical transition structure. The parameter *Gap*, which is the distance from the centre of the signal via to the centre of the ground via, determines the characteristic impedance.

The design of the port on chip backside is restricted by design rules of the hot-via. According to the rules provided by the manufacturer NEDI, the minimal side length of the pad on the backside is 100 µm. Hot-via must be placed within the pad, and the space between the edge of the hot-via and the pad is 32.5 µm. The minimal size of the gap, designated as W in Fig. 4(a), between the backside metal of the signal pad and that of the ground is 50 µm, and the maximum gap is 150 µm. As shown in Fig. 4(b), a 100 µm × 100 µm square pad is placed right under the signal hot-via, which is the minimal size allowed by the design rule to reduce parasitic capacitance. Since the bump cannot be placed right under the hot-via, a 100 µm diameter circle pad is designed and placed next to the square pad. These two pads are connected by backside metal. A street is cut off between the signal pad and the ground. The street open size W has significant impact on the RF performance, which needs to be carefully adjusted to get the best performance.

The bumps are fabricated on the silicon substrate using electroplating process. Compared with the bonding wire technology, the bump is much better in consistency and smaller in size. As shown in Fig. 4(c), the bumps form a quasi-coaxial structure. The signal bump is posted in the middle, and the ground bumps are posted around it on a half circle with a radius $R1$ which needs to be carefully adjusted. The ground around the signal bump is cut off as an eccentric open circle with a radius $R2$. The deviation distance between the center of the eccentric open circle and the center of the bumps is about length d. Usually, the hot-vias and bumps are inductive. Reducing the radius $R2$ and increasing the derivation d can make the eccentric circle structure more capacitive, which further compensates the inductive effect and improves the RF performance. The introduction of an eccentric open circle on the

ground avoids using a quarter matching line, which can significantly reduce the size of the interconnect structure.

To clarify the RF performance, the designed chip-to-substrate interconnect is characterized using a 3-D electromagnetic (EM) model, as shown in Fig. 5(a). Because the working frequency is up to W-band, several details of the manufacturing process are taken into consideration, as shown in Fig. 5(b). As mentioned in Section 2, the square hot-vias are etched from backside to the topside of the chip, whose top side length L_1 is smaller than the bottom side length L_2. Therefore, the hot-via here is modeled as a trapezoidal platform. The bump is modeled as a cylinder, whose height H_3 is the sum of the bump and the Sn-Ag solder cap. As shown in Fig. 5(c), the simulated transmission loss is less than 1.5 dB, and the return loss is better than 10 dB from 88 GHz to 100 GHz.

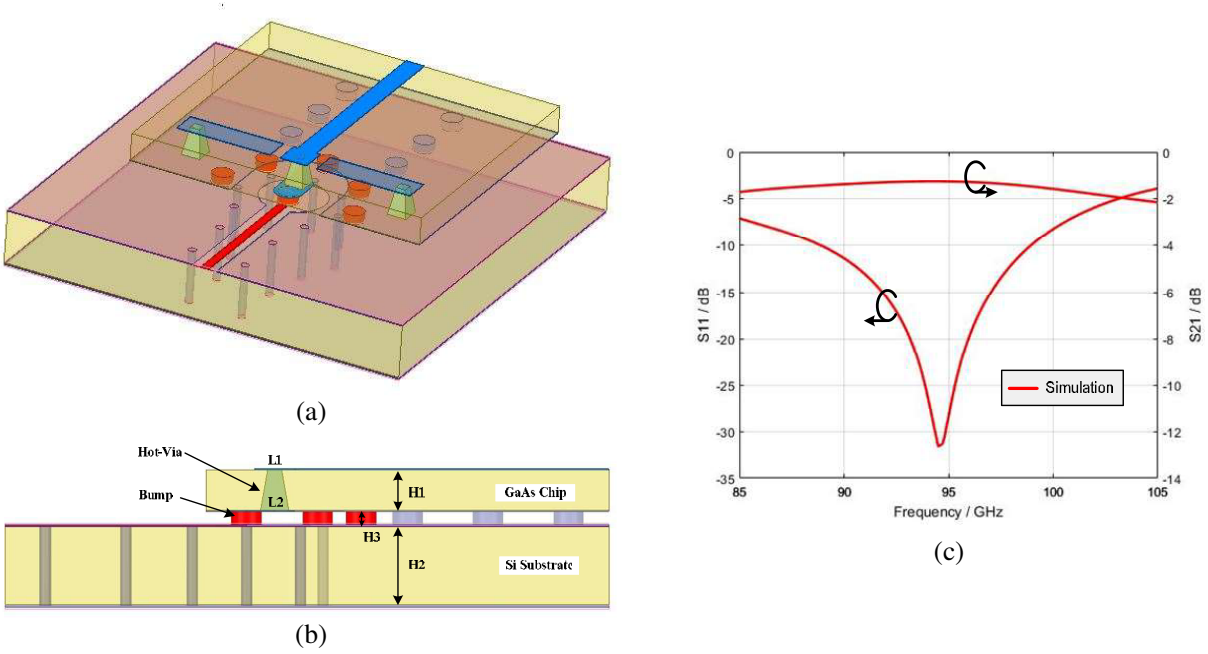

Figure 5. EM view of the hot-via chip-to-substrate interconnect structure and the simulation results. (a) Main view. (b) Side view. (c) Simulation results.

4. FABRICATION AND MEASUREMENT

The demo chip was fabricated in a 4-inch GaAs pHEMT process with an additional backside process by NEDI. The vias were etched from backside of the wafer to the topside. The finalized shape of the via is a trapezoidal platform, whose topside length L_1 is 35 µm, and backside length L_2 is 75 µm. The minimum line width/space that can be fabricated is 20 µm/50 µm. The thickness of the demo chip H_1 is 100 µm. The demo chip consists of a 50 Ω transmission line and two hot-via transitions on the edge, as shown in Fig. 6(a). The signal pads were electroplated on the backside of the demo chip and posted on both sides, as shown in Fig. 6(b). The silicon substrate was fabricated in a 8-inch passive Si process with bump process by NEDI, as shown in Fig. 6(c). The thickness of the silicon substrate H_2 is 200 µm. The bump is electroplated with copper, and the cap is chemical plated with Sn-Ag solder. The total height H_3 is about 20 µm.

For performance evaluation, the demo chip was assembled on the silicon substrate, as shown in Fig. 7. Using the pad on the back side of the GaAs chip and the signal bump on silicon substrate as the alignment mark, the demo chip and silicon substrate were picked up and placed together with advanced mounter. The mounting precision for the fine pitch component can be controlled within 5 µm. Then, the test sample was welded by a reflow soldering process.

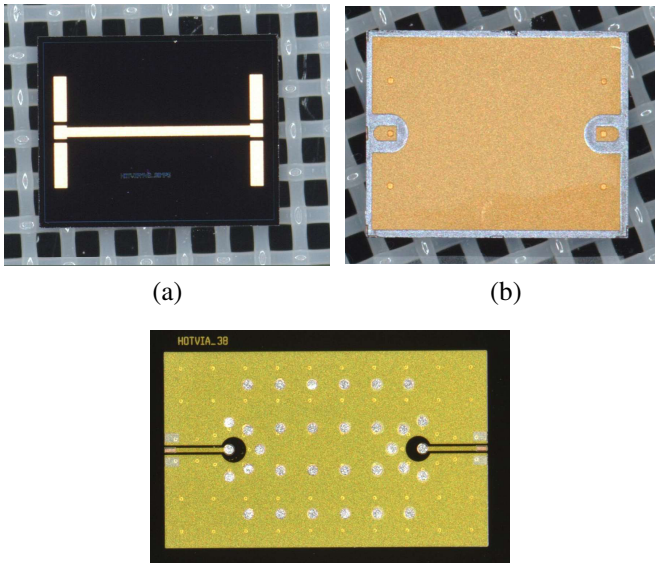

Figure 6. Microscope image of the fabricated demo chip and silicon substrate. (a) Front side. (b) Back side. (c) Silicon substrate.

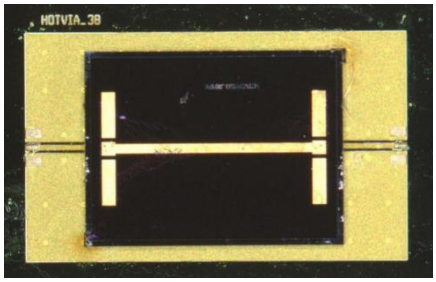

Figure 7. Microscope image of the assembled test sample.

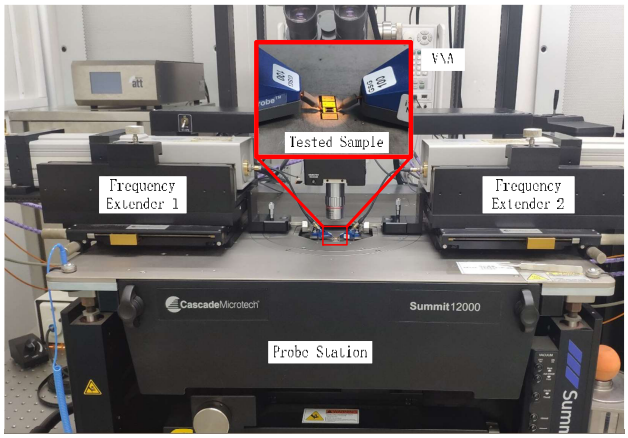

Figure 8. Picture of the test environments and the test sample.

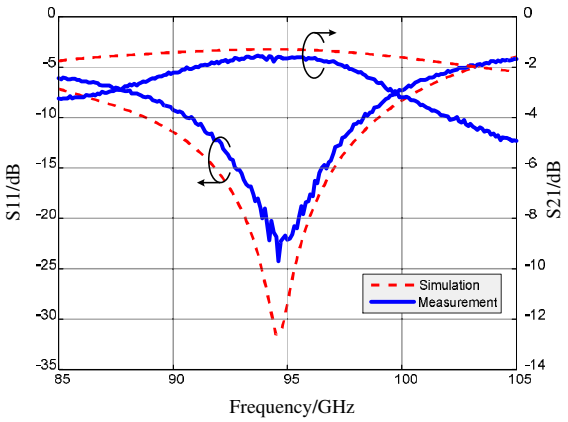

Figure 9. Comparison of the measured performance and the simulation performance.

As shown in Fig. 8, the test sample was measured by the cascade on-wafer probing measurement system using 100 µm spacing GSG probes. The scattering parameters were characterized by the vector network analyzer (VNA) Keysight N5247A with frequency extenders Keysight N5250C. Fig. 9 shows the measurement results of the test sample where the EM-simulation results are also given for comparison. It is shown that the measured overall transmission loss is less than 1.85 dB with 1 dB bandwidth being 10 GHz, and return loss is better than 12 dB from 92 GHz to 96 GHz.

5. CONCLUSION

The design and optimization process of a hot-via chip-to-substrate interconnect at W-band is presented. Details of the via etching process are taken into consideration, and a trapezoidal platform model is adopted for the hot-via modeling, which can significantly improve the simulation accuracy. The structural parameters of the hot-via vertical transition in the GaAs chip and the matching structure on the silicon substrate are optimized. In particular, an eccentric open circle on the ground is designed to reduce the size of the matching structure. The proposed hot-via chip-to-substrate interconnect features compact size and low insertion loss, and it is suitable for system in package application in shorter millimeter-wave bands.

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