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Highly Flexible Uniplanar Dual-Band Power Divider for Arbitrary Source and Load Impedances

Rahul Gupta[1], Maher Assaad[2], and Mohammad Hashmi[3, *]

Abstract—In this paper, a dual-band impedance transforming power divider is investigated for all types of impedance environments at its ports, irrespective of the locations of the ports. The intuitive design approach utilizes conventional single-band Wilkinson Power Divider (WPD) architecture to provide superior dual-band performance with arbitrary port impedances. The proposed power divider also accords a high degree of design flexibility with high frequency ratios (r) and impedance transformation ratios (k). The presented concept is evaluated and verified by design examples and measurements with a fabricated prototype. The agreement between the simulation and measurement results validates the working of the proposed architecture with arbitrary source and load port impedances at two arbitrary design frequencies.

1. INTRODUCTION

Wlkinson Power Divider (WPD) is a conventional power divider for power division and combination purposes [1]. The power divider utilizes a quarter-wavelength transmission line (TL) for impedance matching purposes in the even-mode analysis [2]. However, this quarter wavelength TL only provides the impedance transformation for the real ports Z_0 at a single frequency only. Similar impedance transformation is explored with modified WPD architectures; however, it is noticed that most of them are limited with the real ports only [3–7]. There are some recent architectures that discuss the impedance transformation for complex impedances [8–12]. However, the concurrent power dividers at two arbitrary frequencies with arbitrary frequency-dependent complex impedances at the ports are rare.

In this paper, a dual-band frequency-dependent complex impedance transforming power divider (ITPD) is proposed for the variety of antennas developed for various applications. The contribution is further enhanced by providing the intuitive design approach which improves the design flexibility. The significant contributions of the proposed PD are: 1) enhanced design flexibility for any impedance environment at the ports; 2) either source or load or both terminations can be frequency-dependent complex loads (FDCLs); and 3) a simple and planar microstrip architecture. The proposed architecture eliminates the need to design complex impedance matching circuits for the interconnection purposes between PD and other circuits of a communication system. For example, the ports of the proposed PD can directly be utilized as the feed-line for an antenna having arbitrary impedance at two distinct frequencies of interest.

2. DESIGN METHODOLOGY

The conventional WPD provides the power division for real port terminations at a single frequency of operation only [1]. A TL exhibits complex conjugate input impedances at two arbitrary frequencies, i.e.,

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* Corresponding author: Mohammad Hashmi (mohammad.hashmi@nu.edu.kz).

[1] Department of ECE, IIIT-Delhi, New Delhi, India. [2] Electrical Engineering, Ajman University, Ajman, UAE. [3] School of Engineering and Digital Sciences, Nazarbayev University, Kazakhstan.

θ and $r\theta$, if its electrical length (θ) follows Eq. (1). This property is commonly utilized for dual-band performances [13–15].

$$\theta = \frac{(1+n)\pi}{1+r}; \quad n \in I. \tag{1}$$

Further, a TL can transform an FDCL to complex conjugate impedance [16]. Therefore, as depicted in Fig. 1, a TL with parameters Z_{a1}, θ_{a1} (Z_{b1}, θ_{b1}) is added at the input (output) port of the conventional WPD. Here, the characteristic impedances and electrical lengths of TLs are denoted by the corresponding Z and θ, respectively. The frequency-dependent complex impedances at source (Z_S) and load (Z_L) ports of WPD are defined as Eqs. (2) and (3), respectively, at the two operating frequencies. Since the circuit is symmetric around the dotted axis, the even-odd mode analysis is utilized for further discussion. In the odd-mode equivalent circuit of conventional WPD, depicted in Fig. 2(a), the TL Z_{b1}, θ_{b1} transforms the FDCL Z_L into a complex conjugate admittance Y_{ib1}.

$$Z_S = \begin{cases} R_{S1} + jX_{S1} \ @f_1 \\ R_{S2} + jX_{S2} \ @f_2 \end{cases} \tag{2}$$

$$Z_L = \begin{cases} R_{L1} + jX_{L1} \ @f_1 \\ R_{L2} + jX_{L2} \ @f_2 \end{cases} \tag{3}$$

The configuration is left with a TL with design parameters Z_X, θ, and a resistor $R/2$ to attain the required impedance matching between Y_{ib1} and Y_{iy}. The matching conditions in Eq. (4) yield the solutions for Z_X and R. The electrical length for the dual-band operation can be computed from

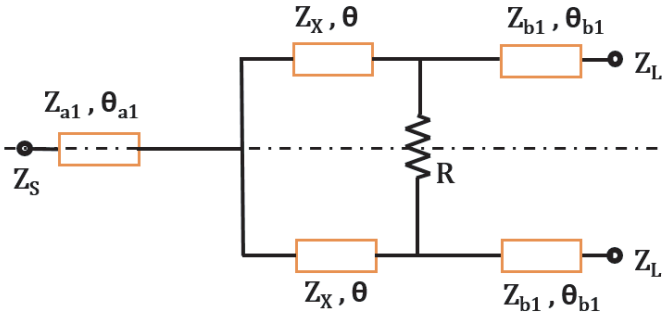

Figure 1. Conventional Wilkinson Power Divider with port extensions.

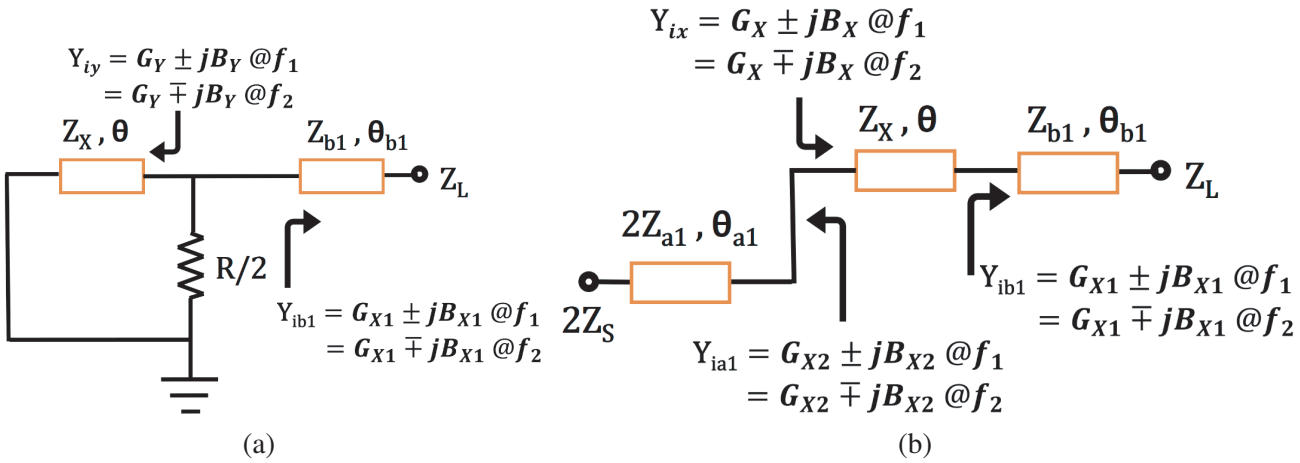

Figure 2. (a) Odd-mode and (b) Even-mode equivalent circuit of the conventional WPD with port extension.

Eq. (1). Moreover, it should be noted that impedance transformation is required in the odd- and even-mode analysis of the PD. Similar to odd-mode analysis, the even-mode equivalent circuit, depicted in Fig. 2(b), utilizes TL with characteristic impedance $2Z_{a1}$ to transform $2Z_S$ into complex conjugate impedance Y_{ia1}. The remaining design parameters Z_X and θ are already calculated in the odd-mode analysis to a fixed value, and therefore, the required impedance matching stated in Eq. (5) cannot be obtained (due to the unavailability of any undefined design parameter).

$$\begin{cases} G_{X1} = G_Y \\ B_{X1} = -B_Y \end{cases} \tag{4}$$

$$\begin{cases} G_{X2} = G_X \\ B_{X2} = -B_X \end{cases} \tag{5}$$

3. PROPOSED DESIGN OF DUAL-BAND POWER DIVIDER

This limitation is addressed further by using the combination of a TL and a short-/open-circuited shunt stub in series at the "//" marked locations as depicted in Fig. 3. The proposed dual-band impedance transforming power divider (DBITPD) enhances the design flexibility highly while keeping the structure compact for a wide range (and variety) of the real, complex, and frequency-dependent complex impedances between the input and output ports. This is due to three reasons: a) the choice of using a TL of the L-type network at either source or load or both; b) the choice of using the stub of the L-type network while the stub has the flexibility of being an open-/short-circuited stub; and c) the choice of using full L-network at either source or load or both. Due to the added TLs and stubs, these additional design parameters provide enhanced freedom to get the realizable design parameters. The proposed architecture is symmetric about the dotted axis, as depicted in Fig. 3, and therefore, the simplified even-odd mode analysis is utilized for the design analysis.

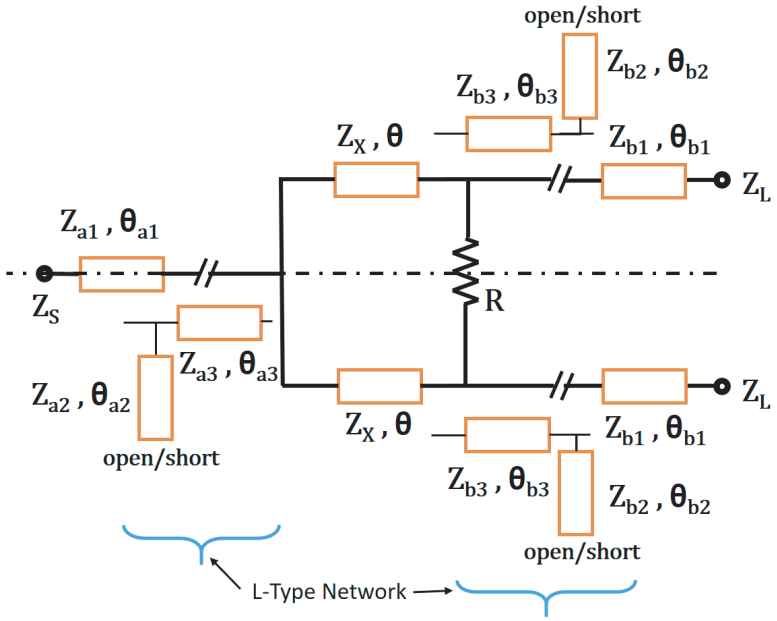

Figure 3. Schematics of the proposed DBIT Power Divider.

3.1. Odd-mode Analysis

The odd-mode equivalent circuit of the proposed architecture is depicted in Fig. 4(a). The term Z_{b1} can be computed following [16] to transform the FDCL load Z_L into a complex conjugate admittance

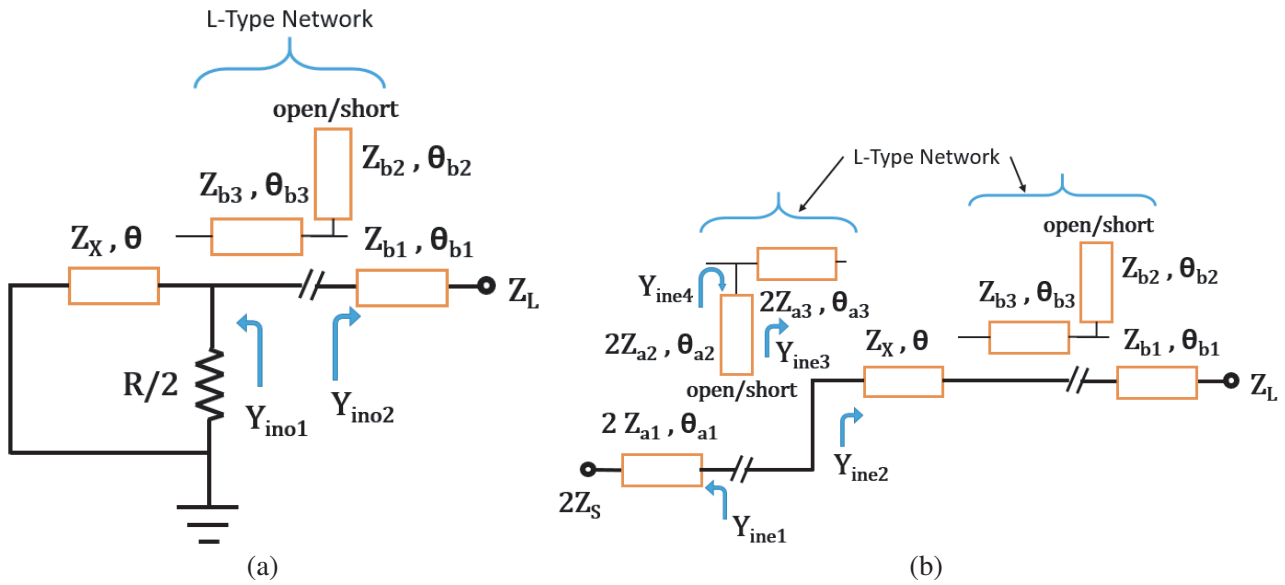

Figure 4. (a) Odd-mode and (b) Even-mode equivalent circuit of the proposed DBIT Power Divider.

Y_{ino2}. The admittance Y_{ino1} can be expressed as Eq. (6). Here, the design parameters Z_X and R are used as independent variables which provide high flexibility to the odd-mode equivalent circuit for the required impedance matching.

$$Y_{ino1} = \frac{1}{(R/2)} + \frac{1}{(jZ_X \tan\theta)} \tag{6}$$

Owing to the wide range of Z_X and R, the use of L-network can be omitted here for several cases to keep the design compact. However, the use of L-network may provides the impedance matching to wide range of port impedances owing to the choice of short-/open-circuited stub. The design parameters of the L-network are derived in the next subsection (even-mode analysis) and can be followed here with a similar approach [17]. The electrical length of the TL and stubs follows Eq. (1) for the dual-band performance. The extreme impedance ranges of the microstrip TLs are considered as 20 Ω and 150 Ω.

3.2. Even-Mode Analysis

The even-mode equivalent circuit of the proposed architecture is depicted in Fig. 4(b). Again, the term Z_{a1} can be computed following [16] to transform the FDCL source $2Z_S$ into a complex conjugate admittance Y_{ine1} ($= G_{ine1} + jB_{ine1}$). The admittance Y_{ine2} is also a complex conjugate entity consisting of all the known design parameters derived in the odd-mode analysis.

Now, the L-type network can be utilized to obtain the required impedance matching. If Y_{ine2} can be written as Eq. (7), the input admittance Y_{ine3} can be expressed as Eq. (8) following the TL theory. Here, θ_{a3} is kept equal to θ for simplification.

$$Y_{ine2} = G_{ine2} + jB_{ine2} \tag{7}$$

$$Y_{ine3} = G_{ine3} + jB_{ine3} \tag{8}$$

Here,

$$G_{ine3} = \frac{G_{ine2}\left(1+\tan^2\theta\right)}{G_{ine2}^2 + \left(B_{ine2} + 2Z_{a3}\tan\theta\right)^2} \tag{9}$$

$$B_{ine3} = \frac{\left(\frac{1}{2Z_{a3}}\right)\left[\left(G_{ine2}^2 + B_{ine2}^2\right)\tan\theta - 4Z_{a3}^2\tan\theta - 2Z_{a3}B_{ine2}\left(1-\tan^2\theta\right)\right]}{G_{ine2}^2 + \left(B_{ine2} + 2Z_{a3}\tan\theta\right)^2} \tag{10}$$

Now, the real part of Y_{ine1} must be equal to G_{ine3} for the required impedance matching. This results in the expression of Z_{a3}, mentioned in Eq. (11).

$$Z_{a3} = \frac{-4G_{ine1}B_{ine2}\tan\theta \pm \sqrt{16G_{ine1}^2B_{ine2}^2\tan^2\theta - 16G_{ine1}\tan^2\theta\left[G_{ine1}B_{ine2}^2 - G_{ine2}\left(1+\tan^2\theta\right)\right]}}{8G_{ine1}\tan^2\theta} \quad (11)$$

Subsequently, the effective imaginary part must be canceled using the open-/short-circuited stub of the L-type network. The characteristic impedance Z_{a2} and electrical length θ_{a2} of the stub can be calculated as mentioned in Eqs. (12) and (13), respectively.

$$\begin{aligned} Z_{a2} &= -\frac{\tan\theta_{a2}}{B_{ine1}+B_{ine3}} \quad \text{for open condition} \\ Z_{a2} &= +\frac{\cot\theta_{a2}}{B_{ine1}+B_{ine3}} \quad \text{for short condition} \end{aligned} \quad (12)$$

$$\theta_{a2} = \frac{(1+n)\pi}{1+r} \quad (13)$$

4. DESIGN PROCEDURE AND FURTHER INVESTIGATIONS

4.1. Design Procedure

The design of the proposed DBITPD for the arbitrary impedances is summarized below.

(i) Based on the design specifications, calculate r.

(ii) Calculate Z_{a1} and θ_{a1} to transform the source impedance into complex conjugate impedance (Y_{ine1}) [16]. Similarly, calculate Z_{b1} and θ_{b1} to transform the load impedance to complex conjugate Y_{ino2}.

(iii) In the odd-mode analysis, the design parameter Z_X and R can be independently chosen within the available/realizable limits.

(iv) If needed, additional sections of L-type network can be utilized and calculated [17]. Here, θ_{b2} and θ_{b3} must follow Eq. (1) with independent choice of n. It should be noted that n should be kept "0" for the miniaturized structure.

(v) Thereafter, in the even-mode analysis, addition of TLs (either only Z_{a2}, θ_{a2} or only Z_{a3} θ_{a3} or both) should be opted for the required impedance matching. Considering the full L-type network, the design parameters Z_{a3} and θ_{a3} can be calculated using Eqs. (11) and (1), respectively.

(vi) Subsequently, Z_{a2} and θ_{a2} can be calculated using Eqs. (12) and (13), respectively.

(vii) In case that there is no realizable solution, the selection of the TLs in step (iv) can be revisited. Furthermore, the selection of n and open- or short-circuited stubs should be tweaked to obtain the realizable design parameters.

To highlight the design flexibility, three different design examples with arbitrary frequency-dependent complex impedances and frequency ratios are listed in Table 1. All the cases represent the arbitrary design specifications with FDCL impedances at both the input and output ports for either power division or combination purposes. The load values are synthesized based on the combination of the TL sections and SMA port. Moreover, the proposed ITPD is suitable for any type of port impedance, either real or complex or frequency-dependent complex impedance.

5. EXPERIMENTAL VALIDATION

To experimentally verify the proposed design technique, case-2 of the design examples is fabricated on an RT/Duroid 5880 substrate with thickness 1.58 mm, $\epsilon_r = 2.2$, $\tan\delta = 0.0009$, and copper laminates thickness 35 µm on both the sides. An isolation resistor with part No. CRCW0603200RFKTA is soldered. To generate 50 Ω impedance environment for the measurement purposes, the input and output ports are synthesized with 50 Ω SMA ports. The fabricated PD, with dimensions 69.85 mm × 74.5 mm

Table 1. Design examples of the proposed DBITPD for distinct specifications. Here, $f_1 = 1\,\text{GHz}$.

Design Parameters	**Case-1** ($\mathbf{r = 3.0}$)	**Case-2** ($\mathbf{r = 3.5}$)	**Case-3** ($\mathbf{r = 6}$)
$Z_S\Omega$ @f_1 GHz	$12.4 + j3.85$	$36.45 - j10.55$	$12.4 + j3.85$
$Z_S\Omega$ @f_2 GHz	$89.5 + j17.3$	$42.89 + j10.11$	$89.5 + j17.3$
$Z_L\Omega$ @f_1 GHz	$9.58 - j11.136$	$153.1 + j59.55$	$154.8 + j26.42$
$Z_L\Omega$ @f_2 GHz	$8.95 - j0.15$	$164.71 + j50.78$	$93.6 + j38.1$
$Z_{a1}\Omega, \theta^\circ_{a1}$	32.25, 66.87	37.28, 36.55	33.77, 38.16
$Z_{a2}\Omega, \theta^\circ_{a2}$	125, 45 (Open-circuited)	124.48, 120 (Open-circuited)	91.1, 77.14 (Open-circuited)
$Z_{a3}\Omega, \theta^\circ$	35.8, 45	21.05, 40	33.4, 25.71
$Z_x\Omega, \theta^\circ$	100, 45	110.27, 40	100, 25.71
$Z_{b1}\Omega, \theta^\circ_{b1}$	42.97, 48.85	95.45, 46.44	109, 34.69
$Z_{b2}\Omega, \theta^\circ_{b2}$	33.39, 45 (Open-circuited)	106.85, 160 (Open-circuited)	53.3, 25.71 (Open-circuited)
$Z_{b3}\Omega, \theta^\circ$	43.1, 45	83.18, 40	77.265, 25.71
$R\Omega$	100	200	100

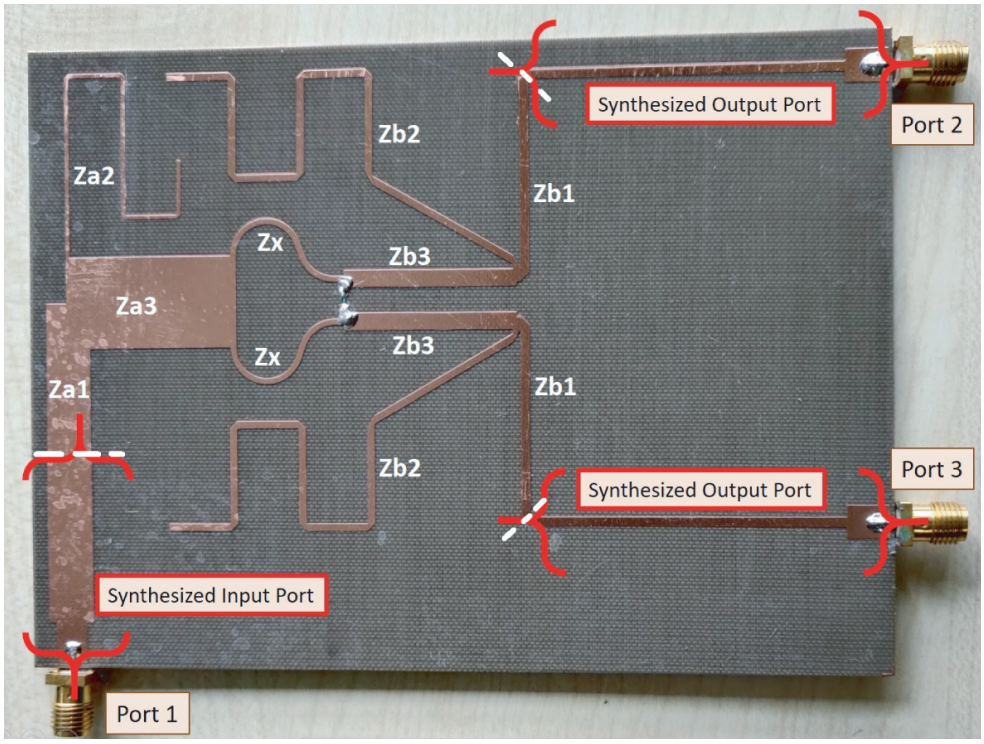

Figure 5. The fabricated prototype with FDCL port terminations. The synthesized ports are not the part of the circuit and are used for the measurement purposes only.

excluding the synthesized ports, is shown in Fig. 5, with respective characteristics impedances for reference.

The measurement results, depicted in Fig. 6, are in good agreement with the electromagnetic (EM) simulation results and thus validate the proposed concept and design procedure. Moreover, the additional resonances can be observed in Fig. 6 which are available due to the harmonics generated by the short-/open-circuited stubs dominantly. The other factors affecting the performance including slight shift in the isolation response at 3.5 GHz are the TL discontinuities and in-house fabrication errors such as fabrication tolerances and soldering errors. The additional resonances between the operating frequencies can be suppressed through the harmonic suppression techniques [18].

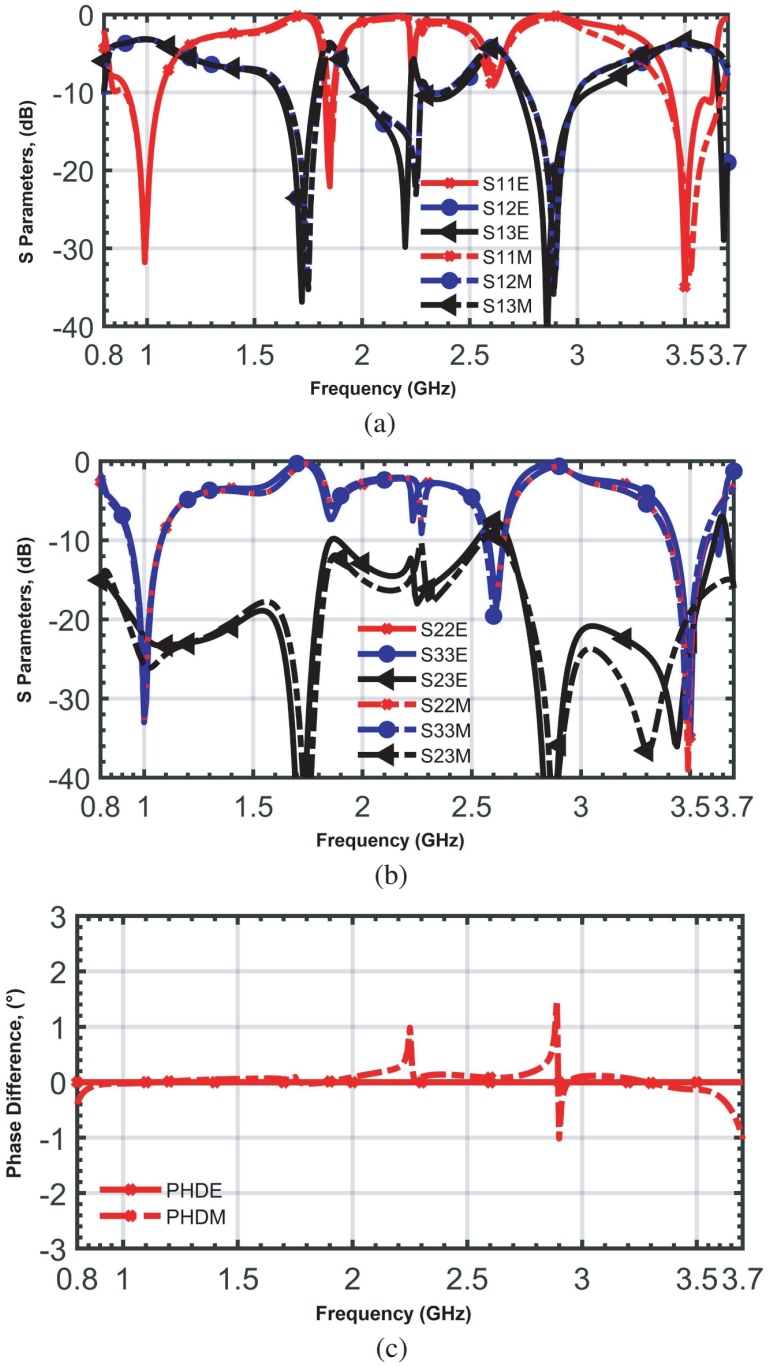

Figure 6. Comparison of the measured (M) and EM simulated (E) results for the proposed PD. (a) Input port matching and insertion losses. (b) Output ports matching and isolation between these ports. (c) Phase difference (PHD).

Also, the circuit performance and features are compared with the recent impedance transforming power dividers in Table 2. While the performance is comparable, the proposed PD is capable of providing the inherent impedance transformation to all the real, complex, and FDCL loads irrespective of the source or load port which is not present in the compared designs. The dimension of the proposed PD, excluding the redundant port transformations, is also compared and found compact. The bandwidth performance of the proposed DBITPD is suitable for various applications at FR1 frequency bands of the 5G communication systems. Overall, the PD works well at the designed frequencies for the arbitrary impedances at both the source and load ports.

Table 2. Comparison with recent impedance transforming power dividers [FBW: Fractional bandwidth].

Refs.	Operating Frequency	No. of Bands	Port Impedance	S_{11} (dB) at f_1, f_2	FBW (%) at f_1, f_2	Size (λ_g^2)
[19]	1.0/1.8	dual	real	-21, -34	15.4, 5.2	NA
[15]	1, 5	dual	real	-29, -21	11, 12	0.175
[20]	0.7, 2.6	dual	real	< -15	24.3, 8.1	0.34
[This Work]	1, 3.5	dual	real, complex and FDCL	-31.8, -27.9	16 and 13.1	0.092

6. CONCLUSIONS

In this paper, an impedance transforming dual-band power divider/combiner has been investigated. The design is capable of addressing the arbitrary impedance environments at two arbitrary frequencies at both the source and load ports. The design examples validate the design flexibility by providing realizable design parameters. A prototype with arbitrary FDCL terminations at widely separated design frequencies is fabricated, and the agreement between the simulation and measurement results has demonstrated the effectiveness of the proposed circuit. The successful validation demonstrates the potential to fill the void in the state-of-the-art designs for arbitrary port impedances.

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