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# A Q-Band Current-Reused Low Noise Amplifier with Simultaneous Noise and Input Matching

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**Abstract**—In this paper, a Q-band GaAs low noise amplifier (LNA) for satellite communications is presented. The LNA is designed using common-source (CS) topology, self-biased configuration, and current-reused technology. Simultaneous noise and input matching are achieved by employing source series inductance. The current-reused LNA is fabricated in a 90 nm GaAs pseudomorphic high electron mobility transistor (pHEMT) process. On-wafer measurement results show that the LNA features a small-signal gain of $23.8 \sim 24.5$ dB, noise figure (NF) of $2 \sim 2.1$ dB, and output 1-dB compression point (OP1 dB) of $6.6 \sim 8$ dBm over $36 \sim 42$ GHz, while consuming 10.9 mA with a supply voltage of 5 V. The chip size is $1.6 \times 0.8\,\text{mm}^2$ including all RF and dc pads.

## 1. INTRODUCTION

As the first stage in a receiving chain, a low noise amplifier (LNA) is one of the most critical active components in the front-end receiver of any communication system [1–4]. Since the signal received at the input of a receiver is quite weak, the common goals in designing an LNA are to achieve low noise figure (NF), reasonable gain, high linearity, as well as low power consumption, and finally to expand the dynamic range and improve the sensitivity of a receiver system [5]. Most of these performance metrics are interdependent and trade with each other, which further introduces challenges to LNAs design.

In most practical applications, the optimum supply voltage of a transistor is usually much lower than that available at the system level [6]. In traditional cases, additional DC-DC conversion stages or resistive elements are used to drop a voltage, which has the drawbacks of more complex system architecture or more power consumption. Furthermore, for systems such as modern active phased array receivers where the number of LNAs can easily reach thousands, LNA power consumption considerations may be more important [7, 8]. To alleviate this problem, current-reused structure was proposed in the literature [9–13], namely increasing circuit voltage to be equal to that provided at the system level without changing the operating point of each transistor.

The paper is organized as follows. Section 2 presents a theoretical analysis of inductive source degeneration. The detailed circuit design and implementation issues are covered in Section 3. The proposed LNA is implemented in a 90 nm GaAs process. The measurement results and comparison to state-of-the-art are presented in Section 4. Finally, Section 5 draws some conclusions.

## 2. INDUCTIVE SOURCE DEGENERATION

In LNA configuration, resistive feedback is often adopted to guarantee gain flatness and stability [14]. The resistive feedback is composed of a series R-L-C circuit which is connected between the gate and drain of a transistor. Unfortunately, simultaneously good input and noise matching cannot be obtained

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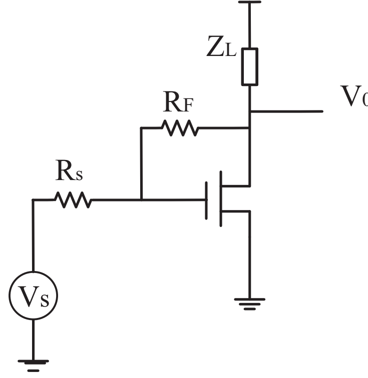


**Figure 1.** Schematic of a resistive feedback LNA.

with feedback configuration. To demonstrate that, let us consider a resistive feedback amplifier circuit shown in Figure 1.

The input impedance is given by

$$Z_{in} = \frac{R_F + Z_L}{1 + g_m Z_L} \tag{1}$$

Neglecting the gate and source parasitic resistance, the noise factor can be given by [15]

$$F \approx \left(1 + \frac{1}{(1 - g_m R_F)^2}\left(\left(\frac{R_F^2}{R_s}\right)\left(\frac{g_m}{2} + \frac{1}{R_F} + \frac{1}{Z_L}\right) + R_s\left(\frac{g_m}{2} + \frac{1}{Z_L} + \frac{(g_m R_F - 1)^2}{R_F}\right)\right)\right) \tag{2}$$

where $R_s$ is the $50\,\Omega$ source resistance.

As shown in Eqs. (1) and (2), the noise factor and input resistance are coupled, and they both depend on $R_F$ and $Z_L$. To achieve a low noise factor without scarifying input matching, inductive source degeneration was introduced to decouple the noise factor from the input impedance.

The input stage of the inductively source-degenerated CS transistor is illustrated in Figure 2. The input impedance can be given by [16]

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right) L_s \tag{3}$$

where $L_g$ and $L_s$ are the gate and source inductance; $g_{m1}$ is the transconductance; $C_{gs}$ represents the gate-source parasitic capacitor.

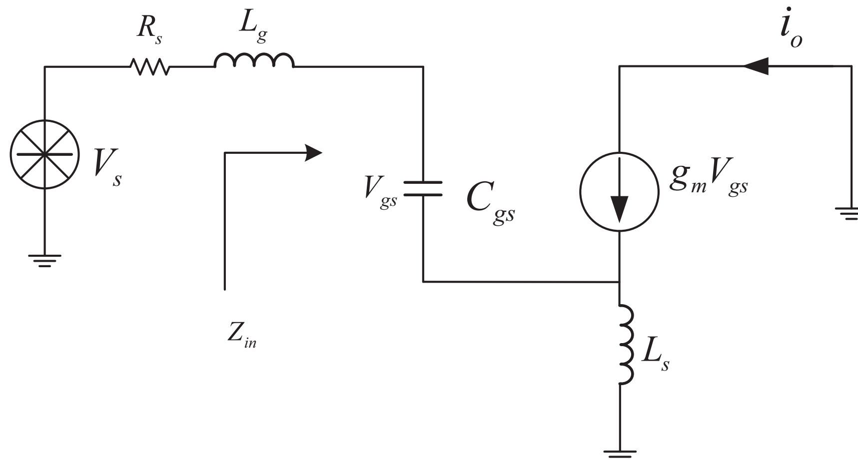


**Figure 2.** Small signal equivalent circuit for the inductively source-degenerated CS transistor.

At the series resonance of the input circuit, $s(L_s + L_g) + \frac{1}{sC_{gs}} = 0$. Resonance angular frequency $\omega_0 = 1/\sqrt{C_{gs}(L_g + L_s)}$. The input impedance is

$$Z_{in} = \left(\frac{g_{m1}}{C_{gs}}\right) L_s = \omega_T L_s \tag{4}$$

where $\omega_T$ is the unity gain frequency of the transistor.

As shown in Eq. (4), at the resonance angular frequency, the input impedance is purely real and proportional to $L_s$. Good input matching can be easily obtained by choosing appropriate $L_s$.

Noise factor of an LNA can be calculated by analysing the small-signal noise equivalent model, as shown in Figure 3. In the circuit, $R_s$ is the $50\,\Omega$ source resistance, $R_l$ the series resistance of the inductor $L_g$, $R_g$ the gate resistance of the CS transistor, and $\overline{i_{nd}^2}$ the channel thermal noise of the transistor. Three noise sources have been considered [17]: the thermal noise of the source resistance ($\overline{i_{n,R_s}^2}$), the gate-induced current noise ($\overline{i_{n,R_l,R_g}^2}$), and the thermal noise of the channel current ($\overline{i_{nd}^2}$).

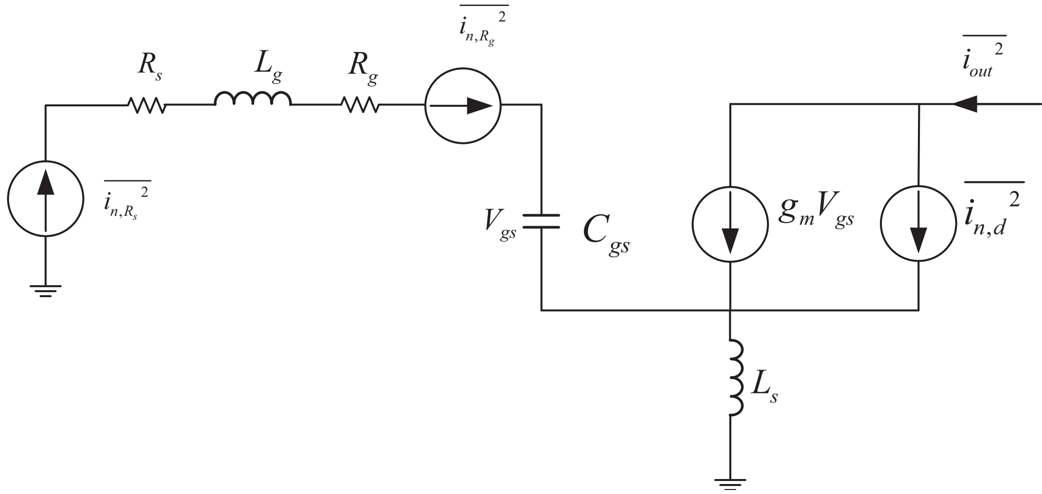


**Figure 3.** Small-signal equivalent model for noise calculation.

The output noise power density arising from the channel thermal noise of the device is

$$\overline{i_{out,nd}^2} = \frac{\overline{i_{n,d}^2}}{\left(1 + \frac{\omega_T L_s}{R_s}\right)^2} \tag{5}$$

The output noise power density due to the $50\,\Omega$ source is given by [18]

$$\overline{i_{n,R_s}^2} = |G_m|^2\,\overline{V_{n,R_s}^2} = \left|\frac{\omega_T}{j\omega_0(R_s + \omega_T L_s)}\right|^2 \cdot 4KTR_s = \frac{4KT\omega_T^2}{\omega_0^2 R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)^2} \tag{6}$$

The output noise power density due to $R_l$ and $R_g$ is

$$\overline{i_{n,R_l,R_g}^2} = \left|\frac{\omega_T}{j\omega_0(R_s + \omega_T L_s)}\right|^2 \cdot 4KT\,(R_l + R_g) = \frac{4KT\,(R_l + R_g)\,\omega_T^2}{\omega_0^2 R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)^2} \tag{7}$$

The total output noise power density is the sum of Eqs. (5)–(7).

$$F = 1 + \frac{\overline{i_{n,R_l,R_g}^2} + \overline{i_{out,nd}^2}}{\overline{i_{n,R_s}^2}} = 1 + \frac{R_l + R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{8}$$

where $g_{d0}$ is the zero-bias drain conductance.

As shown in Eq. (8), the dominant term of noise factor is the last term. Moreover, for a given resonance frequency $\omega_0$, the noise factor improves quadratically with the transistor unity gain frequency $\omega_T$. As shown in Eqs. (4) and (8), noise factor and input impedance are decoupled. It is noted that simultaneously input and noise matching can be obtained by introducing source inductor $L_s$. In this paper, source inductances are implemented via transmission lines to achieve a compact chip area at the cost of a little more insertion loss.

## 3. CIRCUIT DESIGN

### 3.1. Device Size and Bias Selection

Transistor selection is the first and most important step in designing an LNA [19]. The main design targets of the proposed LNA are a gain of 22 dB and the NF below 2.5 dB in the frequency band of 36 $\sim$ 40 GHz. Also, the output 1-dB compression point should be above 5 dBm. The LNA is designed using a 90 nm gate length pHEMT on a 70 µm GaAs substrate, and the cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{MAX}$) are 110 and 380 GHz. It includes 2 sets of metal layers, air bridges, MIM capacitors with SiN dielectric material, NiCr and GaAs resistors, and via-hole components. The minimum NF at 40 GHz is 1.39 dB. The device with four fingers and 25 µm gate width is chosen for each unit amplifying stage. The biasing point is chosen with 20% of $I_{dss}$ to obtain noise figure and low power consumption, as shown in Figure 4. The bias point of each transistor is VDS = 1.5 V and IDS = 11 mA at VGS = −0.5 V.

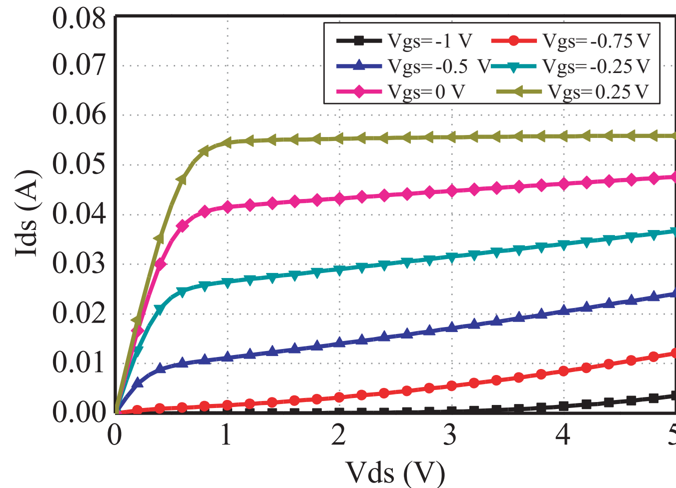


**Figure 4.** I-V characteristics of a transistor (4 × 25 µm).

### 3.2. Current-Reused Configuration

As shown in Figure 5, a current-reused configuration is utilized to guarantee lower power dissipation. The dc current flows from the drain of $Q_3$ to the drain of $Q_1$ by the single power supply $V_{dd}$ which is operated at 5 V. The dc bias voltage drops from the drain of $Q_3$ to the drain of $Q_1$. The amplified drain ports of $Q_1$ and $Q_2$ are connected to the gates of $Q_2$ and $Q_3$ with coupling capacitors $C_{g2}$ and $C_{g3}$. The capacitors $C_{s1}$ and $C_{s2}$ are added for RF-bypassed paths for $Q_1$ and $Q_2$, and prevent the dc current flowing into the ground. All choke inductors and by-pass capacitors are also utilized for impedance matching. All three transistors share the same dc current and operate as common-source amplifiers in a cascaded connection. The drain voltages of $Q_3$, $Q_2$, $Q_1$ are operated at 5 V, 3.5 V, 2 V, respectively. The voltage between drain and source $V_{ds}$ and the voltage between gate and source $V_{gs}$ of each transistor are 1.5 V and −0.5 V, respectively.

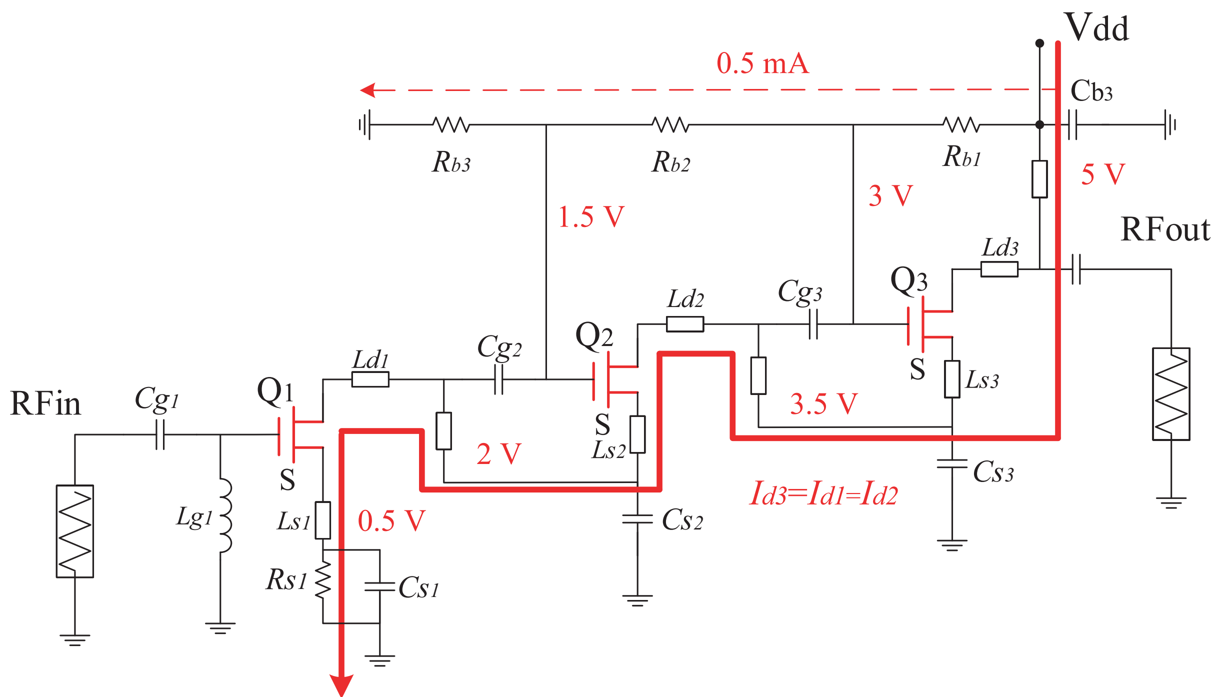


**Figure 5.** Overall schematic of the proposed LNA.

### 3.3. Self-Bias Structure

For a depletion mode technology, negative gate voltages are required to drive the transistor working at saturate region, which brings inconvenience in the application. A self-biased topology [20] was proposed by inserting a parallel RC structure between the source inductor and ground, as shown in Figure 6. The resistor, in which drain current flows, was sized to provide the selected positive dc voltages at the source terminal. Thus, fixing to zero the voltage at the gate terminal with a dc path to the ground, any required negative gate-source voltage $V_{gs}$ could be obtained. It is expressed as follows:

$$V_{gs} = V_g - V_s = -V_s = -I_d R_s \tag{9}$$

Moreover, a shunt capacitor was used to provide a direct path to the ground to the RF signal, reducing the detrimental effects of the resistors on gain and noise performance.

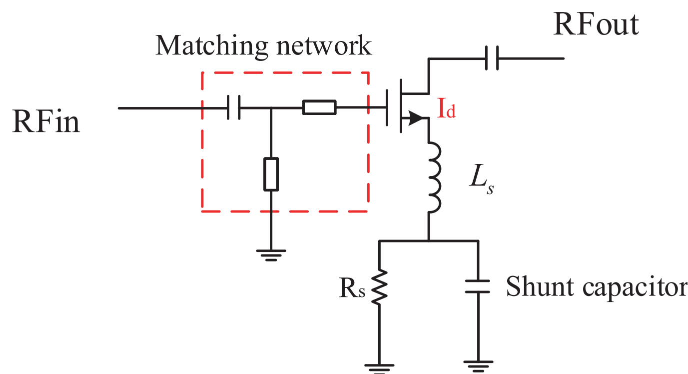


**Figure 6.** Self-bias structure of a transistor.

## 4. MEASUREMENT RESULTS

The proposed Q-band LNA is fabricated in a 90 nm GaAs pHEMT process with 70 µm substrate thickness. Figure 7 shows a micrograph of the LNA with a compact $1.6 \times 0.8\,\text{mm}^2$ chip size, including all RF and dc pads. The LNA is measured by on-wafer probing at RF and dc pads. The measurement setup is shown in Figure 8. The LNA is measured by the Cascade Microtech probe station, Summit 11000B-M. $S$ parameters are measured on-wafer by Agilent E5071C network analyzer, and the noise figure is measured on-wafer byAgilent N8975B noise figure analyzer.

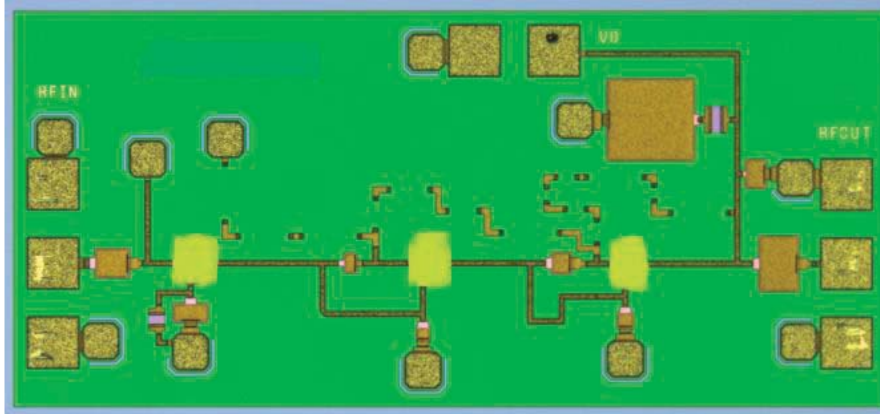


**Figure 7.** Micrograph of the proposed LNA.

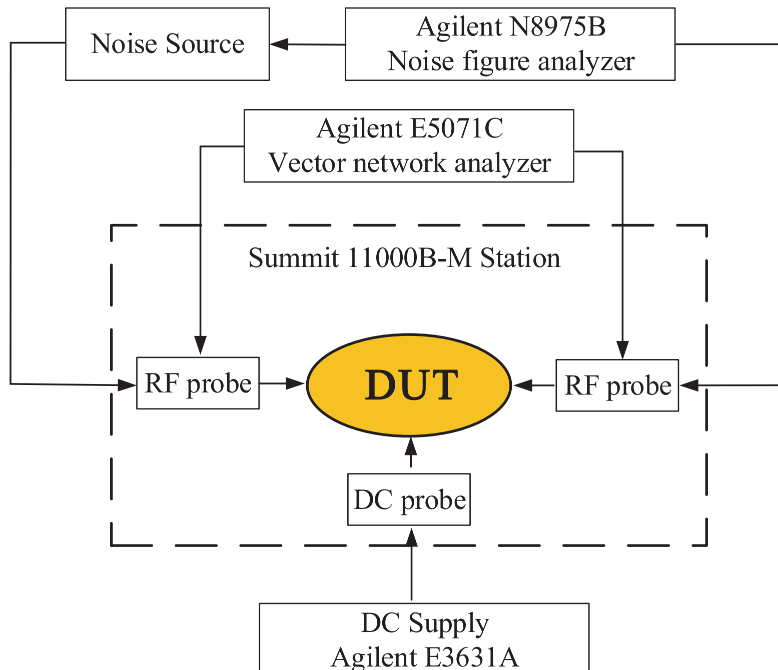


**Figure 8.** Measurement setup ($S$-parameter and noise figure).

For arbitrary 2 sites (1# and 2#) measured across the wafer, the measured and simulated $S$-parameters, NFs, and OP1 dB of the proposed LNA are depicted from Figure 9 to Figure 14. As shown in Figures 9, we can see that the measured $S$-parameter curves of 1# and 2# almost overlap, which indicates that the GaAs process is stable and consistent. As shown in Figures 10∼13, the LNA achieves

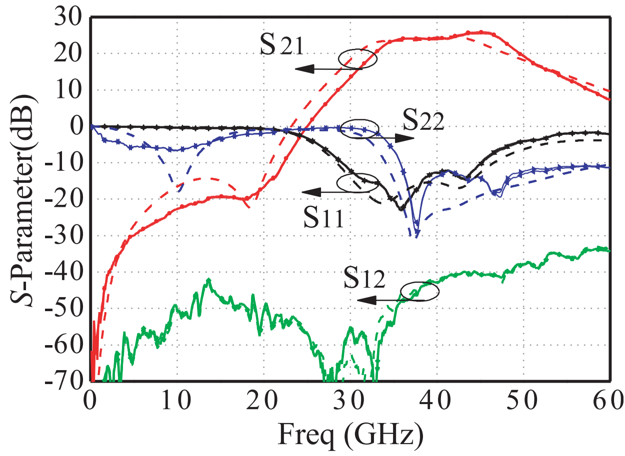


**Figure 9.** Measured (solid line) and simulated (dashed line) $S$-parameters of the proposed LNA (0–60 GHz).

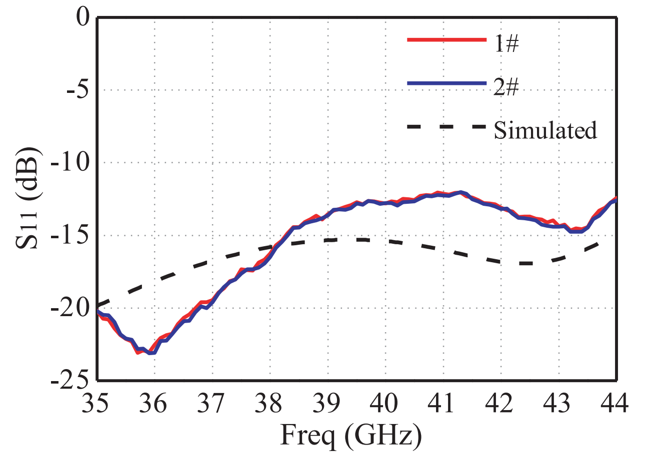


**Figure 10.** Measured and simulated $S_{11}$ of the proposed LNA.

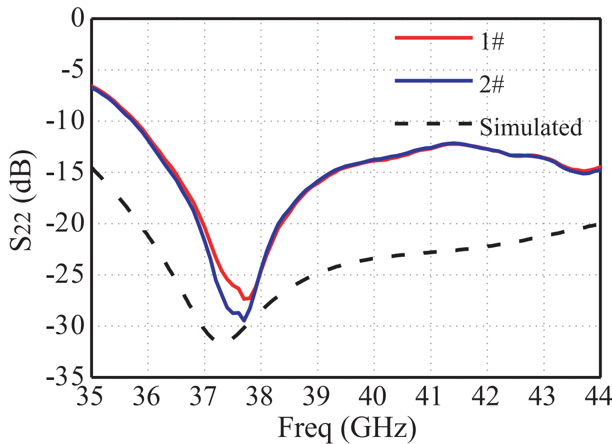


**Figure 11.** Measured and simulated $S_{22}$ of the proposed LNA.

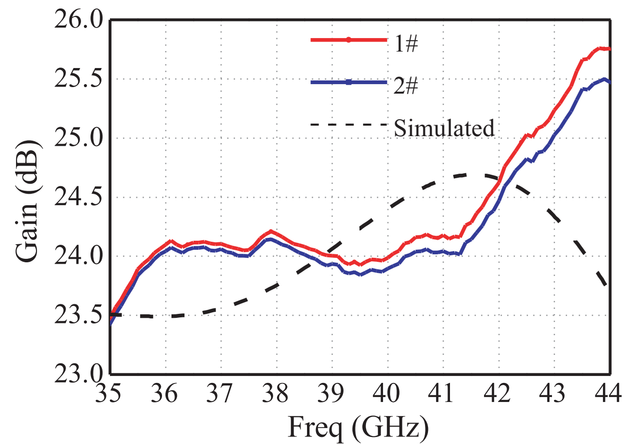


**Figure 12.** Measured and simulated gain of the proposed LNA.

a flat small-signal gain of 23.8 $\sim$ 24.5 dB at frequency band of 36 $\sim$ 42 GHz, and the NF is in the range of 2 $\sim$ 2.1 dB. Input and output return-loss is better than 10 dB. The measured results exhibit a frequency shift about 1 GHz in operating frequency bands compared with the simulated results, which is mainly caused by the improper modeling of the process and the high sensitivity of some matching networks. Noise figure measurement result is approximately 0.2 dB higher than simulated results.

As shown in Figure 14, the measured OP1dB from 36–42 GHz is 6.6 $\sim$ 8 dBm.

The performance of LNA can be assessed by the figure of merit (FOM) related to gain, bandwidth, OP1 dB, noise figure, and dc consumption. The definition of FOM can be written by [21]:

$$FOM = \frac{Gain\,[\text{abs}] \cdot OP1\,[\text{mW}] \cdot Bandwidth\,[\text{GHz}]}{P_{DC}\,[\text{mW}] \cdot (NF - 1)\,[\text{abs}]} \tag{10}$$

Table 1 compares the performance of the proposed LNA with other state-of-the-art LNAs. Compared with other works, the proposed LNA exhibits a good trade-off among gain, noise figure, and dc power consumption.

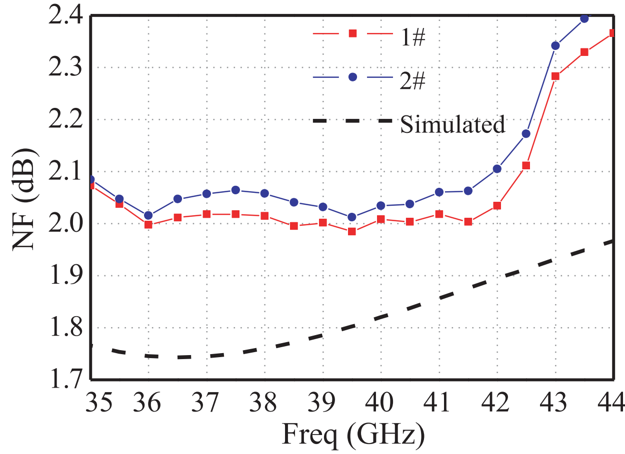


**Figure 13.** Measured and simulated NF of the proposed LNA.

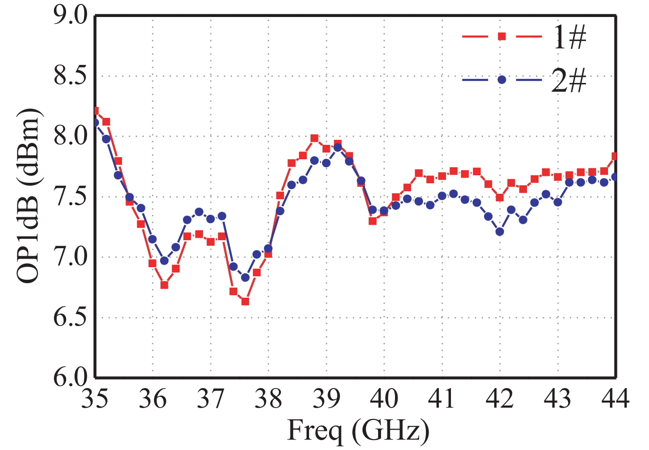


**Figure 14.** Measured OP1 dB of the proposed LNA.

**Table 1.** Comparison with similar works in literature.

| Ref. | Freq (GHz) | NF (dB) | Gain (dB) | OP1 (dBm) | PDC (mW) | Area ($mm^2$) | FOM | Tech |
|---|---|---|---|---|---|---|---|---|
| [22] | 26–32 | 1.8–2.2 | 12.4 | 1.4 | 98 | 0.7 | 0.69 | 0.25 µm SiGe |
| [23] | 35–50 | 3.8–5 | 23 | / | 62.6 | 3 | / | 0.15 µm GaAs |
| [24] | 29–37 | 3.1–4.1 | 25.5–28.5 | 5.3 | 80 | 0.21 | 6.48 | 0.25 µm SiGe |
| [25] | 27–31.5 | 1.7 | 16–18 | 3 | 115 | 3.6 | 1.02 | 70 nm GaAs |
| [26] | 35–50 | 2.5–3 | 25–28 | 9.6 | 155 | 1.62 | 15.8 | 0.1 µm GaAs |
| [27] | 33–41 | 3–4 | 15 | 13 | 280 | 0.7 | 21 | 0.12 µm GaN |
| This work | 36–42 | 2–2.1 | 23.8–24.5 | 6.6–8 | 54.5 | 1.28 | 19.9 | 90 nm GaAs |

## 5. CONCLUSION

A current-reused LNA for Q-band satellite communications application has been presented. The three cascaded common-source amplifying stages share the same current. Source series inductance has been employed to obtain simultaneous noise and input match. The proposed LNA is implemented in a 90 nm GaAs pHEMT technology. The chip area including RF and dc pads is $1.6\times0.8\,mm^2$. The measurement results show a small-signal gain of 23.8∼24.5 dB, noise figure (NF) of 2∼2.1 dB, and output 1-dB compression point (OP1dB) of 6.6∼8 dBm over 36∼42 GHz, while consuming 10.9 mA from a 5 V voltage supply. A high FOM of 19.9 has been achieved.

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