

# Reflection Budgeting Methodology for High-Speed Serial Link Signal Integrity Design

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**Abstract**—Reflective interference caused by impedance discontinuities in the interconnect is a serious impediment to high speed serial link designs. The reflections can be addressed either through expensive equalization circuits or through interconnect redesign. Here a new technique for determining the most significant places to make changes in an interconnect design is presented. Through linearizing the  $S$ -parameter cascading process, three unique reflection budgets are created based on 1) frequency domain insertion loss deviation, 2) time domain peak distortion analysis and 3) time domain reflectometry. Example analysis of a 25.8 Gb/s NRZ system identifies the connectors as the primary contributors to reflective interference and estimates that the interactions with the rest of the interconnect with the connector impedance discontinuities reduces the system eye height by 84 mV.

## 1. INTRODUCTION

The performances of low-loss wired communication links, from sub Gb/s early PCI-express and Ethernet interfaces to modern interfaces with speeds of 10 Gb/s, 25 Gb/s [1], 64 Gb/s and 112 Gb/s, are often limited by reflections caused by impedance discontinuities (mismatches) in the system. These reflections can be reduced by improving the impedance discontinuities [2] such as by etching the PCB reference ground plane to improve connector contact pad impedance [3], utilizing unique PCB via anti-pad shapes to balance the capacitive and inductive differential coupling [3], back drilling PCB vias to remove reflective stubs [4], and utilizing new via designs like face vias instead of conventional barrel vias [5]. Alternatively, power-hungry and complex equalization schemes like floating-tap decision feedback equalization circuitry can be utilized [6].

For a wired channel suffering from excessive reflections, impedance discontinuities must be located and improved. Either a time domain reflectometry (TDR) waveform [7] or resonances in the frequency domain insertion loss [8] can be used to estimate the location of a discontinuity. That segment of the interconnect is then modified to see if the system performance improves. When applied iteratively, this approach usually identifies the primary source of reflective interference. This process is neither systematic nor wholly repeatable due to the many subjective choices involved. Since procedures like this are learned through experience, it is often difficult to convey this knowledge to others and contributes to the perception that signal integrity is more art than engineering. Additionally, removing or modifying a segment fundamentally changes the system, making the true impact of a single discontinuity difficult to quantify [9].

Reflections have traditionally been budgeted by considering their impact as a source of noise in the system [10]. In this paper, we propose a new approach similar to the communication power link budget [11], which provides design targets for the loss/power of each component. Where the power link budget is an essential system design tool when loss is the dominant impairment in the system, this reflection budget is useful for systems where reflections are the dominant impairment. By quantifying

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how each two-way combination of impedance discontinuities degrade the system performance, the often non-intuitive and complex multi-bounce reflections are clearly understood. This newly gained insight into the resonant behavior of the system can lead to a prioritized redesign of the interconnect. Conventional system simulation or analysis tools, such as insertion loss deviation (ILD), peak distortion analysis (PDA) and TDR can quantify the collective impact of the system loss and reflections but a reflection budget can use these same tools to quantify how each system block contributes to the total reflection impairment.

This paper demonstrates a practical approach to reflection budgeting for high-speed wired communication link designs utilizing a cascading  $S$ -parameter linearization technique (CSLT) introduced in [12] and expanded and generalized here. The linearization separates the actual total system response into physically meaningful pieces that can be manipulated in the frequency and time domains. The objective of the linearization and subsequent analysis is not to provide an alternative way to calculate the actual total system response, for which excellent methods already exist, but to gain insight and understanding of the sources of reflective interference in the system. With this perspective, the small error introduced with the linearization is acceptable in many applications. We use an illustrative example where three fictional engineering teams jointly design a CEI 25G-LR interface [1]. While most current circuit design focus is on 112 Gb/s and 56 Gb/s interfaces, slower 25 Gb/s interfaces are still widespread and commoditized as system integrators work to maintain performance while reducing material cost through interconnect redesign. We show how using reflection budgets in the frequency domain with an ILD budget (Subsection 3.1), in the time domain with a PDA budget (Subsection 3.2), and a TDR budget (Subsection 3.3) can guide multi-party interconnect design. Section 4 concludes with a discussion of the advantages and disadvantages of the three reflection budgets as well as future enhancements and other potential applications of the CSLT approach.

## 2. MASON'S RULE AND LINEARIZATION

System level signal integrity commonly utilizes the process of cascading together a series of frequency domain  $S$ -parameter models of packages, circuit board vias, transmission lines, connectors, etc., to obtain the total system  $S$ -parameter [13–15] which is then used to quantify the system performance with either frequency or time domain analysis. When  $S$ -parameter block boundaries correspond to component boundaries, the  $S$ -parameter reflection terms can be used as proxy for the impedance discontinuities present in each component.

Therefore, to illustrate how each block in a system contributes to the reflective interference, we consider a two-port three-block system in Fig. 1(a); the three individual  $S$ -parameters are labeled  $A$ ,  $B$  and  $C$ . After expressing the system as a signal-flow graph in Fig. 1(b), we utilize Mason's rule [16] to find the actual total through response,  $S_{21}$ . The first Mason's rule step is to identify the loops in the system, which are  $L_1 = A_{22}B_{11}$ ,  $L_2 = A_{22}B_{21}C_{11}B_{12}$ , and  $L_3 = B_{22}C_{11}$  as shown in Fig. 1(b). The next step is to identify all direct paths between the in- and out-ports. For the actual total  $S_{21}$ , there is only one direct through path,  $P_1 = A_{21}B_{21}C_{21}$ .

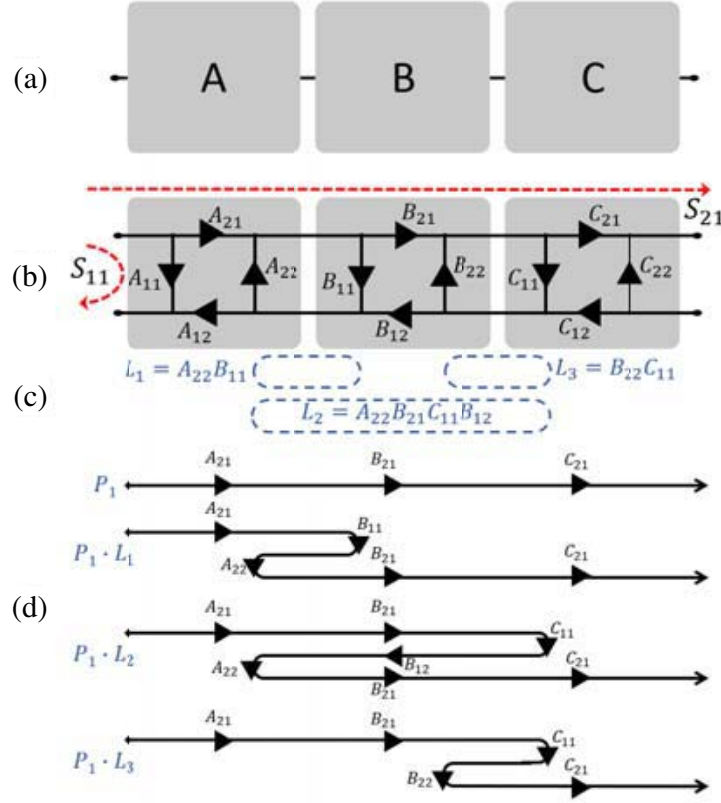
The next step in Mason's rule is to find the determinant ( $\Delta$ ) of the graph and the co-factor ( $\Delta_k$ ) of each direct path. The determinant is found by collecting products of non-touching loops in groupings of one-at-a-time, two-at-a-time, etc., until all possible non-touching loop combinations are included as shown in Eq. (1).

$$\Delta = 1 - \sum L_i + \sum_{\text{non-touching}} L_i L_j - \sum_{\text{non-touching}} L_i L_j L_k + \dots \quad (1)$$

This calculation accounts for the interactions that occur between non-touching loops, and as will be seen below, a modification of this calculation opens the opportunity for linearization [12, 17, 18]. For our three-block example, there are three one-at-a-time loops ( $L_1, L_2, L_3$ ), one two-at-a-time non-touching loop ( $L_1 L_3$ ) and no three-at-a-time non-touching loops, giving the determinant of

$$\Delta = 1 - L_1 - L_2 - L_3 + L_1 L_3. \quad (2)$$

The cofactor of a direct path is defined as the determinant calculation over the set of loops which do not touch the direct path. Since the direct path  $P_1$  touches each loop,  $\Delta_1 = 1$ .



**Figure 1.** (a) Black box diagram of three two-port  $S$ -parameter block system, labeled  $A$ ,  $B$  and  $C$ . (b) A signal flow graph shows the individual  $S$ -parameter components of  $A$ ,  $B$  and  $C$  and illustrates the many loops and paths through the system. (c) Energy can resonate (get trapped) in the loops,  $L_1$ ,  $L_2$ , and  $L_3$ . (d) A 1st order approximation of the through response,  $S_{21}$ , is found by summing the direct path  $P_1$  and the paths going through each loop once.

Once the loops, paths, determinant and cofactors are identified, Mason’s rule gives the transfer function equation:

$$S_{ij} = \frac{\sum_k P_k \Delta_k}{\Delta}. \quad (3)$$

Applying (3), the actual total  $S_{21}$  of the signal flow graph in Fig. 1(a) is

$$S_{21} = \frac{P_1}{1 - L_1 - L_2 - L_3 + L_1 L_3}. \quad (4)$$

### 2.1. Linearization of the Through Response ( $S_{21}$ ) with CSLT

The actual total through response,  $S_{21}$ , in Eq. (4) is nonlinear in the sense that the multi-path reflective behavior of the system, as embodied by the denominator, is not easily separated from the direct through path  $P_1$ , and the inclusion of more blocks can significantly change the behavior in complex ways. Linearizing the cascade of  $S$ -parameters [12], accomplished by moving the denominator to the numerator and simplifying as described in this section, will allow for the estimation of the reflective interference contribution of each block in the system. This is done by first modifying the Mason’s rule determinant calculation to assume that none of the loops touch and are thus independent. This results in the inclusion of the higher order terms  $L_1 L_2$ ,  $L_2 L_3$  and  $L_1 L_2 L_3$ , which is acceptable due to their

small magnitude, i.e.,  $1 > |A_{22}| > |L_1| > |L_1L_2| \gg |L_1L_2L_3|$ .

$$S_{21} \approx \frac{P_1}{1 - L_1 - L_2 - L_3 + L_1L_2 + L_1L_3 + L_2L_3 - L_1L_2L_3} \quad (5)$$

These additional terms allow for the determinant to be completely factorized, and any numerator cofactor terms from loops that the path does not touch will be canceled as well (see Subsection 2.2):

$$S_{21} \approx S_{21}^\dagger = \frac{P_1}{(1 - L_1)(1 - L_2)(1 - L_3)} \quad (6)$$

This approximation,  $S_{21}^\dagger$ , will be utilized by the ILD analysis (Subsection 3.3) where Eq. (6) is separated by a logarithmic operator. For time domain analysis, the product must be further separated into additive terms by applying the geometric series approximation,  $\frac{1}{1-x} = \sum_{n=0}^{\infty} x^n$  if  $|x| < 1$ , which gives:

$$S_{21} \approx P_1 \left( \sum_{n=0}^{\infty} L_1^n \right) \left( \sum_{n=0}^{\infty} L_2^n \right) \left( \sum_{n=0}^{\infty} L_3^n \right) \quad (7)$$

Truncating each infinite series at  $n = 1$ :

$$S_{21} \approx P_1 (1 + L_1)(1 + L_2)(1 + L_3) \quad (8)$$

and discarding cross-terms (due to their smaller magnitude) simplifies to:

$$S_{21} = \tilde{S}_{21} + \epsilon_{S_{21}} = P_1 (1 + L_1 + L_2 + L_3) + \epsilon_{S_{21}} \quad (9)$$

We call  $\tilde{S}_{21}$  the 1st order linearization of  $S_{21}$ . This allows the actual total through response  $S_{21}$  to be decomposed into the sum of the direct path reflection-less through response,  $P_1 = A_{21}B_{21}C_{21}$ , and loop responses,  $P_1L_1$ ,  $P_1L_2$ , and  $P_1L_3$  as seen in Fig. 1(c). The additive linearization error,  $\epsilon_{S_{21}}$ , is found by taking the difference between the total response,  $S_{21}$ , and the approximate response,  $\tilde{S}_{21}$ . This will be shown to be sufficiently small for the examples in this paper. This error estimates the uncertainty bound on the analysis results. Lastly, the linearization error could be further reduced by including higher order loop terms in Eqs. (7) and (8) at the cost of additional complexity [12]. This could be beneficial for highly resonant systems.

## 2.2. Reflection Response ( $S_{11}$ or $S_{22}$ ) with CSLT

The actual total reflection response,  $S_{11}$  or  $S_{22}$ , is more complex than the actual total through response,  $S_{21}$ , since the reflection response of the cascade of  $N$  2-port  $S$ -parameters will have  $N$  direct paths whereas the through response will only have a single direct path. The actual total  $S_{11}$  for the three-block system in Fig. 1(a) has three direct paths,  $P_1 = A_{11}$ ,  $P_2 = A_{21}B_{11}A_{12}$ , and  $P_3 = A_{21}B_{21}C_{11}B_{12}A_{12}$  and is calculated from Mason's rule as:

$$S_{11} = \frac{P_1\Delta}{\Delta} + \frac{P_2(1 - L_3)}{\Delta} + \frac{P_3}{\Delta}, \quad (10)$$

where  $\Delta$  is the same as Eq. (2). Linearizing Eq. (10) gives:

$$S_{11} \approx S_{11}^\dagger = P_1 + \frac{P_2(1 - L_3)}{(1 - L_1)(1 - L_2)(1 - L_3)} + \frac{P_3}{(1 - L_1)(1 - L_2)(1 - L_3)} \quad (11)$$

$$S_{11} = \tilde{S}_{11} + \epsilon_{S_{11}} = P_1 + P_2(1 + L_1 + L_2) + P_3(1 + L_1 + L_2 + L_3) + \epsilon_{S_{11}}$$

The linearization step of assuming that the loops are independent allows the determinant,  $\Delta$ , to be factorized and the cofactor term,  $1 - L_3$ , of the direct path  $P_2$  to be canceled out. The additive error,  $\epsilon_{S_{11}}$ , is found by taking the difference between the actual total  $S_{11}$  and the linearization  $\tilde{S}_{11}$ . This three-block decomposition has three direct paths and five loop responses that each contribute to the reflection response. This perspective will be applied to TDR decomposition and budgeting in Subsection 3.3.

### 2.3. Generalization of CSLT

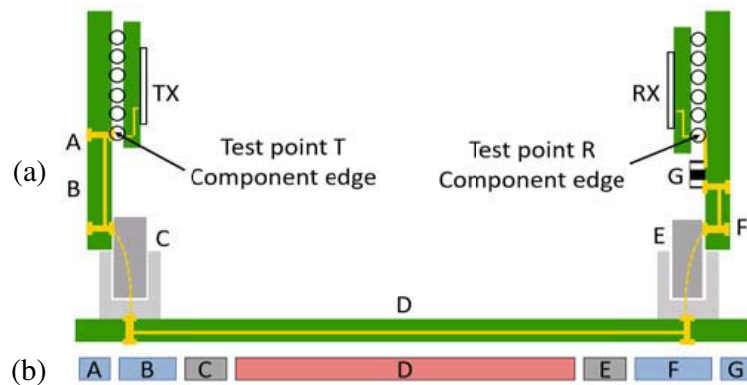
The generalized 1st order cascading  $S$ -parameter linearization technique uses the loops  $L_i$  and the direct paths  $P_K$  between the in- and out-ports to give the analytic expression for the through or reflection response:

$$S_{out,in} = \sum_k \left( P_k \left( 1 + \sum_{i=\{P_k \sim L_i\}} L_i \right) \right) + \epsilon \tag{12}$$

where the notation  $P_k \sim L_i$  indicates the set of loops  $L_i$  that touch path  $P_k$  and  $\epsilon$  is the additive error. The linearization does introduce error, but this error is readily calculated and quantified. A bound to the error was attempted in [12] but for practical applications it is much more effective to empirically track the error and use it to inform the uncertainty of any analysis. In the next section, this CSLT in Eq. (12) will be applied directly in the time domain for the peak distortion analysis (PDA) reflection budget and time domain reflectometry (TDR) budget and a generalization of Eq. (6) will be applied in the frequency domain for the insertion loss deviation (ILD) reflection budget.

### 3. REFLECTION BUDGETS

In this section, we will provide an illustrative example of a practical reflection budget methodology using the cascading  $S$ -parameter linearization technique (CSLT) for a CEI 25G-LR interface design [1] shown in Fig. 2(a). The example physical CEI 25G-LR channel is based on a proprietary system model derived from measurements and 3D EM simulations. While this proprietary channel model is not directly used, permission was granted to emulate this interface with numerous short parametric lossy transmission line models, where the electrical delay, impedance profile and overall loss were maintained. This synthetic model is divided into seven segments or blocks as illustrated in Fig. 2(b). The lossy parameterized transmission line models are from the causal channel operating margin (COM) package equations [10, 19]. The  $S$ -parameter creation, time domain waveform conversion and analysis were performed in MATLAB<sup>TM</sup>. As with any signal integrity analysis that is based on  $S$ -parameters, this analysis relies on the  $S$ -parameter models of the system being passive, causal and accurate [20]. Therefore, if the system analysis is already based on cascading  $S$ -parameter channel components to obtain the total channel response, this analysis is directly applicable, regardless of whether the  $S$ -parameters are measured, simulated [21] or calculated [22, 23].

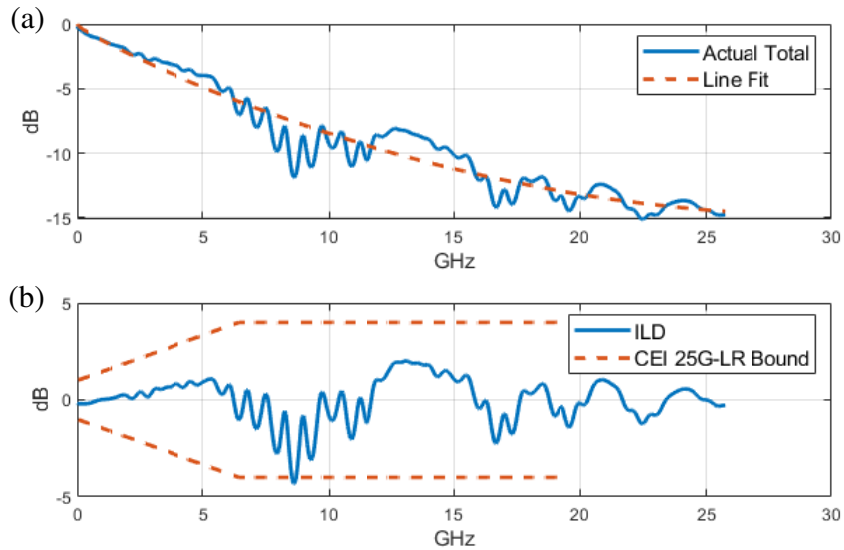


**Figure 2.** (a) The CEI 25G-LR interface presents a very challenging design task for high speed SerDes. The impedance discontinuities from the connectors and many PCB vias create large reflections that distort and interfere with the desired signal. The “channel” is defined from test point T on the transmitter (TX) to test point R on the receiver (RX) side. (b) The channel interconnect is modeled here with 7  $S$ -parameter blocks. Team X is responsible for integrated circuit (IC) package and line card design and owns blocks labeled A, B, F and G. Team Y is responsible for the connector design and owns blocks labeled C and E. Team Z is responsible for the backplane design (the block labeled D) and system integration.

The design is a collaborative effort among three fictional teams. Team X is responsible for integrated circuit (IC) package and line card design represented by blocks  $A$ ,  $B$ ,  $F$ ,  $G$ . Team Y is responsible for the connector design (blocks  $C$  and  $E$ ); Team Z is responsible for the backplane design (block  $D$ ) and the integration of the various components of the system. These three fictional teams represent the competing interests common to collaborative project design. This segmented design approach allows each team to develop their interconnect models independently and to vary segment properties (such as impedance) for use in design space exploration. During a high-volume manufacturing study, where the seven channel components are varied in impedance, Team Z, the system integrator, identifies a worst-case channel configuration that violates the insertion loss deviation (ILD) bounds in the CEI 25G-LR specification. The analysis of this worst-case channel will be the use case discussed in the remainder of the paper.

### 3.1. Insertion Loss Deviation (ILD) Reflection Budget

In this section, the cascading  $S$ -parameter linearization technique (CSLT) from Section 2 will be applied to quantify the impact of each block on the insertion loss in this worst-case channel using ILD [1, 10], described in Appendix A. The actual total frequency domain differential insertion loss provides insight into the channel attenuation. A smooth insertion loss is indicative of a simple lossy channel, whereas a highly variable insertion loss as shown in Fig. 3(a) is common for very reflective channels. ILD is used to quantify the variability in the insertion loss and is defined as the difference between the insertion loss and a polynomial line fit model [1], also shown in Fig. 3(a). For this worst-case channel, the ILD exceeds the CEI 25G-LR ILD specification bound at 8.6 GHz as shown in Fig. 3(b); ideally, the ILD would be around 0 dB. The three design teams must decide how to reduce the ILD.



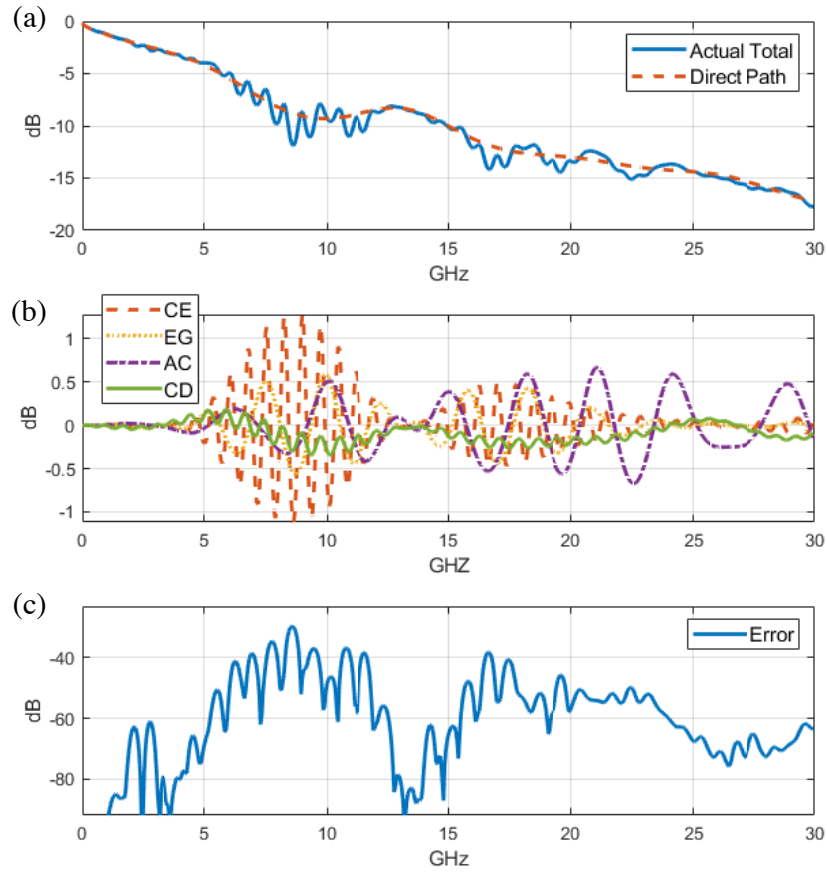
**Figure 3.** (a) Insertion loss (IL) with high variability due to reflections and a polynomial line fit. (b) Insertion Loss Deviation (ILD) is the difference between the insertion loss and the line fit; it is ideally 0 dB. This channel has an ILD in excess of  $-4$  dB at 8.6 GHz which violates the ILD bound for the CEI 25G-LR standard [1].

We extend the CSLT in Eq. (6) to find the linearized or approximate through response,  $S_{21}^{\dagger}$ , of the seven-block system as a product of physically meaningful terms:

$$S_{21}^{\dagger} = \frac{P_1}{\prod_{i=1}^{21} (1 - L_i)} \quad (13)$$

where  $P_1 = A_{21}B_{21}C_{21}D_{21}E_{21}F_{21}G_{21}$  is the direct reflection-less through path, and  $1/(1 - L_i)$  is the  $i$ th loop response. For a cascade of  $N$  two-port  $S$ -parameter blocks, there will be  $N(N - 1)/2$  loops present. Therefore, for  $N = 7$  blocks there are 21 loops to consider. The  $\log_{10} S_{21}^\ddagger = \log_{10} P_1 - \log_{10} (1 - L_1) - \dots - \log_{10} (1 - L_{21})$  uses the linear nature of the ILD operator to allow each term to be independently analyzed.

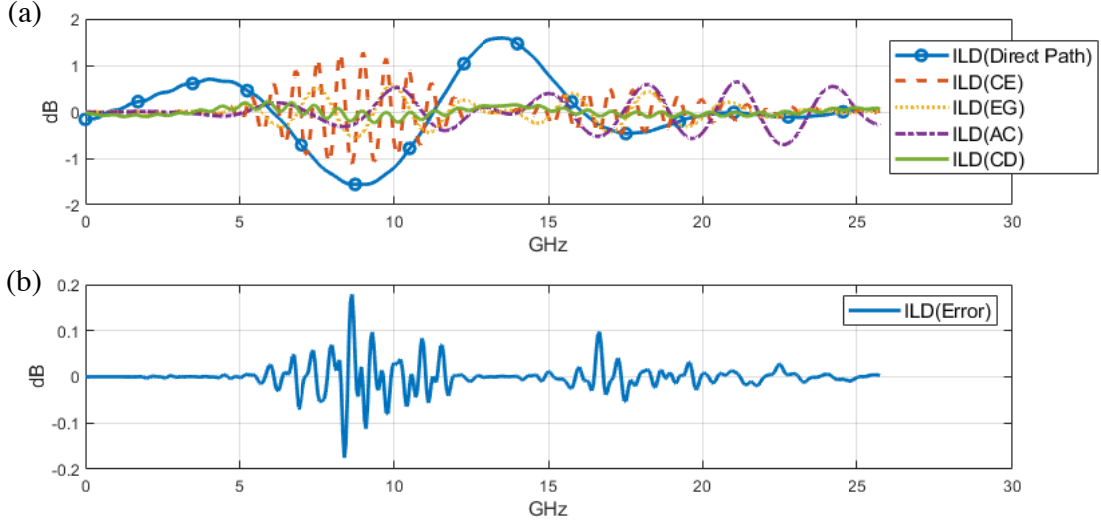
The logarithm of the individual components of Eq. (13), i.e., the ILD decomposition of  $S_{21}$ , is shown in Fig. 4. The magnitudes of the actual total and direct reflection-less through paths are shown in Fig. 4(a). The magnitude of the four largest loop responses between blocks  $C&E$ ,  $E&G$ ,  $A&C$  and  $C&D$  in Fig. 4(b) and the magnitude of the decomposition error,  $S_{21} - S_{21}^\ddagger$ , is shown in Fig. 4(c). The maximum magnitude of the error response of  $-40$  dB (a difference of  $1/100$ ) validates that the insertion loss of  $S_{21}$  can be successfully decomposed into a direct reflection-less insertion loss and several 1st order resonant loops.



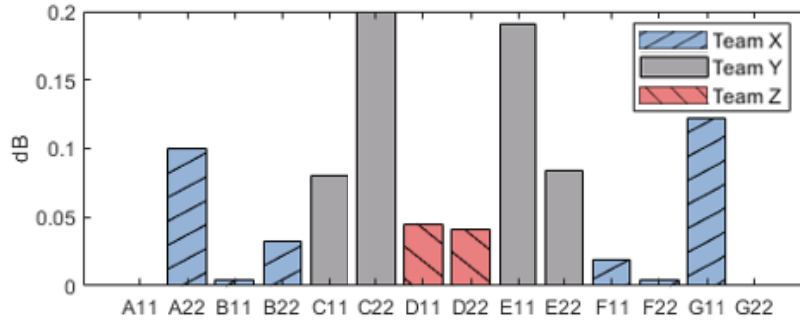
**Figure 4.** The actual total  $S_{21}$  is decomposed into a direct reflection-less through path and loop responses, (a) shows the magnitudes of the actual total  $S_{21}$  and the direct reflection-less through path. Each pair of blocks creates a loop, (b) shows the magnitude of the four largest loop responses, where the loop between blocks  $C$  and  $E$  is labeled  $CE$ , etc. The difference between the actual total  $S_{21}$  and the sum of the direct reflection-less through path and loop responses is the decomposition error and (c) shows the magnitude of this error.

Each piece of the linearized through response in Eq. (13) is processed with the linear ILD operator to quantify its contribution to the actual total ILD. The ILD of the direct reflection-less through path and the top four loop responses are shown in Fig. 5(a). Notably, at 8.6 GHz all the contributors to the ILD have the same sign and combine constructively to cause the maximum ILD seen in Fig. 3(b).

The CEI 25G-LR standard provides a figure of merit,  $FOM_{ILD}$  [1], to summarize the ILD waveform



**Figure 5.** (a) Utilizing the linear ILD operator, the ILD contributions of the direct reflection-less through path and the loop responses are calculated. At 8.6 GHz, the frequency of the maximum ILD, every contributor constructively combines to achieve the maximum ILD. (b) The ILD of the insertion loss decomposition error is less than 0.2 dB at 8.6 GHz.



**Figure 6.** A reflection budget based on the  $FOM_{ILD}$  is found by distributing the  $FOM_{ILD}$  of each loop response to the return loss bins that define each loop. The connector  $S$ -parameters, blocks  $C$  and  $E$ , are the largest contributors but the receiver package ball and PCB model, block  $G$ , adds significant ILD to the system. The  $FOM_{ILD}$  of the error is 0.021 dB and sets the uncertainty of the reflection budget.

in a single value, as detailed in Appendix A. Unfortunately, this metric is nonlinear, as the FOM of the sum of signals is less than or equal to the sum of the FOM of signals as shown in Eq. (A8). Nevertheless, provided that we understand this over-estimation shortcoming, the metric is useful in understanding the relative impact of each component on the actual total  $FOM_{ILD}$ . In this situation, the actual total  $FOM_{ILD}$  is 0.755 dB, whereas the sum of the component's  $FOM_{ILD}$  is 0.921 dB.

To quantify how each of the 21 loops in the system contributes to the actual total  $FOM_{ILD}$  and to create a reflection budget, we create bins for each return loss term in the system and assign the  $FOM_{ILD}$  of each of the 21 loop responses to the bin according to the return loss terms in each response. For instance, the loop response between blocks  $C$  and  $E$ , labeled ‘ $CE$ ’ in Fig. 5(a), is  $1/(1 - C_{22}D_{21}E_{11}D_{12})$ ; the  $FOM_{ILD}$  of this response is 0.273 dB and is split equally between the  $C_{22}$  and the  $E_{11}$  bins of Fig. 6. The result of this assignment for all the 21 loop responses is collected in Fig. 6. This shows that the connector reflection coefficients,  $C_{22}$  and  $E_{11}$ , are the primary contributors, but also that  $G_{11}$ , the receiver package bump/PCB via model, is a major contributor to reflective interference.

With the sources of reflective interference between blocks identified and quantified, the blocks of each team is responsible for are shown in Fig. 6. Team X cumulatively has 0.282 dB of  $FOM_{ILD}$  (30.5%



of total) for blocks  $A$ ,  $B$ ,  $F$  and  $G$ , Team Y cumulatively has 0.554 dB of  $FOM_{ILD}$  (60.1% of total) for blocks  $C$  and  $E$ , and Team Z cumulatively has 0.086 dB of  $FOM_{ILD}$  (9.3% of total) for block  $D$ .

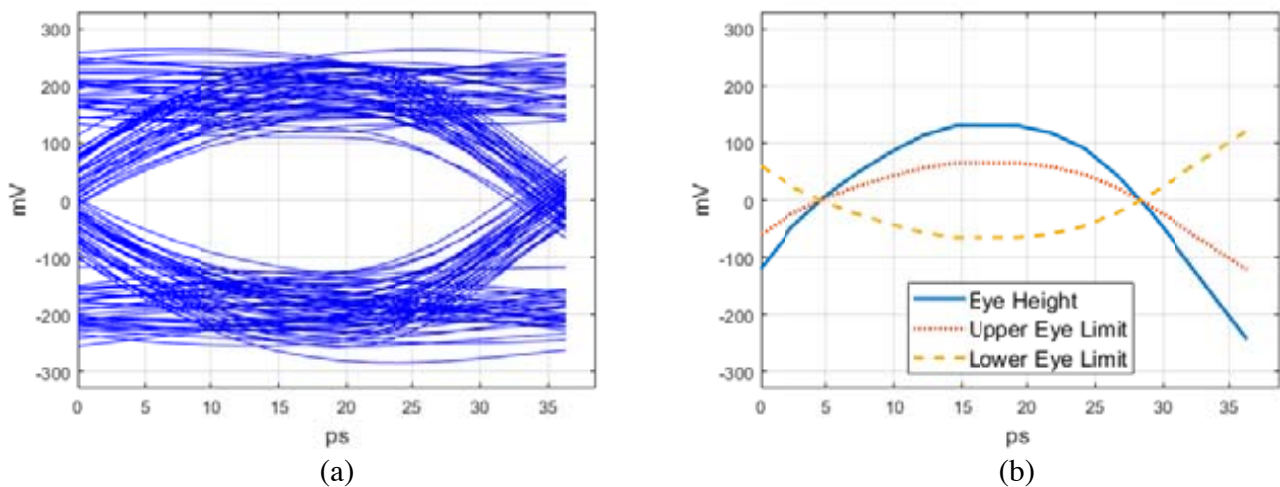
Although the connectors, blocks  $C$  and  $E$ , are the primary cause of the reflections, the connector design team Y is limited in its ability to improve the connectors' impedance mismatch. Therefore, the teams might collectively decide that Team X, the IC package and line card design team, should improve the impedance variation of their PCB vias and packages in block  $G$  to reduce the ILD at 8.6 GHz to avoid the possibility of this worst-case channel. Another approach is to lower the target characteristic impedance of the backplane and line-card transmission lines from  $100\ \Omega$  to  $85\ \Omega$  (like the PCIe standard), but this is precluded by the CEI 25G-LR standard that requires a nominal transmitter and receiver differential impedance of  $100\ \Omega$ . Overall, when excess ILD is encountered, this method can quantify how each component of the channel contributes to the system reflections.

A caveat of the analysis is to consider *where* the channel is broken into blocks, since the ILD due to interactions between the blocks is captured and budgeted, but the ILD within a block is not. Dividing the channel into more blocks will increase the localization of the decomposition but will also increase the decomposition error and thus effectively limit the precision of the analysis. If a  $S$ -parameter block contains multiple discontinuities, for example a combined model of a PCB via and connector, then the analysis is unable to distinguish between the multiple discontinuities and can only quantify the collective impact of the block discontinuities. The budget analysis is appropriate when the number of blocks is minimized, and boundaries are chosen to separate transmission lines from vias, connectors and solder bumps.

### 3.2. Peak Distortion Analysis (PDA) Reflection Budget

The ILD analysis in the frequency domain from the previous subsection is useful, but a time domain approach can give better insight into the system performance. This is due to the ability to directly estimate the bit error rate (BER), visualize/analyze eye diagrams and apply equalization to improve signal quality in the time domain. The worst-case 7-block channel is analyzed at 25.8 Gb/s and has a unit interval of 38.76 ps [1].

An eye diagram is found by taking time domain symbol pattern waveforms, slicing them at the symbol transition times, and overlaying them as shown in Fig. 7(a). There are also analytic methods to estimate the eye from a pulse response [24] as shown in Fig. 7(b). The peak distortion analysis (PDA) method (described in Appendix B) estimates the worst-case inner eye due to the inter-symbol



**Figure 7.** An eye diagram shows how difficult it is to distinguish a logic high symbol from a logic low symbol at the receiver. (a) An eye diagram formed by slicing and overlaying a symbol pattern waveform, (b) inner eye limits are found with peak distortion analysis (PDA) operating on the pulse response.

interference present in a pulse response. The difference between the upper and lower eye limits is the eye height, shown in Fig. 7(b). These eye diagrams include a receiver based continuous time linear equalizer (CTLE) with 9 dB of peaking gain at 12.8 GHz [25] to compensate for the loss in the interconnect. Although this equalization improves the eye height by 132 mV, it cannot compensate for the reflective interference of the system and falls short of the system eye height target of 150 mV.

The cascading  $S$ -parameter linearization of Eqs. (9) and (12) is applied to the frequency domain through response of the 7-block system, which results in:

$$S_{21} = P_1 (1 + L_1 + L_2 + \dots + L_{21}) + \epsilon_{S_{21}} \quad (14)$$

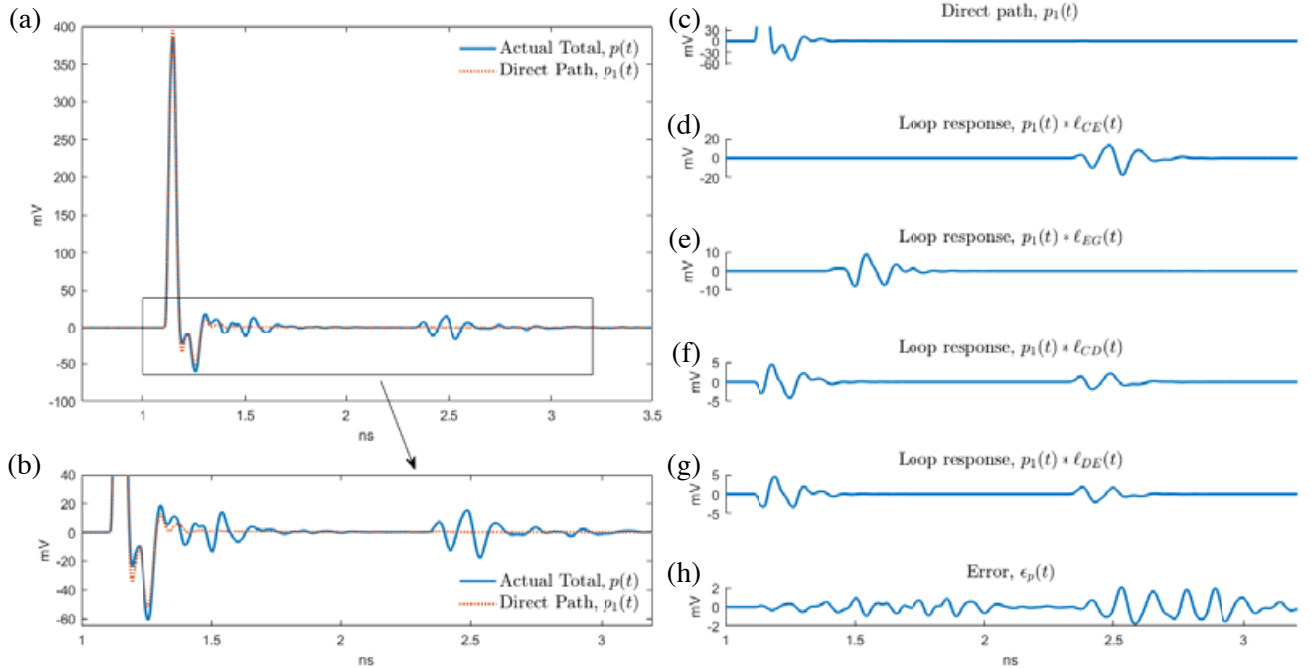
where  $P_1 = A_{21}B_{21}C_{21}D_{21}E_{21}F_{21}G_{21}$  is the direct reflection-less through path;  $P_1L_i$  is the  $i$ th loop response for loops 1 through 21; and  $\epsilon_{S_{21}}$  is the frequency domain additive error. The decomposed frequency domain responses in Eq. (14) are converted to the time domain and transformed to pulse responses:

$$p(t) = p_1(t) * (1 + \ell_1(t) + \ell_2(t) + \dots + \ell_{21}(t)) + \epsilon_p(t) \quad (15)$$

where  $*$  is the convolution operator. The pulse responses for the actual total through,  $p(t)$ , the direct reflection-less through path,  $p_1(t)$ , and the pulse response error,  $\epsilon_p(t)$ , are shown in Fig. 8. The difference between the actual total and the direct path pulse responses illustrates the reflective interaction between the seven blocks in the link. The four largest time domain loop responses are shown in Figs. 8(d)–8(g). We validate the decomposition by finding the difference between the actual total pulse response and the sum of the direct reflection-less through path and the 21 loop responses. This error, which has a 2 mV peak swing, is shown in Fig. 8(h); this shows that the 1st order linearization can accurately represent the system.

The influence of each loop response,  $p_1(t) * \ell_i(t)$ , on the eye opening is found by first forming a pulse response *omitting* the contribution of this loop response:

$$p_i^\Delta(t) = p(t) - p_1(t) * \ell_i(t). \quad (16)$$



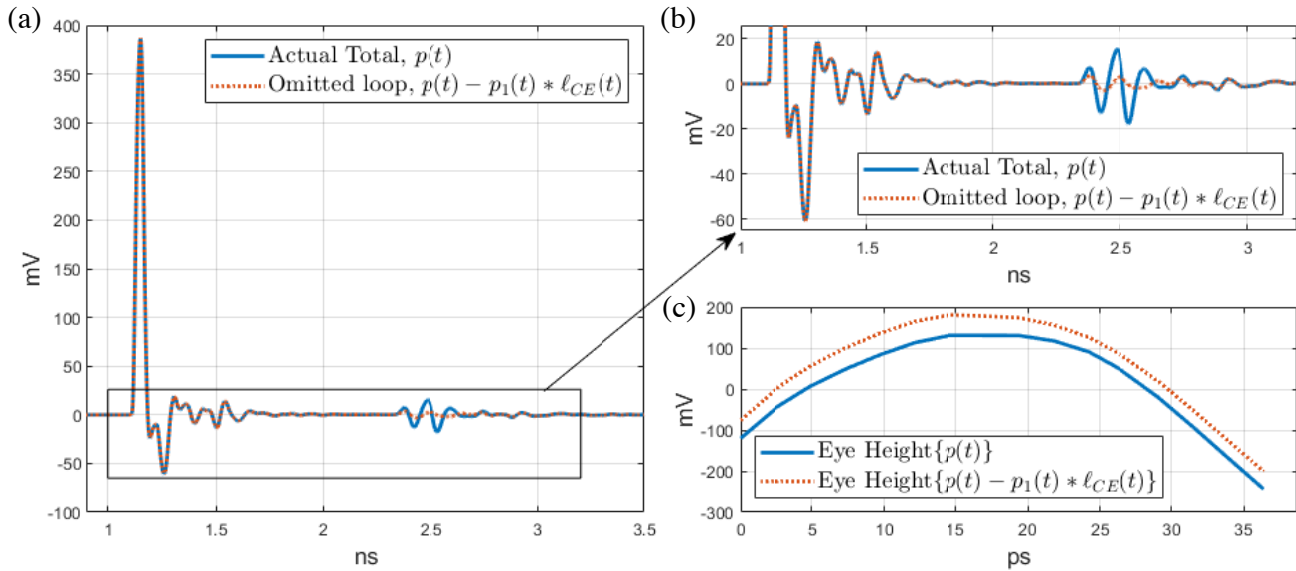
**Figure 8.** The pulse response is a common characterization of the channel and is the basis of several analysis techniques for estimating the goodness of channel capacity (PDA, Statistical Eye, etc.). (a) The actual total pulse response and the direct reflection-less through path pulse response, (b) zoom view of (a) to emphasize the system reflections, (c) zoomed view of the direct reflection-less through path, (d)–(g) the four largest loop responses, (h) pulse response error found by taking the difference between the actual total and the sum of the direct path and all of the loop responses per (15).

The impact of the loop can be indirectly quantified by contrasting the maximum PDA eye heights with and without the loop response. Note that other metrics such as eye width could have been used, but this becomes ill-defined for marginal systems. Whereas a negative maximum eye height has a clear interpretation, a negative eye width does not. The impact of each loop is found by using the PDA maximum eye height operator defined in Eq. (B4):

$$I_i = \text{EH}_{\max} (p_i^{\Delta}(t)) - \text{EH}_{\max} (p(t)). \tag{17}$$

In short, by quantifying the system performance with and without a loop response waveform, its eye closure contribution is quantified.

An example of this loop impact calculation is shown in Fig. 9 for loop  $l_{CE}$ . The pulse responses with and without  $Loop_{CE}$  are shown in Figs. 9(a) and 9(b) and the PDA eye height for both in Fig. 9(c). By contrasting the maximum eye height, we estimate the impact of loop  $l_{CE}$  to be 50 mV of eye closure.

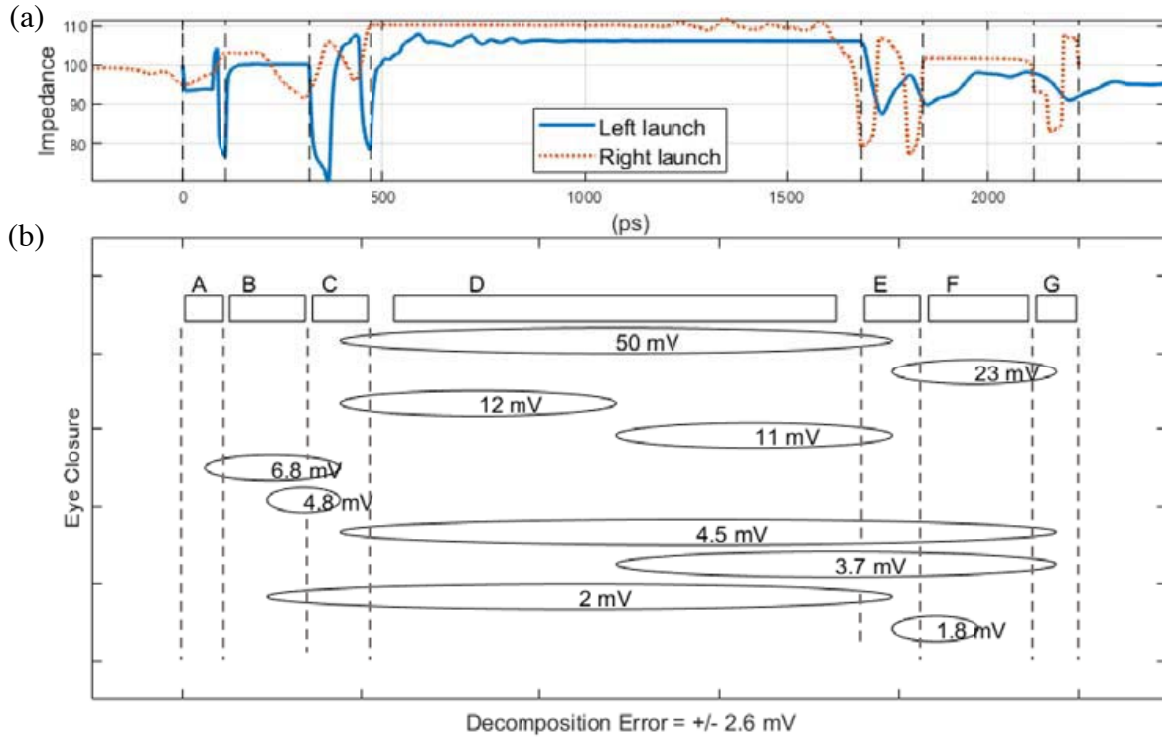


**Figure 9.** To determine the impact of the resonant loop between blocks  $C$  and  $E$ , (a) and (b) the omitted loop pulse response is found by subtracting the loop response from the actual total pulse response, (c) peak distortion analysis (PDA) is then used to estimate the eye height (versus position in the eye) for the actual total and the omitted loop pulse responses. The impact of loop  $l_{CE}$  is estimated to be 50 mV by finding the difference between the maximum eye heights of the responses.

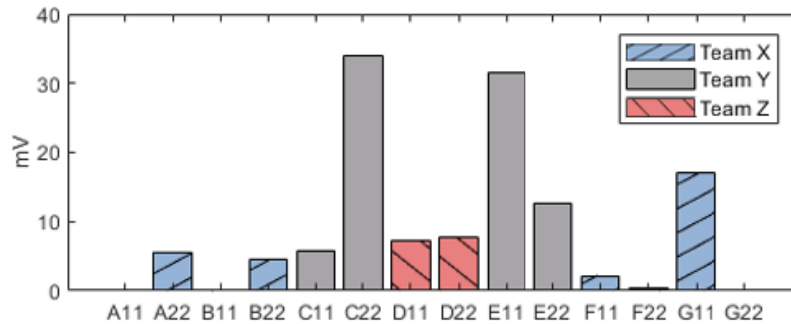
The impact of the ten most significant loops on eye height closure is shown in the loop diagram of Fig. 10. Here a TDR response from both the left- and right-side launches is paired with rectangular blocks whose lengths are proportional to their electrical length. The loops and their impact are shown below this. Applying Eq. (17) to the linearization error gives 2.6 mV and allows us to have confidence in the eye height reduction impact estimates that are much larger than this error.

The diagram in Fig. 10 combines the TDR response, the traditional way of investigating excessive reflections in a system, with the cascading  $S$ -parameter linearization that quantifies the impact of each resonant loop in the system.

Recall that our three fictional teams are trying to quantify and budget how each block in the system contributes to the total system reflection interference. Therefore, bins for each block return loss term collect the loop eye height reduction impact values. This analysis, shown in Fig. 11, illustrates the impact of the two connectors, blocks  $C$  and  $E$ , as well as the tertiary significance of the receiver package and vias, block  $G$ . Connector designs are often very difficult due to competing mechanical, thermal and electrical requirements. Although the connector design may be improved, it is interesting to note the impact of the receiver package/via junction of block  $G$ . Redesigning this portion of the interconnect could probably significantly improve the system with the least effort.



**Figure 10.** By pairing a (a) TDR plot, the traditional way of analyzing reflections, with (b) a diagram of the most impactful resonant loops, the quantifiable impact of each impedance discontinuity can be estimated. Note that (a) contains the TDR from the right and left sides of the network. In (b) the impact of each loop response of Fig. 8(b) is estimated by contrasting the actual total pulse response PDA eye height with the omitted loop pulse response PDA eye height. The vertical dashed lines in (a) show twice the approximate electrical length of each block shown in (b).



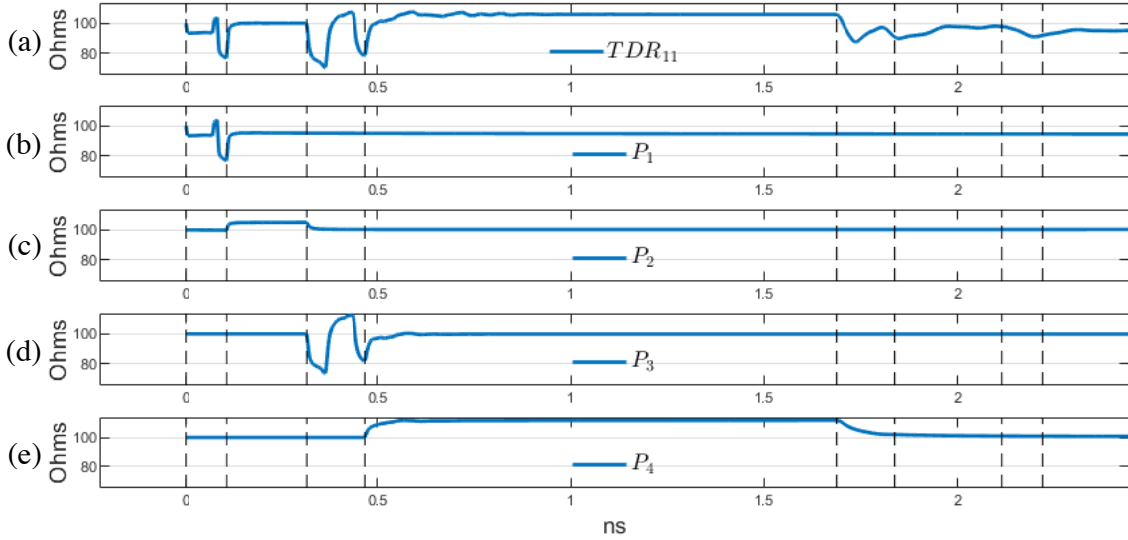
**Figure 11.** A reflection budget for each *S*-parameter reflection term in the network is found by attributing the impact of each loop response to the left and right return loss terms that form each resonant loop. Here we find that the connectors, block *C* and *E* are the most problematic, but it is also interesting that the receiver package ball and PCB model, block *G*, is the 3rd largest contributor to eye closure. The PDA metric of the decomposition error is 2.6 mV which sets the general uncertainty in this reflection budget.

The sources of reflective interference between blocks are identified, quantified, and associated with a team, as shown in Fig. 11. Team X cumulatively has 29 mV of PDA eye closure for blocks *A*, *B*, *F* and *G*, or 23% of the total. Team Y cumulatively has 84 mV of PDA eye closure for blocks *C* and *E*, or 65% of the total. Team Z cumulatively has 15 mV of PDA eye closure for block *D*, or 12% of the

total. This PDA eye closure view of the reflection budget supports the perspective that the connector is the primary contributor to reflection losses, but that the improvement of the line card and package impedance profile can reduce these losses with less effort than redesigning the connectors.

### 3.3. Time Domain Reflectometry (TDR) Reflection Budget

The preceding two subsections have seen the development of reflection budgets based on the linearization of the through response,  $S_{21}$ , in the frequency and time domains. These are directly relatable to existing ILD and PDA metrics. We propose a TDR decomposition and “impact” metric to budget the severity of each block on the actual total TDR variation shown in Fig. 12(a).



**Figure 12.** The actual total TDR (a) is decomposed into its direct paths of which the first four are shown in (b) through (e). For a 7-block system there are 7 direct paths. The sum of all the direct path responses forms an idealized TDR without any interactions or reflections between blocks as shown in Fig. 13. The vertical dashed lines approximate twice the electrical length of each block in the system.

As noted in Section 2, the 1st order CSLT can be applied to any system, not just the through path, by applying Eq. (12). To determine the TDR linearization for the worst case 7-block system, we have 7 direct paths, each of which interacts with (touch) a different set of the 21 loops. Assuming that each  $S$ -parameter block is symmetric, i.e.,  $A_{21} = A_{12}$ , then the seven direct paths are  $P_1 = A_{11}$ ,  $P_2 = A_{21}^2 B_{11}$ ,  $P_3 = A_{21}^2 B_{21}^2 C_{11}$ ,  $P_4 = A_{21}^2 B_{21}^2 C_{21}^2 D_{11}$ ,  $P_5 = A_{21}^2 B_{21}^2 C_{21}^2 D_{21}^2 E_{11}$ ,  $P_6 = A_{21}^2 B_{21}^2 C_{21}^2 D_{21}^2 E_{21}^2 F_{11}$ , and  $P_7 = A_{21}^2 B_{21}^2 C_{21}^2 D_{21}^2 E_{21}^2 F_{21}^2 G_{11}$ . The actual total  $S_{11}$  from Mason’s rule is:

$$S_{11} = P_1 + \frac{P_2 \Delta_2}{\Delta} + \frac{P_3 \Delta_3}{\Delta} + \frac{P_4 \Delta_4}{\Delta} + \frac{P_5 \Delta_5}{\Delta} + \frac{P_6 \Delta_6}{\Delta} + \frac{P_7 \Delta_7}{\Delta} \quad (18)$$

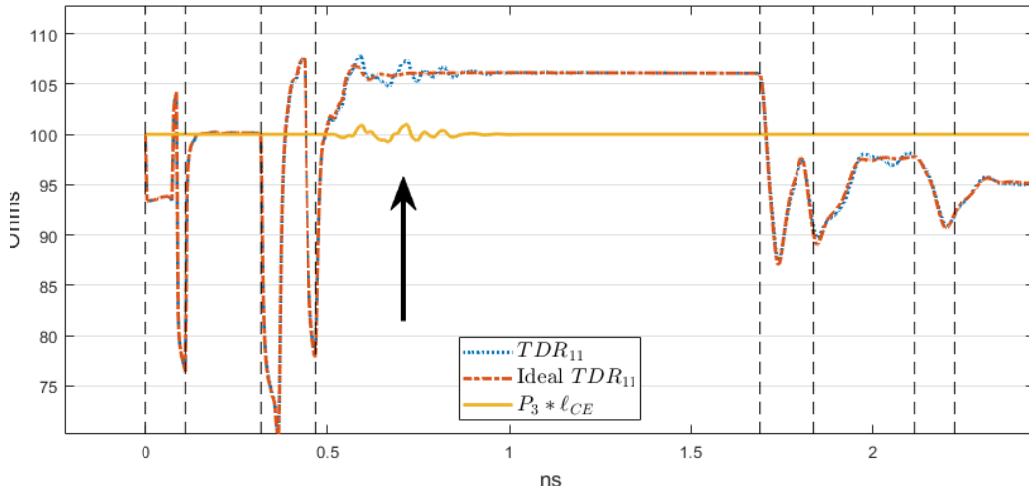
And its linearization is

$$\begin{aligned} \tilde{S}_{21} = & P_1 + P_2 \left(1 + \sum L_i\right) + P_3 \left(1 + \sum L_i\right) + P_4 \left(1 + \sum L_i\right) \\ & + P_5 \left(1 + \sum L_i\right) + P_6 \left(1 + \sum L_i\right) + P_7 \left(1 + \sum L_i\right) \end{aligned} \quad (19)$$

In Eq. (19), each of the direct paths,  $P_k$ , is multiplied by  $(1 +$  the loops that  $P_k$  touches), as expressed in Eq. (12). The first four direct paths of the TDR are shown in Figs. 12(b)–(e). These direct path TDR responses show the isolated impedance profile of each  $S$ -parameter block with the correct delay but without the reflective interactions between blocks. The TDR waveforms were calculated by first combining the numerous  $S$ -parameters components in the frequency domain and then converting

to the time domain with the inverse discrete Fourier transform to determine the impulse response. After converting this to a voltage step response,  $v(t)$  the TDR impedance is found by the transformation,  $z(t) = Z_0 \frac{1+v(t)}{1-v(t)}$ , where  $Z_0 = 100\ \Omega$  in our example.

The sum of all direct paths gives an idealized TDR without the resonant interactions between blocks. An overlay of the actual total and ideal TDR responses is shown in Fig. 13. Comparing these waveforms shows the impact on the TDR of the multiple reflections between blocks. The seven direct paths combine with the 21 resonant loops to create 91 path/loop TDR contributors for the 1st order linearization. The largest contributor is  $P_3 * \ell_{CE}$ , also shown in Fig. 13. Note that the region of the TDR plot identified by the vertical arrow shows a high degree of variation in the 4th segment within block  $D$ . Comparing the actual total TDR, the ideal TDR and the TDR loop response,  $P_3 * \ell_{CE}$ , we see that this variation is not due to variation of characteristic impedance of block  $D$ , as we might have initially assumed, but is instead due to the multiple reflection as embodied by the TDR loop response,  $P_3 * \ell_{CE}$ .

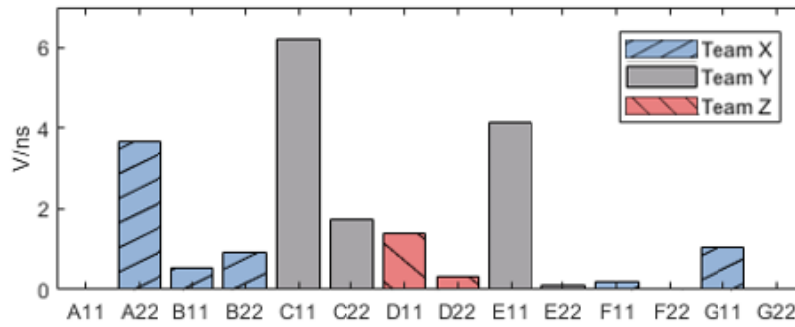


**Figure 13.** The TDR is decomposed into paths and loops. Comparing the actual total TDR with the idealized TDR illustrates how multiple reflections from blocks disturb the TDR waveform. The largest such resonant loop, from path  $P_3$  interacting with loop  $\ell_{CE}$ , is also shown. This view shows that the variation in TDR at the point indicated by arrow is due to reflective resonance and not to characteristic impedance variation.

To quantify how the variation of each decomposed TDR loop contributes to the variation of the actual total TDR, we introduce the following figure of merit (FOM):

$$\text{FOM}_{\text{TDR}} = \text{RMS} \left( \frac{d}{dt} z(t) \right) \quad (20)$$

where RMS is the root-mean-square operator,  $d/dt$  the derivative, and  $z(t)$  the TDR loop response waveform. This metric measures the variation in the TDR waveform and has been normalized to units of volts/nanoseconds. Each contributor has three reflection terms, one from the direct path and two from each loop. The value of the TDR metric is distributed to these three return loss bins and is aggregated in Fig. 14. As expected, the connector, blocks  $C$  and  $E$ , is the primary contributor to the TDR variation. However, since the TDR is a measure of the reflective behavior of the system instead of the through behavior like in the ILD and PDA budgets, the  $C_{11}$  bin is greater than the  $C_{22}$  bin, and the  $A_{22}$  bin is greater than the  $G_{11}$  bin (because only a fraction of the injected energy returns from the last block). Here Team X cumulatively has 6.37 V/ns of impact for blocks  $A$ ,  $B$ ,  $F$ , and  $G$ , or 31.4% of the total. Team Y cumulatively has 12.2 V/ns of impact for blocks  $C$  and  $E$ , or 60.1% of the total. Team Z cumulatively has 1.72 V/ns of impact for block  $D$ , or 8.4% of the total. In general, forming a TDR reflection budget is less directly applicable than the ILD and PDA budgets; however, these results confirm the observation that the connectors are the primary source of multiple reflections.



**Figure 14.** A reflection budget based on the TDR decomposition is found by quantifying the impact of each of the 91 path/loop responses with the RMS of the derivative of each TDR loop response and distributing the resulting metric to the three return loss bins associated with each path/loop combination. The connectors, blocks *C* and *E* are the largest contributors but the first block, where the signal energy is greatest, is the next most impactful. The RMS of the derivative of the TDR decomposition error is 0.97 V/ns.

#### 4. CONCLUSION

For high speed interconnects, reflective interference can severely limit the performance of the link and may be addressed through interconnect redesign or costly equalization circuitry. Through an illustrative example of three teams collaboratively designing a CEI 25G-LR interface, we have shown how the cascading *S*-parameter linearization technique (CSLT) can be used to identify and quantify sources of reflective interference. We explored reflection budgets for ILD, PDA, and TDR, and showed how each would be used to guide which block should be redesigned to best resolve the reflective interference. Using this technique can take what was previously considered reflective noise [10] and change it into reflective information for use in better understanding and reducing multi-path reflections. System integrators dealing with legacy backplanes, where the connector is known to be the primary source of reflections, can quickly identify the secondary sources of reflections and quantify how much system performance can be had through a particular block redesign. This provides a systematic and quantitative process for addressing excessive reflections which does not rely on the ‘art’ of signal integrity.

The three reflection budgets indicate the same source of the reflective interference, and each has advantages and disadvantages. The ILD budget is simple to calculate, as it and the input *S*-parameters are both in the frequency domain, and it only requires minimal pre-processing. The downside is that  $FOM_{ILD}$  is difficult to relate to the total system performance [26]. The PDA budget is calculated in terms of eye height closure, which is directly related to eye-opening margin, a very common signal integrity metric. The calculation is a bit more difficult than the ILD, as it requires converting the frequency domain response to the time domain response, which can be difficult for bandlimited, discrete *S*-parameter data [20]. The TDR budget provides interesting insights into the reflective response, rather than the through response, of the system, although the metric used may be difficult to relate to system performance and requires conversion to the time domain like the PDA budget.

It is anticipated that the PDA eye closure budget will be the most useful to design teams, since it is the most comparable to laboratory scope equipment and is directly relatable to the system bit error rate. All three budgets suffer from an unavoidable drawback that the use of nonlinear metrics overestimates the overall impact of each component.

The applications of the CSLT discussed here could be further refined by extending the technique beyond point-to-point interconnects to branching or flyby topologies for use in DDR interfaces. This would require a thorough analysis to find all the loops in the system and identify which ones touch each path as defined in Eq. (12). DDR transceiver circuitry is typically at best only weakly linear and time-invariant (LTI), and thus the impulse based analysis and metrics utilized in this paper would have a large systematic error. Therefore, relating a pair of impedance discontinuities to eye closure for DDR

systems would require linearizing the transceiver. Additionally, expanding the metrics beyond ILD and PDA to include statistical eye analysis [24] and channel operating margin (COM) metrics would be very helpful. Including a floating tap decision feedback equalization to allow for a direct comparison between addressing reflections with large and power-hungry circuits or through interconnect redesign would be very relevant. Lastly, an investigation of the role of reflections in mode conversion, i.e., single-ended to differential energy coupling studies would be interesting.

It is anticipated that several new applications will be found for the CSLT. One use being currently explored is application to channel sensitivity analysis to determine how close a channel is to a catastrophic resonance due to manufacturing variation of materials. Another use for the TDR decomposition could be found in inversion theory applications as an alternative to TDR impedance peeling algorithms [27, 28]. These decompositions have potential for machine learning applications where the high-speed interconnect is decomposed and summarized as a feature extraction method for analysis by artificial neural networks. Another potential application of the technique is analyzing interconnect crosstalk [29, 30].

## APPENDIX A. INSERTION LOSS DEVIATION

Insertion loss deviation (ILD) is a method of quantifying the extent of the reflective behavior of an insertion loss waveform as a function of frequency,  $f$ . The ILD is further summarized by a figure of merit (FOM) metric,  $\text{FOM}_{\text{ILD}}$ , which expresses the severity of the ILD. ILD is used in several standards including IEEE 802.3bj [10] and OIF [1].

ILD is the difference between the insertion loss, i.e., the dB of the through frequency response  $S_{21}(f)$ , and a polynomial line fitted to the insertion loss as expressed in Eqs. (A1) and (A2).

$$\text{ILD}(f) = 20 \cdot \log_{10} |S_{21}(f)| - \text{IL}_{\text{fitted}}(f) \quad (\text{A1})$$

$$\text{IL}_{\text{fitted}}(f) = a_0 + a_1\sqrt{f} + a_2f + a_4f^2 \quad (\text{A2})$$

The fitted insertion loss is found through a weighted least squares procedure where the weight is derived from the insertion loss itself to put more emphasis on the higher frequencies than the lower frequencies. Here  $\mathbf{a}$  is the vector of polynomial coefficients  $[a_0 a_1 a_2 a_4]$ ,

$$\mathbf{a} = (F^T W F)^{-1} F^T W Y \quad (\text{A3})$$

where  $F$  is the frequency matrix with the columns filled with  $f^0$ ,  $\sqrt{f}$ ,  $f$ , and  $f^2$  in units of GHz;  $W$  is a square weight matrix with the diagonal elements filled with  $1/|S_{21}(f)|^2$ ; and  $Y$  is the insertion loss in dB, i.e.,  $20 \cdot \log_{10} |S_{21}(f)|$ . Since  $|S_{21}(f)| < 1$  for passive structures and typically decreases with frequency, the weighting values range from about 1 to some larger values. Some standards define an iterative ILD fitting process that limits coefficients to certain ranges [1], but here we use an ILD with no coefficient bounds [10], since it is a linear operator and can thus be applied to the decomposed insertion loss responses.

The  $\text{FOM}_{\text{ILD}}$  in Eq. (A4) is found through a weighted root-mean-square process, using the weighting function,  $w(f)$  in Eq. (A5), which is proportional to the power spectral density of the waveform and includes terms that describe the bandwidth of the transmitter and receiver.

$$\text{FOM}_{\text{ILD}} = \sqrt{\frac{\sum (w(f) \cdot \text{ILD}(f))^2}{M}} \quad (\text{A4})$$

$$w(f) = \text{sinc}^2(f/f_b) \left( \frac{1}{1 + (f/f_t)^4} \right) \left( \frac{1}{1 + (f/f_r)^8} \right) \quad (\text{A5})$$

where  $f_b$  is the baud rate frequency;  $f_t$  is the transmitter filter bandwidth;  $f_r$  is the  $-3$  dB reference receiver bandwidth; and  $M$  in Eq. (A4) is the number of samples over which the summation occurs. In this paper we will utilize the linear property of the least squares operator where it is applied to each piece of the decomposed insertion loss,  $Y = Y_1 + Y_2 + \dots + Y_n$ , to obtain the ILD of each part. This linearity is illustrated for the ILD fit coefficients in Eqs. (A6) and (A7)

$$\mathbf{a} = (F^T W F)^{-1} F^T W (Y_1 + Y_2 + \dots + Y_n) \quad (\text{A6})$$

$$\mathbf{a} = \mathbf{a}_1 + \mathbf{a}_2 + \dots + \mathbf{a}_n \quad (\text{A7})$$



Unfortunately, the  $FOM_{ILD}$  metric is not linear, as expressed in Eq. (A8), and thus the cumulative impact of the decomposed metrics will be over-estimated. This is important to keep in mind in interpreting the decomposed  $FOM_{ILD}$  metric results.

$$FOM_{ILD}(Y_1 + Y_2) \leq FOM_{ILD}(Y_1) + FOM_{ILD}(Y_2) \quad (A8)$$

## APPENDIX B. PEAK DISTORTION ANALYSIS

Peak Distortion Analysis (PDA) [24] is a common signal integrity tool to estimate a link's worst-case eye and data pattern from the pulse response. For symbol time  $T$  and pulse response  $p(t)$ , PDA gives the worst-case upper eye limit as

$$s_1(t) = p(t) + \sum_{k=-\infty, k \neq 0}^{\infty} p(t - kT) \Big|_{p(t-kT) < 0} \quad (B1)$$

and the worst-case lower eye limit as

$$s_0(t) = \sum_{k=-\infty, k \neq 0}^{\infty} p(t - kT) \Big|_{p(t-kT) > 0}. \quad (B2)$$

Conceptually, the calculation of the worst-case upper eye limit can be thought of as taking the one symbol wide cursor portion of the pulse response,  $p(t)$ , and combining this with all prior and subsequent portions of the pulse response that are negative and will thus reduce the upper eye limit. Similarly, the worst-case lower eye is conditioned on collecting all positive portions of the pulse response that increase the lower eye limit.

The PDA eye height, Eq. (B3), illustrated in Fig. 7(b), is found by taking the difference between the upper and lower eye limits. The  $EH_{\max}$  operator returns the maximum eye height value.

$$EH(t) = s_1(t) - s_0(t) \quad (B3)$$

$$EH_{\max}(p(t)) = \max[EH(t)] \quad (B4)$$

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