Progress In Electromagnetics Research Letters, Vol. 95, 115–123, 2021

Design and Simulation of CMOS Circuit Structure for CTL-CTM Crosstalk Cancellation Method in High-Speed Interconnects

Huifang Sun[1, 2], Yafei Wang[1, 2, *], Yanxiao Zhao[1, 2], and Xuehua Li[1, 2]

Abstract—A circuit module for coupled transmission line channel transmission matrix (CTL-CTM) crosstalk cancellation is designed and simulated by using CMOS technology in a high-speed interconnection system. The module consists of an adder and a subtractor to realize analog addition and subtraction of digital signals. The adder is composed of CMOS transistor pair connected to an inverter at the next stage. The subtractor is composed of a current mirror as the load of CMOS differential pair. The crosstalk cancellation circuit module is simulated and verified by advanced design system (ADS) software. The designed adder and subtractor work well and have no significant difference with the ideal output, and the signal eye diagram recovered by the crosstalk cancellation circuit is of good quality, which solves the circuit implementation problem in the CTL-CTM crosstalk cancellation method.

1. INTRODUCTION

Crosstalk is a phenomenon of harmful noise interference from electrical signals in high-speed interconnected systems to adjacent channels. The main reason for crosstalk is the presence of electromagnetic coupling between the signals from different channels. A series of methods can be adopted to reduce the crosstalk on victim lines, such as inserting shielding lines between transmission lines, distributing decoupling capacitors, reducing the coupling length of transmission lines and reducing the thickness of the medium layer [1–4]. However, most approaches are at the expense of hardware resources allocation. In the background of smaller and smaller size of electronic products, the application range of these methods has become increasingly narrower.

The method of eliminating the crosstalk between microstrip lines based on coupled transmission line channel transmission matrix (CTL-CTM) in reference [5] is effective, but no specific circuit design and implementation is carried out. In this paper, a metal oxide semiconductor field effect transistor (MOSFET) is used to design the circuit for the proposed method. An adder and a subtractor are used as basic units to realize a crosstalk cancellation circuit. MOSFET in microwave semiconductor devices is widely used in radio frequency and microwave-integrated circuits due to its high performance, low power consumption, high integration, and low cost [6].

For the circuit module of CTL-CTM crosstalk cancellation method, two units of the circuit are first respectively designed by using four CMOS transistors. The adder [7–9] is composed of a CMOS transistor pair connected to an inverter at the next stage. The subtractor [10, 11] is composed of a current mirror as the load of CMOS differential pair. Then, the designed adder and subtractor are applied to the CTL-CTM circuit to cancel crosstalk, and the necessary impedance matching is performed [12]. Finally, ADS software is used to simulate the effectiveness of the adder and subtractor and the quality

Received 23 September 2020, Accepted 11 December 2020, Scheduled 28 December 2020

* Corresponding author: Yafei Wang (wangyafei@bistu.edu.cn).

[1] School of Information and Communication Engineering, Beijing Information Science and Technology University, Beijing 100101, China. [2] Key Laboratory of Modern Measurement and Control Technology, Ministry of Education, Beijing Information Science and Technology University, Beijing 100101, China.

of the signal eye diagram at the receiving end. The output effects of the adder and subtractor designed with MOSFET devices are good, and the eye diagram quality of the transmitted signal recovered by the crosstalk cancellation circuit is better than that of two normal transmission lines with the same parameters. The crosstalk cancellation circuit using CMOS technology is accurate and feasible, and the circuit is simple.

2. CROSSTALK CANCELLATION METHOD BASED ON CTL-CTM

The crosstalk cancellation method of CTL-CTM was proposed previously [5]. The fundamental is to describe the signal relationship between the ports of the transmission channel according to the transfer function of the channel model in Fig. 1, and to establish the CTL-CTM matrix reflected by Equation (1).

$$\mathbf{H} = \begin{pmatrix} H(\omega) & C(\omega) \\ C(\omega) & H(\omega) \end{pmatrix} \tag{1}$$

where $H(\omega)$ is the transfer function of microstrip lines, and $C(\omega)$ is the transfer function of the far-end crosstalk between microstrip lines.

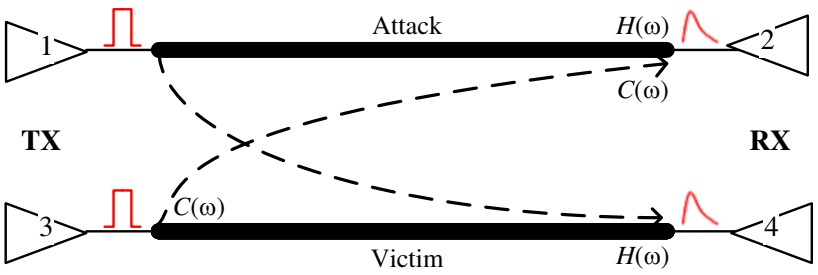


Figure 1. Channel model of two coupled microstrip lines.

Since the transfer function has the same physical meaning as the S-parameter in the interconnect lines, under weak coupling, $H(\omega)$ and $C(\omega)$ are as shown in Equations (2) and (3) [5].

$$H(\omega) = S_{21} = S_{43} = e^{\frac{-j(\Delta\beta)l}{2}} \cos\left[\frac{(\Delta\beta)\,l}{2}\right] \tag{2}$$

$$C(\omega) = S_{23} = S_{41} = -je^{\frac{-j(\Delta\beta)l}{2}} \sin\left[\frac{(\Delta\beta)\,l}{2}\right] \tag{3}$$

where $\Delta\beta = \beta_e - \beta_o$; β_e and β_o are respectively the even mode and odd mode propagation constants, and l is the coupled length.

The transfer function in Equation (1) is converted into a diagonal matrix by the eigen value decomposition (EVD) of CTL-CTM matrix, as in Equations (4) and (5). Then, transmission line signals are linearly combined and transformed to form orthogonal mode. So, the crosstalk transfer function is converted to zero. Finally, crosstalk cancellation effect is achieved.

$$\mathbf{H} = \mathbf{U}\Lambda\mathbf{U}^{-1} = \mathbf{U}\mathbf{\Lambda}\mathbf{U}^{\mathbf{H}} \tag{4}$$

$$\mathbf{\Lambda} = \begin{pmatrix} e^{-j(\Delta\beta)l} & 0 \\ 0 & 1 \end{pmatrix}, \quad \mathbf{U} = \begin{pmatrix} \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & -\frac{\sqrt{2}}{2} \end{pmatrix} \tag{5}$$

where $\mathbf{\Lambda}$ is the diagonal matrix formed by the eigenvalues of $\mathbf{H}$ matrix, and $\mathbf{U}$ is the unitary matrix composed by the eigenvectors of $\mathbf{\Lambda}$ matrix.

According to the above analysis, a crosstalk cancellation circuit model is constructed to obtain signal non-crosstalk transmission, as shown in Fig. 2. The transmission signal undergoes two linear combination transformations at the transmitting end and receiving end of the two interconnecting

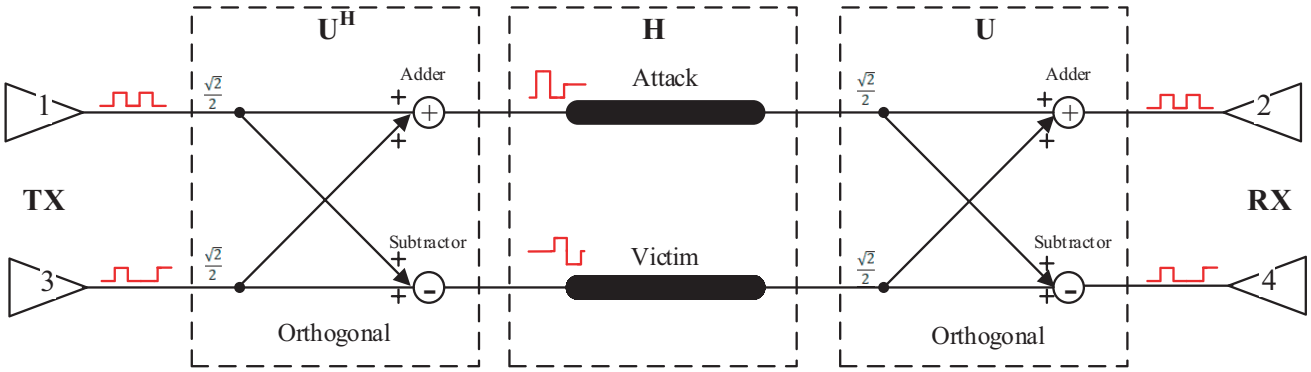


Figure 2. The model of crosstalk cancellation circuit.

lines. Thus, the transmission signal forms an orthogonal mode, and finally, the transmission signal is reconstructed.

Based on this model of crosstalk cancellation circuit in Fig. 2, the linear combination transformation process of the transmission signals at the transmitting end and receiving end are found to require addition and subtraction operation. So, adder and subtractor are important units in the entire circuit design. As common units in circuit system modules, adders and subtractors have many design methods. The crosstalk cancellation circuit is characterized by analog addition and subtraction of digital signals. Thus, this paper uses CMOS components to design the crosstalk cancellation circuit.

3. THE DESIGN OF CROSSTALK CANCELLATION CIRCUIT

This paper proposes the adder structure shown in Fig. 3, where the CMOS transistor pair is connected to an inverter at the next stage. It only needs four MOSFETs to implement adder and to form an inverter simply and easily, as follows: M_1 and M_2 are NMOS transistors, and M_3 and M_4 are PMOS and NMOS, respectively.

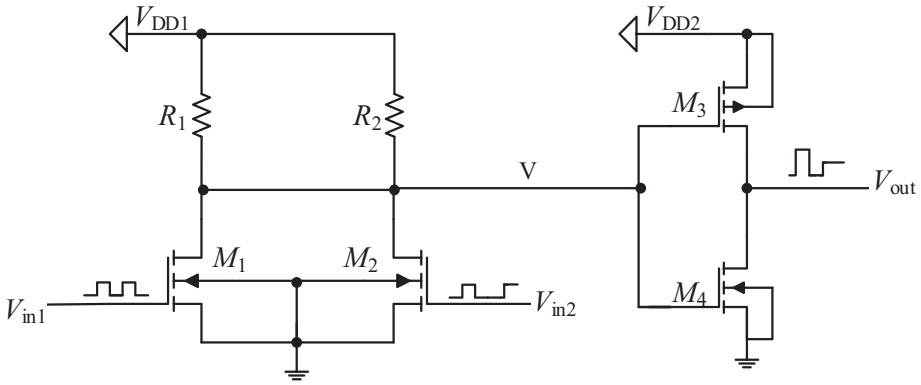


Figure 3. Structure of the adder.

To make the circuit work normally at low voltage, an inverter is connected to the output port V of the first stage, so that the final output port V_{out} is a full swing output, that is, negative voltage to positive voltage, which can better drive the next level and reduce time delay. This circuit structure of adder is simple and easy to achieve. Furthermore, the circuit structure by four MOSFETs is used to implement circuit function with the advantages of low power consumption and low cost.

Subtraction based on addition has been widely used in very large-scale integrated circuits. Thus, the current mirror load CMOS differential amplifier shown in Fig. 4 is used to form a simple subtractor,

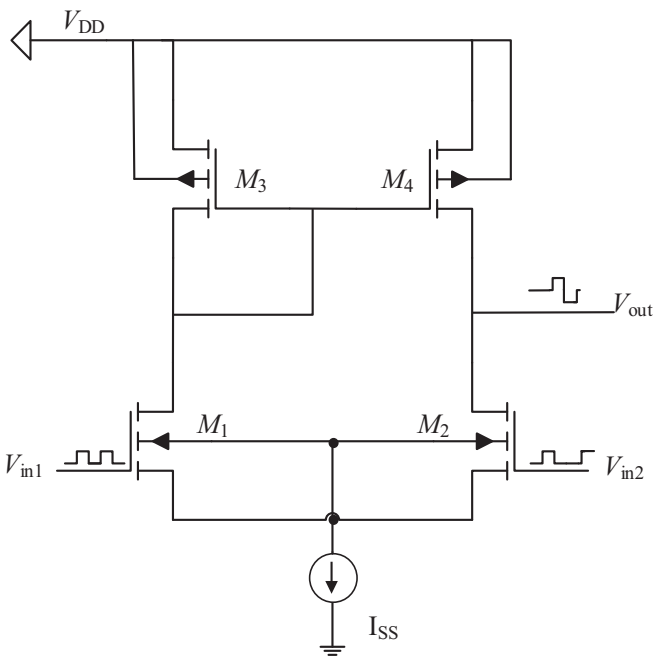


Figure 4. Structure of the subtractor.

which can convert the differential-mode output signal into a single-ended output signal. M_1 and M_2 use NMOS as signal input pair tubes, and M_3 and M_4 use PMOS as current mirror tubes. This circuit structure also achieves the required subtraction function by four MOSFET transistors, and the cost is low.

To verify the effectiveness of the input signal through the circuit including the adder and subtractor formed by MOSFET, a crosstalk cancellation circuit structure as shown in Fig. 5 is constructed.

The key of this circuit design is to match the characteristic impedance of the microstrip line to ensure integral signal transmission and achieve a good crosstalk cancellation effect. Commonly used impedance matching techniques include series terminal matching and parallel terminal matching. In

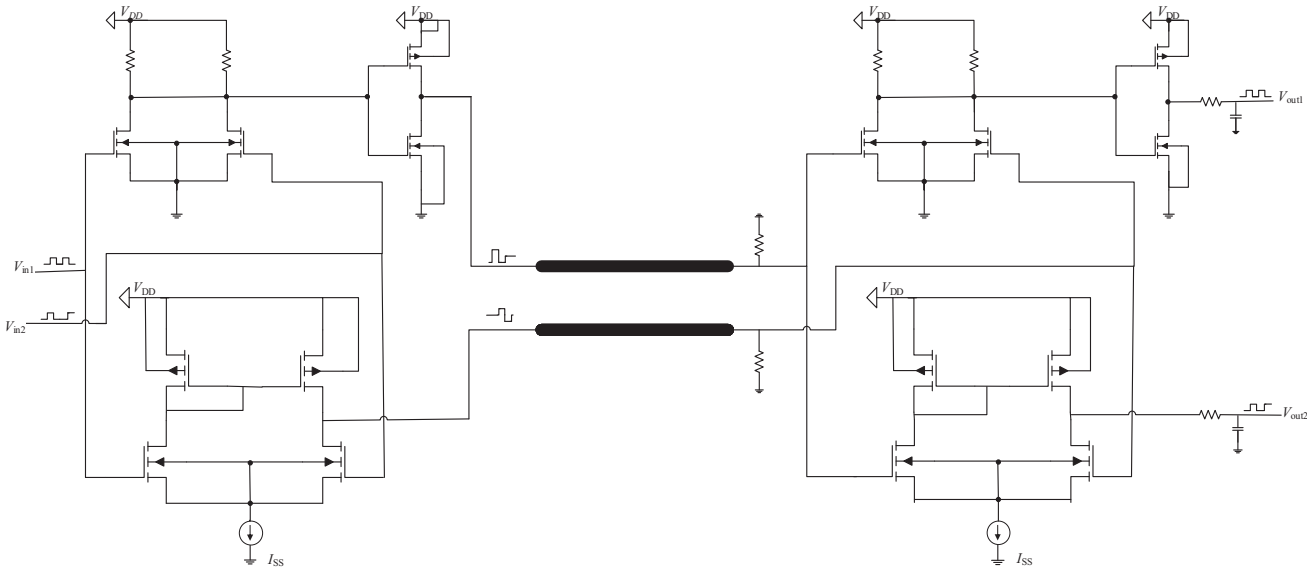


Figure 5. The circuit structure of crosstalk cancellation.

addition, the orthogonal transmission of the input signals between the two interconnects is reflected by respectively carrying out two times of addition and subtraction operations in the circuit. In this way, the input signals are reconstructed to achieve the purpose of crosstalk cancellation.

4. SIMULATION RESULTS AND ANALYSIS

The validity of the proposed circuit is simulated and verified by utilizing Keysight Technologies ADS2017 software. The output results of the adder and subtractor and the eye diagrams of the crosstalk cancellation circuit are simulated.

4.1. Adder Simulation

The CMOS device in the circuit is to call the MOSFET components in Devices-MOS of ADS Software. Then, simulation verification is performed according to the schematic diagram of the adder in Fig. 3. The basic parameters are shown in Table 1, where L is the channel length of the transistor, and W is the channel width of the transistor.

Table 1. Basic parameters of adder.

	M_1	M_2	M_3	M_4	V_{DD1}	V_{DD2}	R_1	R_2
L/μm	1	1	1.05	1.32	5 V	3 V	179 Ω	179 Ω
W/μm	330	330	255	424				

Simultaneously, the amplitude of the two input signals is set to 1 V. The transmission rate is 1 Gbit/s. The rise/fall time is 0.1 ns. The input data is shown in Fig. 6 as a pseudo-random sequence. The simulation results are shown in Fig. 7.

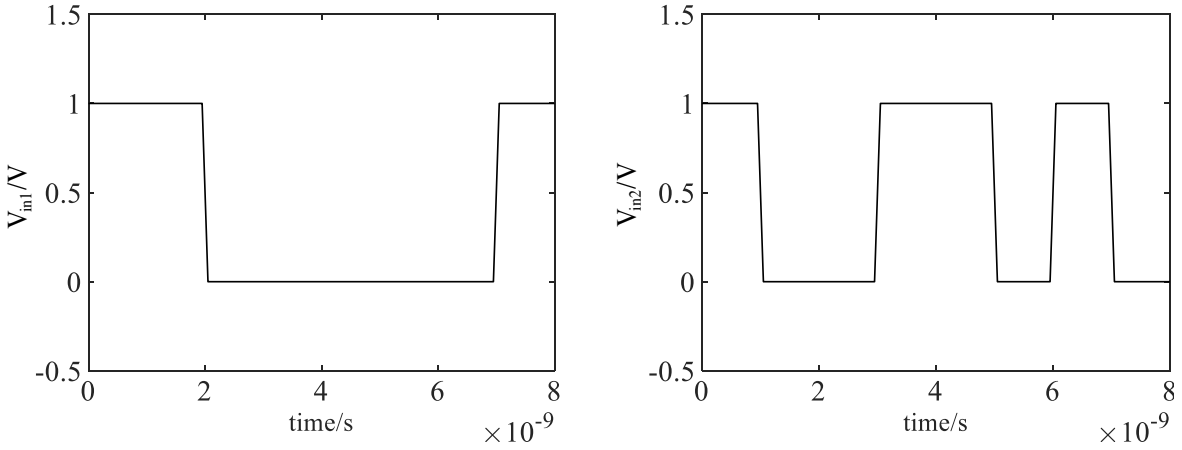


Figure 6. Two input signals of the adder.

Figure 7 shows that the output result of the adder constructed is the same as the ideal output result obtained by the equation $V_{\text{out\_ideal}} = V_{\text{in1}} + V_{\text{in2}}$. The simulation shows that this circuit structure can realize the addition function and work well. However, because the MOS tube is a nonlinear device, even when it works in the linear region, a little distortion will inevitably occur due to the device itself.

4.2. Subtractor Simulation

The schematic diagram of the subtractor also uses ADS software for simulation and verification according to Fig. 4. The basic parameters of the subtractor are shown in Table 2, where L is the channel length

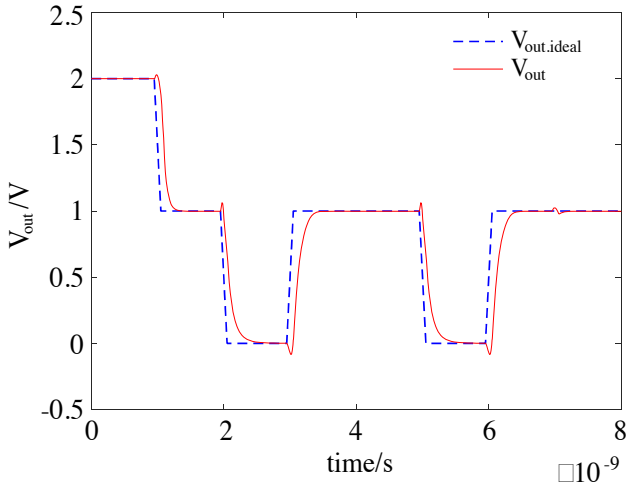


Figure 7. Output results of the adder.

Table 2. Basic parameters of subtractor.

	M_1	M_2	M_3	M_4	V_{DD}	I_{SS}
L/μm	2	2	1.07	1.07	5V	387mA
W/μm	6	6	100	100		

of the transistor, and W is the channel width of the transistor.

Simultaneously, the amplitude of the two input signals is set to 1 V. The transmission rate is 1 Gbit/s. The rise/fall time is 0.1 ns. The input data are shown in Fig. 8 as a pseudo-random sequence. The simulation results are shown in Fig. 9.

Figure 9 shows that the output result of the subtractor constructed is the same as the ideal output result obtained by the equation $V_{\text{out\_ideal}} = V_{\text{in1}} - V_{\text{in2}}$. The simulation result shows that this circuit can realize the subtraction function under high-rate signal input, and the effect is good.

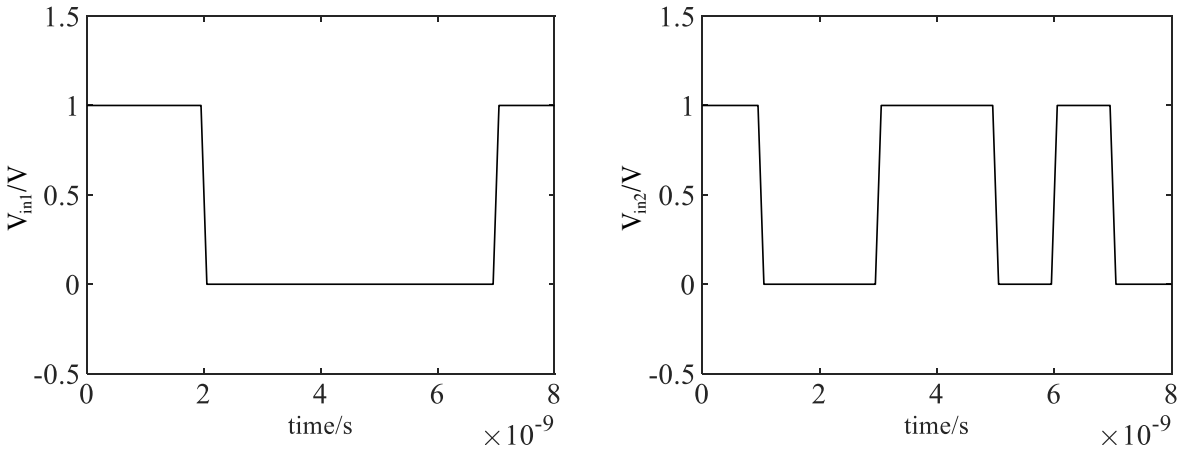


Figure 8. Two input signals of the subtractor.

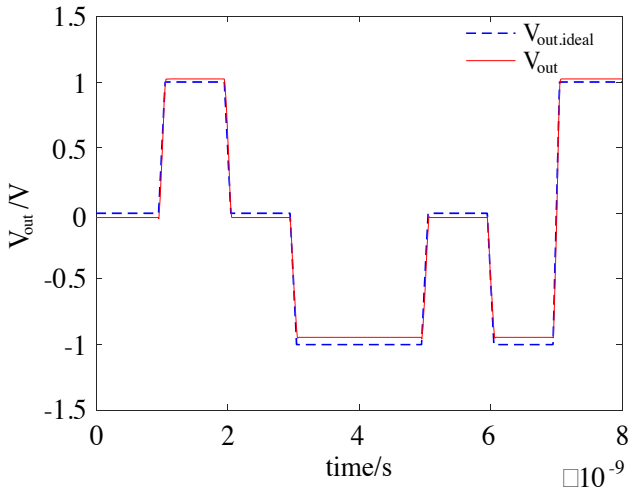


Figure 9. Output results of the subtractor.

4.3. Simulation of Crosstalk Cancellation Circuit

The above adder and subtractor are used in the structural layout of the crosstalk cancellation circuit in Fig. 5. The MACLIN2 of TLines-Microstrip is used to create two microstrip lines in parallel. The architecture parameters are as follows: width of the microstrip line $w = 40$ mil, medium height $d = 22$ mil, distance between adjacent microstrip lines $s = 20$ mil, line conductor thickness $t = 2.8$ mil, dielectric constant $\varepsilon_r = 4.5$, magnetic permeability $\mu_r = 1$, dielectric loss angle tangent $\tan\delta = 0.02$, and length of the microstrip line $l = 16$ inch. The conductor is copper. The characteristic impedance is 50 Ω. The transmission rate of input data is set as 1 Gbit/s. The rise/fall time is 0.1 ns, and the input data are pseudo-random sequence. The eye diagrams of the receiving signal on the microstrip lines are simulated before and after the method is used.

Before and after the method is used, when the signals of the input end are synchronized symbols, the comparison results of the eye diagrams are as shown in Fig. 10. When the phase difference of the two signals has a half symbol, the comparison results of the eye diagrams are as shown in Fig. 11.

In the above two cases, the results show that the designed circuit can improve the width and height

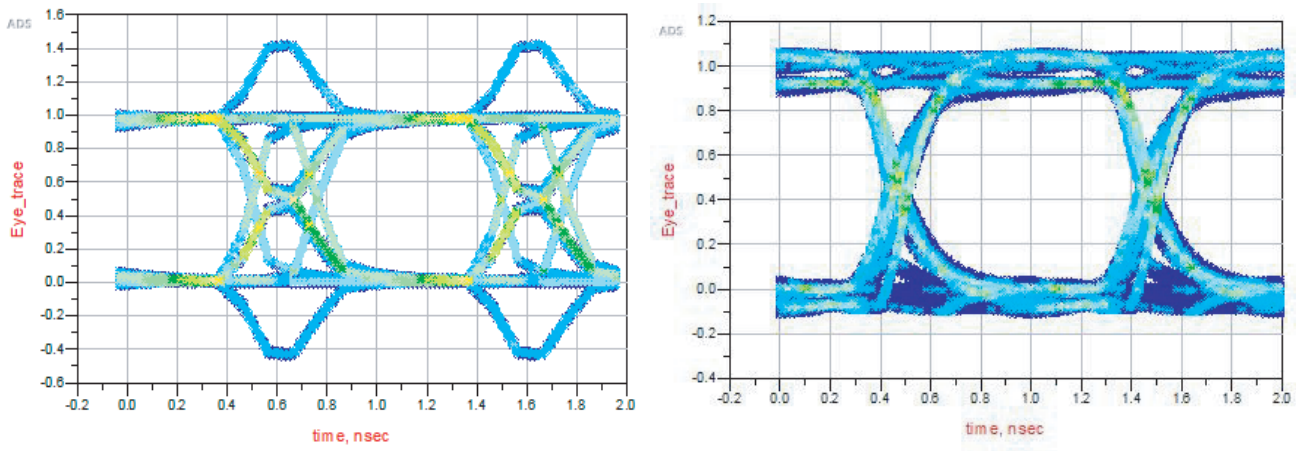
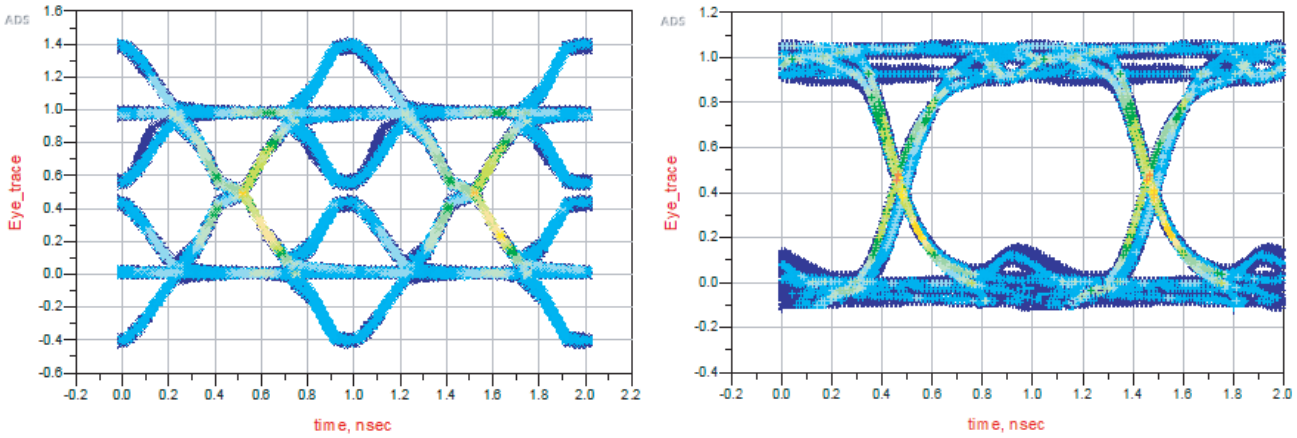


Figure 10. Eye diagrams under synchronizing symbols. (a) Before using the method. (b) After using the method.



(a) (b)

Figure 11. Eye diagrams under a half symbol. (a) Before using the method. (b) After using the method.

of the eye diagram and reduce jitter. The eye diagram caused by crosstalk nearly is closed especially when the phase difference of the transmitted signal has a half symbol. After the signal is processed by the CMOS circuit, the jitter and noise are reduced.This proves that the method of forming a crosstalk cancellation circuit based on CMOS technology is effective. Simulation shows that the adder and subtractor designed with MOSFET work well, and the signal eye diagram recovered by the crosstalk cancellation circuit is of good quality. The crosstalk cancellation circuit using CMOS technology is accurate and feasible.

The circuit designed in this paper also has the advantage of low power consumption. The addition circuit and subtraction circuit designed in this paper can achieve the required functions by using only four CMOS transistors, which greatly reduces the power consumption. Furthermore, the circuit structure adopts symmetrical structure, which reduces the parasitic capacitance and the power consumption of the circuit.

For $n \geq 3$ transmission lines, the structure of CMOS circuit will be designed by the CTL-CTM matrix in [13] in the following work.

5. CONCLUSION

A circuit for CTL-CTM crosstalk cancellation in high-speed interconnection system is designed and implemented by using CMOS technology. The scheme is composed of two units, as follows: an adder composed of a CMOS transistor pair connected to an inverter at the next stage and a subtractor composed of a current mirror as the load of CMOS differential pair. Analog addition and subtraction of digital signal in crosstalk cancellation circuit can be implemented. Then, the whole structure is symmetrical, sharing 16 CMOS transistors to realize the circuit of crosstalk cancellation. The simulation results show that the adder, subtractor, and crosstalk cancellation circuit based on CMOS have good output results, and the circuit structure is simple and easy to implement.The proposed circuit can be used in various signal processing applications such as oscillators, trans-conductance amplifier, and sensor interface.

ACKNOWLEDGMENT

This work is supported by the Young Scientists Fund of the National Natural Science Foundation of China (Grant No. 61601038).

REFERENCES

1. Mudavath, R. and B. R. Naik, "Estimation of far end crosstalk and near end crosstalk noise with mutually coupled RLC interconnect models," *2018 International Conference on Communication and Signal Processing (ICCSP)*, 182–185, Chennai, India, 2018.
2. Huang, B., K. Chen, and C. Wang, "Far-end crosstalk noise reduction using decoupling capacitor," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 58, No. 3, 836848, 2016.
3. Lee, K., H. Lee, H. Jung, et al., "A serpentine guard trace to reduce the far-end crosstalk voltage and the crosstalk induced timing jitter of parallel microstrip lines," *IEEE Transactions on Advanced Packaging*, Vol. 31, No. 4, 809–817, 2008.
4. Halligan, M. S. and D. G. Beetner, "Maximum crosstalk estimation in weakly coupled transmission lines," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 56, No. 3, 736–744, 2014.
5. Wang, Y., H. Sun, and X. Li, "Non-crosstalk scheme based on linear combination transformation in high-speed interconnects," *Progress In Electromagnetics Research Letters*, Vol. 85, 45–50, 2019.
6. Skotnicki, T., J. A. Hutchby, T.-J. King, H.-P. Wong, and F. Boeuf, "The end of CMOS scaling: Toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits and Devices Magazine*, Vol. 21, No. 1, 16–26, Jan.–Feb. 2005.
7. Wang, Y. and X. Li, "Crosstalk cancellation method based on unitary transformation of coupled transmission lines-channel transmission matrix," *Progress In Electromagnetics Research Letters*, Vol. 52, 45–50, 2015.
8. Oh, T. and R. Harjani, "A 6-Gb/s MIMO crosstalk cancellation scheme for high-speed I/Os," *IEEE Solid-State Circuits*, Vol. 46, No. 8, 1843–1856, Aug. 2011.
9. Wang, C., H.-M. Lam, and X. He, "A high-voltage analog adder based on class-B amplifier for source driver of AMOLED EXTERNAL COMPENSATION SCHEme," *SID Symposium Digest of Technical Papers*, 54, 2017.
10. Bansal, N. and R. Pandey, "A novel current subtractor based on modified wilson current mirror using PMOS transistors," *2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, 444–449, Ghaziabad, 2016.
11. Gupta, R., R. Gupta, and S. Sharma, "High performance full subtractor using floating-gate MOSFET," *Microelectronic Engineering*, Vol. 162, 75–78, 2016.
12. Bliskavitski, A. K., Y. K. Vladimirov, and S. K. Taktashov, "Microwave impedance matching of a laser diode to a microstrip line with a 50-Ω characteristic impedance," *Quantum Electronics*, Vol. 23, No. 3, 251, 1993.
13. Wang, Y. and X. Li, "Crosstalk cancellation study of eigen value decomposition of n-channel transmission matrix," *Chinese High Technology Letters*, Vol. 28, No. 4, 320–326, 2018.