Progress In Electromagnetics Research Letters, Vol. 93, 123–130, 2020

Research on DM Conducted EMI Suppression Method of Switching Power Supply

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Abstract—On the basis of serious electromagnetic interference (EMI) produced by power electronic equipment, coupling capacitance existing between transistor and transistor is considered as the main factor disturbing differential-mode (DM) loop. Calculation model of coupling capacitance is established by using FEM (Finite Element Method) and moment method, and computing method is also derived. EMI improvement method for converter system is proposed by controlling the coupling capacitance impedance. Experimental results show that changing the placement distance and position of the transistor can reduce the conducted interference.

1. INTRODUCTION

The starting point for studying electromagnetic compatibility (EMC) optimization is to consider three elements of EMC: 1) reduce or suppress the EMI generated by the interference source; 2) cut off or change the coupling path; 3) improve the anti-interference ability of sensitive equipment [1]. At present, the main methods for suppressing conducted EMI are: soft switching technology, modulation technology, PCB board optimization design technology, and EMI filter [2]. Soft switching technology and modulation technology are widely used in product development and design stage. It is a relatively mature technology at present [3]. PCB optimization design technology will increase R&D costs, and the addition of EMI filters will increase product volume and weight [4]. Changing the permittivity and thickness of the thermal conductive adhesive filled between the transistor heat-conducting plate and heat sink can reduce the conducted interference. But this method is only suitable for suppressing the low-frequency DM interference within 10 MHz, and when the power device works for a long time [5], it will make the thermal conductive grease invalid [6, 7].

Based on this, this paper takes the widely used switching power supply as an example. Through analysis, it is determined that the coupling capacitance between the power devices is the main factor affecting the DM interference. In the product design process, the designer can increase the DM impedance by adjusting the placement and distance of the device to achieve the effect of suppressing conducted EMI. Compared with the existing filtering technology, the principle is simple, easy to implement, and almost no additional materials and design cost.

2. COMPONENT MODEL

Part of the circuit schematic of the full-bridge buck converter is shown in Figure 1. $D5$ and $D6$ represent the diode rectifier silicon stack [3].

Received 2 July 2020, Accepted 4 August 2020, Scheduled 7 October 2020
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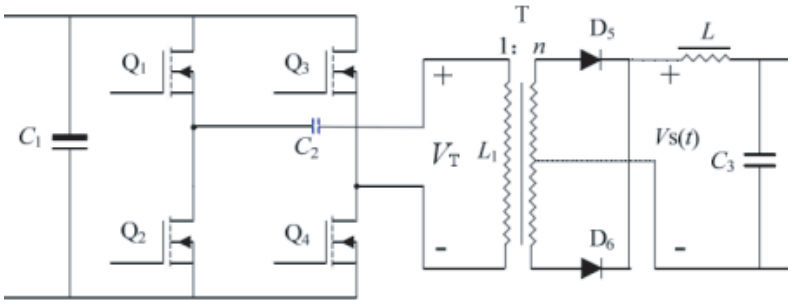

Figure 1. Full-bridge buck converter.

2.1. Effect of Parameters on Interference

The DM interference circuit is shown in Figure 2.

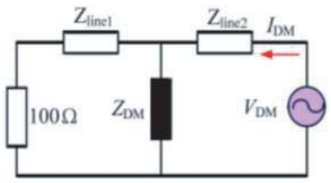

Figure 2. DM EMI equivalent circuit.

In Figure 2, V_{DM} represents the source of DM interference, Z_{line1} the line impedance, Z_{line2} the impedance of other devices in the loop, Z_{DM} the impedance formed by the coupling capacitance between the power devices, and $100\,\Omega$ resistance represents the two $50\,\Omega$ resistances of LISN in series. The impedance of the DM loop is:

$$Z_{DM-loop} = \frac{(100 + Z_{line1})Z_{DM}}{100 + Z_{line1} + Z_{DM}} + Z_{line2} \tag{1}$$

Z_{line1} and Z_{line2} are inherent values of the system.

It can be seen that increasing the impedance of the parasitic parameters in the loop can reduce the interference current.

2.2. Parameter Extraction

There are multiple power devices on the PCB, and each device has a capacitance c_{jj} to ground, and a coupling capacitance c_{ij} exists between the two devices. The capacitance matrix can be solved by solving the induced charge on the power device. Since there are a corresponding injection voltage on each power device and a coupling capacitance between the power devices, the total charge of each induction is as follows:

$$Q_j = C_{j1}V_1 + C_{j2}V_1 + \ldots + C_{jn}V_n \tag{2}$$

In the formula, n is the total number of power devices. Combine the finite element method and the moment method [3] to solve the induced charge Q. Solve the electrostatic field equation in the region as:

$$\begin{cases} E = -\nabla\phi \\ \nabla \times E = 0 \end{cases} \tag{3}$$

$$D = \varepsilon E \tag{4}$$

where ε is the dielectric constant, E the electric field strength, D the electrical displacement vector, and ϕ the scalar potential.

The finite element method is used to solve the power device surface layer, and the moment method is used to solve the problem internally. By injecting a specific voltage vector V, a unit pulse voltage P is generated on each device, assuming that a set of charge coefficients is α_j, then

$$\rho = \sum_{j=1}^{N} \alpha_j P_j(x, y, z) \tag{5}$$

$$\phi = \int_V \frac{\rho}{d} dV \tag{6}$$

Through Equations (5) and (6), the charge distribution density ρ and induced potential ϕ of the device body can be calculated, compared with a specific voltage vector V. If it is not equal, change the charge coefficient α_j and iteratively calculate again, until a set of charge coefficients is found, and the calculated ϕ is equal to the specific voltage vector V. Finally, the induced charge Q is obtained, so that the capacitance matrix C can be obtained.

3. EMI SUPPRESSION PRINCIPLE

In a DC power converter, the distribution of DM parasitic parameters is shown in Figure 3

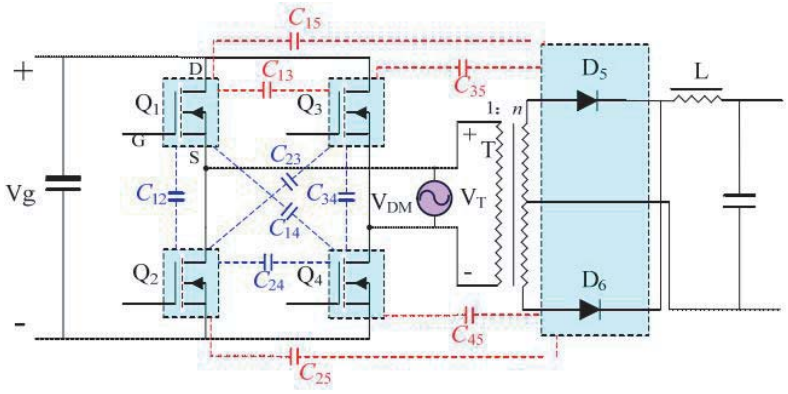

Figure 3. DM coupling capacitance distribution.

The coupling capacitances that affect the DM interference propagation path are C_{12}, C_{24}, C_{14}, C_{23}, and C_{34}. The drains of MOSFETs Q1 and Q2 are connected, and the drain is connected to the metal thermal conductive plate, so C_{14} and C_{34} are connected in parallel; C_{12} and C_{23} are connected in parallel; C_{24} exists between the two arms. The source of system DM interference is the turn-on or turn-off voltage across the switching device.

The area of the MOSFET thermal pad is 220 mm^2; the area of the diode silicon stack thermal pad is 680 mm^2; the relative dielectric constant of thermal grease is $\varepsilon_r = 8$; the thickness of thermal grease is $d = 2.2$ mm. The device placement is shown in Figure 4.

The DM coupling capacitance and common mode (CM) parasitic capacitance at different placement positions are calculated through finite element simulation. Equation (7) is the calculated capacitance matrix at the position in Figure 4.

$$C = \begin{bmatrix} 14.452 & 0.01082 & 4.20E-5 & 2.2021E-7 & 8.245E-9 \\ & 14.314 & 0.010811 & 4.118E-5 & 1.521E-8 \\ & & 14.314 & 0.01122 & 1.081E-8 \\ & & & 14.452 & 5.042E-8 \\ & & & & 52.132 \end{bmatrix} \text{pF} \tag{7}$$

In matrix of Eq. (7), the main diagonal element is the CM parasitic capacitance of each power device in the system to ground, and the remaining elements are the DM coupling capacitance between

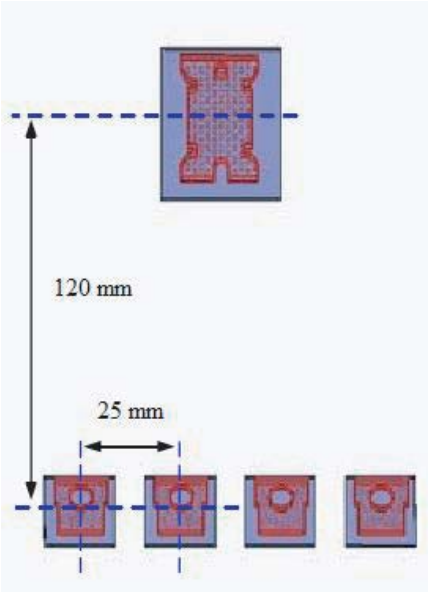

Figure 4. Position of power devices (Position 1).

power devices in the system, which is also explained by $C_{ij} = C_{ji}$. Different placements of power devices will affect the DM interference propagation of the system, and they will not affect the system's CM interference propagation.

Therefore, different positions of power devices have an impact on the DM interference propagation of the system and will not affect the CM interference propagation of the system [3, 4].

4. EXPERIMENTAL VERIFICATION OF EMC SCHEME

The relative dielectric constant of thermal grease is $\varepsilon_r = 8$; the thickness of thermal grease is $d = 2.2\,\text{mm}$; the area of the MOSFET thermal pad is $220\,\text{mm}^2$; the area of the diode silicon stack thermal pad is $680\,\text{mm}^2$. The physical layout is shown in Figure 5. Time domain measurement uses N2873 active current clamp and Agilent analog-to-digital hybrid oscilloscope DSO7104B. Frequency domain measurement uses FCC current probe, coaxial cable, and Agilent N9000A spectrum analyzer.

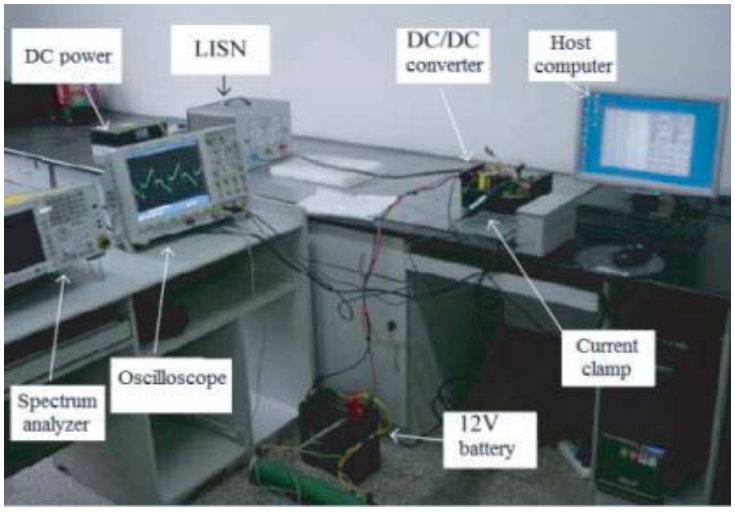

Figure 5. Experiment platform for checking EMI optimization plan.

We change the relative distance and position of the five power devices of the DC/DC converter, and the result of the influence of the power device placement distance on the DM current can be verified. In Figure 5, the corresponding DM current can be observed through an oscilloscope.

The distance among the five power devices is changed, and the relative placement mode is unchanged, as shown in Figure 6.

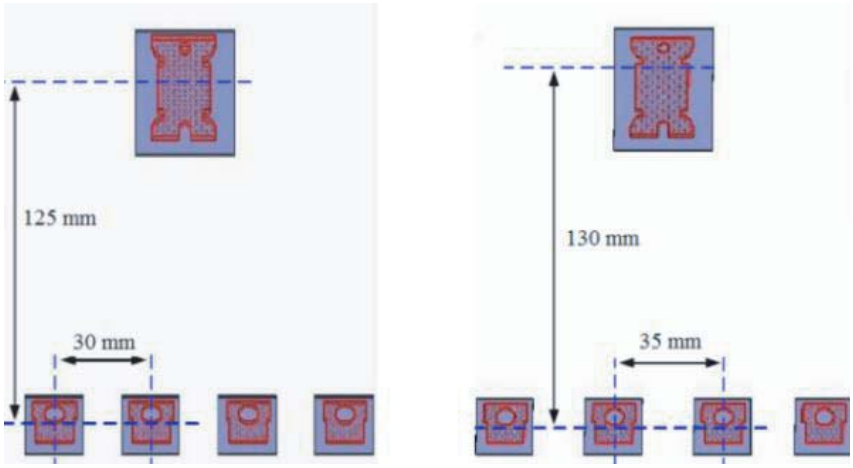

Figure 6. Adjust the distance of the power devices. (a) Position 2. (b) Position 3.

When the power devices are placed at different distances, the simulation results of the impedance characteristics of the system DM loop are shown in Figure 7.

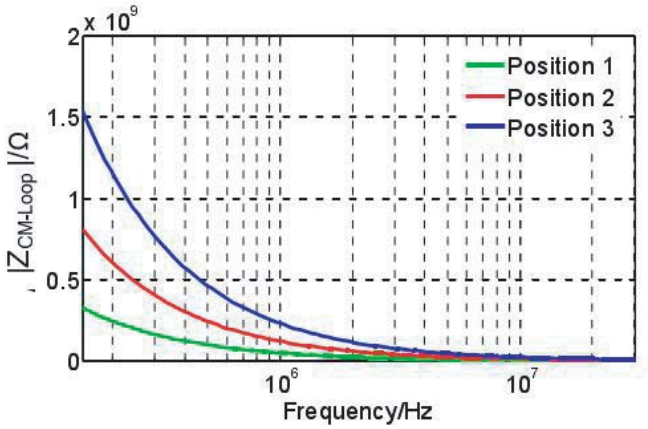

Figure 7. Frequency-impedance characteristic of DM equivalent circuits.

Through circuit simulation calculation, the effect of different placement positions on the system DM current is shown in Figure 8.

Change the placement and location of power devices, as shown in Figure 9.

Under the premise of unchanged relative distance, change the placement of power devices, as shown in Figure 10.

The time domain characteristics of the power device placement positions 1, 4, 5, 6 are shown in Figure 11.

The frequency domain characteristics of the power device placement positions 1, 4, 5, 6 are shown in Figure 12.

It can be seen that different distances and different placement methods have an impact on the DM conducted EMI interference of the switching power supply. In order to suppress the DM conducted

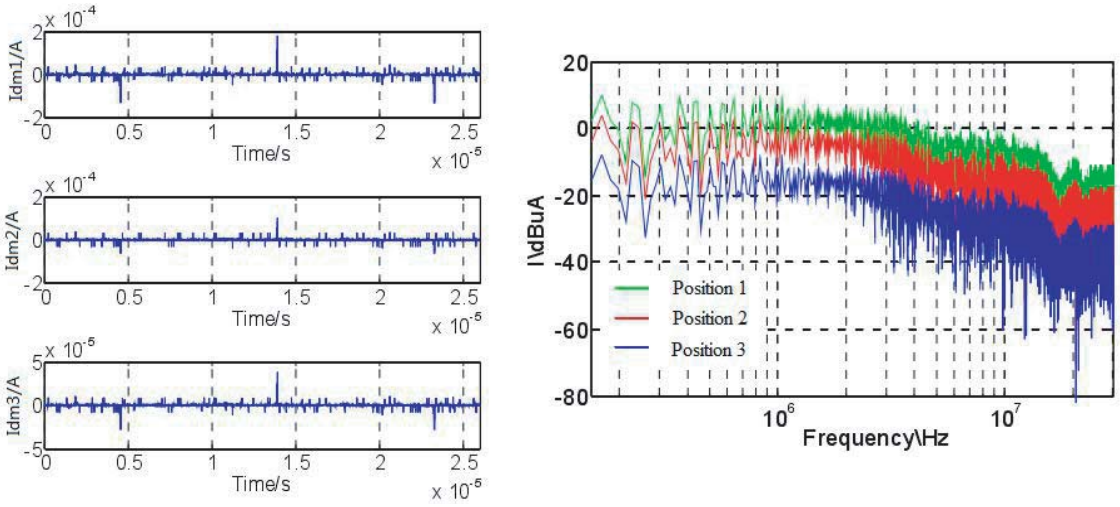

Figure 8. Comparison of DM current simulation results in differernt positon. (a) DM current in time domain. (b) DM current in frequency domain.

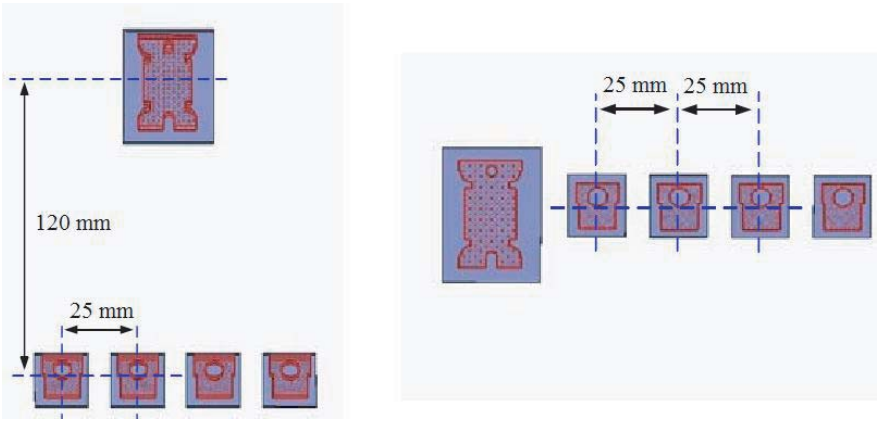

Figure 9. Different position of power devices. (a) Position 1. (b) Position 4.

Figure 10. Different placement of power devices. (a) Position 5. (b) Position 6.

EMI, this method can be used in the product design stage. Under the condition of space permitting, the greater the distance is between power devices, the stronger the EMI suppression capability is. In order to improve the integration of switching power supplies, power devices should be arranged with silicon stack as the center and the switching tubes arranged in a circle, which can effectively reduce DM interference.

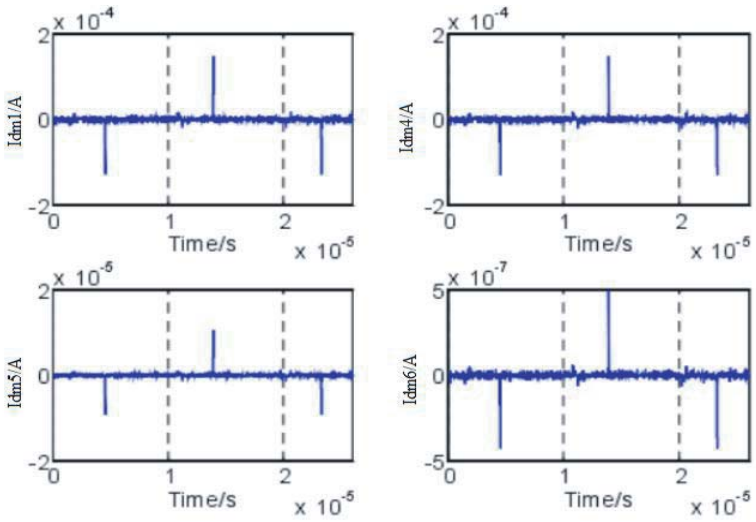

Figure 11. DM current in time domain.

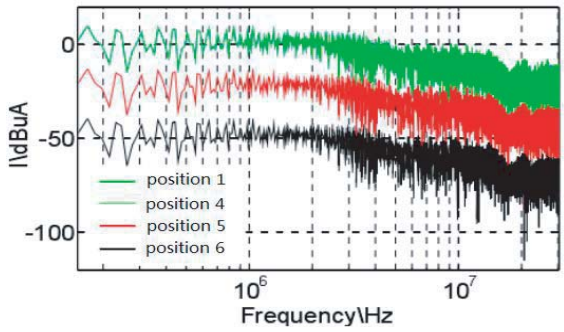

Figure 12. DM current in frequency domain.

5. CONCLUSION

The experimental results show that the relative distance and position of the power devices have an impact on the system DM conducted interference. The greater the mutual distance is between the power devices, the more obvious the DM suppression effect is, but the greater the distance is between the devices, the greater the volume of the product is, in the design stage, by adjusting the relative position of the power device, thereby reducing the level of DM conducted EMI. This EMI optimization method has little additional cost, compared with the filter greatly reducing the weight and volume of the converter, suitable for use in the EMC design stage of the product.

ACKNOWLEDGMENT

This work is partially supported by the Key Program of Guangyuan Science and Technology Bureau Project (2019ZCZDYF002); Sichuan Information Vocational and Technical College 2020 Research Project (2020KC19). The authors would like to express their sincere thanks to the referees for their valuable suggestions and comments.

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