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A Low-Parasitic CMOS Transistor Structure for Wide Locking Range ILFD Design

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Abstract—A wide locking range injection locked frequency divider (ILFD) with a low power consumption for 60 GHz applications is presented. The locking range of the ILFD is enhanced by reducing the parasitic capacitances of the transistors. The cross-coupled transistor and injected transistors are integrated to become a compact structure, which exhibits simple routing and induces less parasitic capacitances. To verify the proposed structure, the ILFD was fabricated using 65 nm CMOS technology. It has a measured locking range of 55.3 GHz to 67 GHz (19%) with 0 dBm input power. The circuit dissipates 1.98 mW at 0.5 V supply voltage without the output buffers.

1. INTRODUCTION

The unlicensed 7 GHz bandwidth at 60 GHz is now available for high data rate transmission. In such wide band transceivers, most speed-demanding circuits are the voltage-controlled oscillator (VCO) and the pre-scaler in a phase-locked loop design [1]. An injection-locked frequency divider (ILFD) is more attractive than the other type dividers due to its lower power consumption and higher operating frequency. However, the traditional ILFD design suffers from a narrow locking range. Some methods have been proposed to enhance the locking range of the ILFD by employing a shunt-peaking technique [2], tuning the varactor [3], using switching inductor [4, 5], forward body bias technology [6], using high order resonators [7], and frequency-tracking technology [8]. In these references, the ILFDs are usually more complicated, occupying a larger chip area and consume more power. In this letter, a novel low parasitic CMOS transistor structure is presented, which can integrate the cross-coupled transistors and injected transistors. Using this device, the layout routing of our ILFD is greatly facilitated. The parasitic capacitance is also reduced. So a high-performance ILFD is obtained.

2. CIRCUIT DESIGN

A conventional direct injection scheme based on a MOS transistor switch over the tank is shown in Fig. 1(a). The injection-locked oscillator is composed of a cross-coupled NMOS pair, a center-taped inductor, and a direct injection transistor. The LC tank absorbs the parasitic capacitor into the resonator. It consists of the parasitic capacitor of the coupled pair, the injection transistor, the load capacitor of the next stage, and the interconnected metal path. The locking range satisfies the following equation [9]:

$$|\Delta\omega|_{\max} \propto \left|\frac{\alpha_2 V_i}{C}\right| \tag{1}$$

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where V_i is the amplitude of the input signal, α_2 the second order nonlinear coefficient of the injection transistor, and C the capacitance of the resonator. According to the equation, the locking range can be improved by reducing the parasitic capacitances.

In contract of the RF NMOS layout structure of the single transistor configuration (M3), as different fingers are used for drain and source terminals, both terminals will have different parasitic values. To

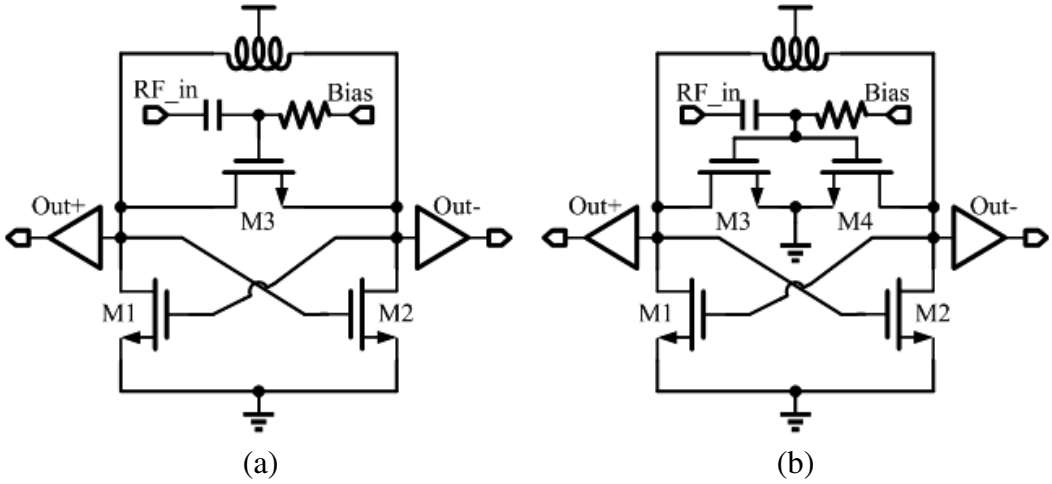

Figure 1. Circuit schematics of direct ILFDs: (a) Conventional ILFD, (b) proposed ILFD.

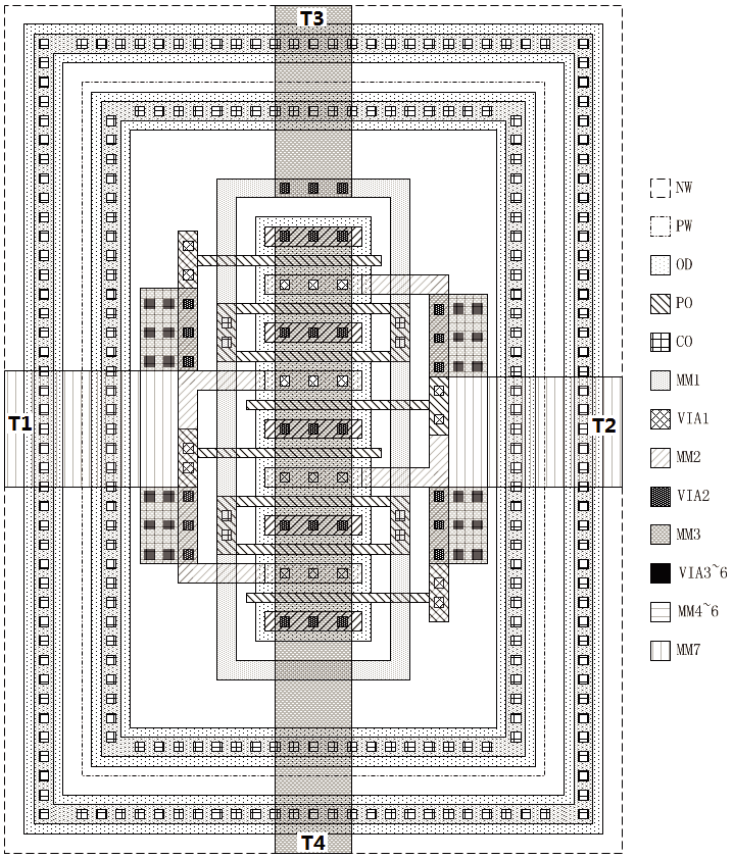

Figure 2. Proposed low parasitic CMOS 4 terminal transistor structure.

eliminate it, two transistors injection method is proposed to replace a single transistor as shown in Fig. 1(b). In addition, for the same g_m of injection, the size of symmetry structure should be double of the single transistor. This induces more parasitic capacitance and might worsen the locking range. However, the common sources of the symmetry injection transistors are connected to ground, the switch on time is larger than the convention structure during every period, and the injection current is also larger. This is more significant than the impact of the twice size of injection transistor. Furthermore, a new layout structure is proposed to reduce the parasitic of injection transistors.

The cross-coupled transistors have some common nodes with each other, so they can be built on a single standard RF transistor cell [10]. In our circuit, the gate of M1, the drain of M2, and the drain of M4 are connected together while the gate of M2, the drain of M1, and the drain of M3 are also connected together. The sources of M1 to M4 are connected to the ground as well. Due to this special configuration, the injection and cross-coupled transistors can be built on a single transistor cell. Fig. 2 shows the layout of two fingers of each M1 to M4. The proposed transistor structure reduces the number of source and drain fingers. And the gate of M1, the drain of M2 and M4 are tied directly with shorter metal path and then leave the transistor cell via Metal-7 (T1). The gate of M2, the drain of M1 and M3 are tied directly with shorter metal path and then leave the transistor cell via Metal1-7 (T2). The gates of M3 and M4 form a ring via Metal-2 (T3). All the source terminals are tied together via Metal-3 (T4). It can be configured as a four-terminal transistor cell.

From the simulation, the two ILFDs are designed for 60 GHz operation with $L_{\text{tank}} = 450$ pH. Their self-resonant frequencies are 59.1 GHz and 62.3 GHz, respectively. It means that the capacitance of the tanks is reduced from 16.1 fF to 14.5 fF. Even the size of the injected transistors is doubled, and the optimized layout can still effectively reduce the parasitic capacitance of the circuit. Fig. 3 shows the simulated locking range for the two ILFDs. At 0 dBm injection power, the conventional locking range is 54.8–65.5 GHz while the proposed ILFD is 53.8–70.8 GHz. This indicates that the proposed ILFD increases the locking range.

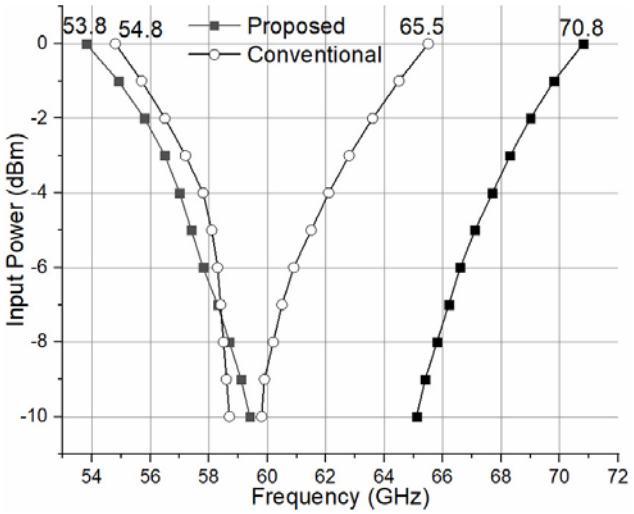

Figure 3. Simulated operation frequency against input power.

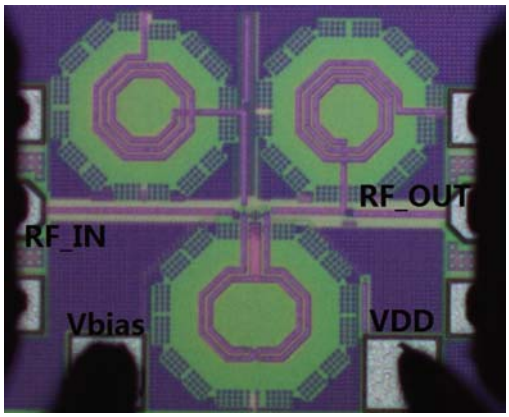

Figure 4. Chip micrograph of the 55.3 to 67 GHz ILFD.

3. EXPERIMENTAL RESULTS

The proposed design was implemented in 65 nm CMOS process. The simulation was carried out using Cadence Spectre with all parasitic parameters extracted from EM simulation (HFSS). Fig. 4 is a die photograph of the 60 GHz ILFD. The silicon area of the test chip is about $0.55 \times 0.42\,\text{mm}^2$ containing all DC and RF pads, while the core area is just about $0.2 \times 0.2\,\text{mm}^2$.

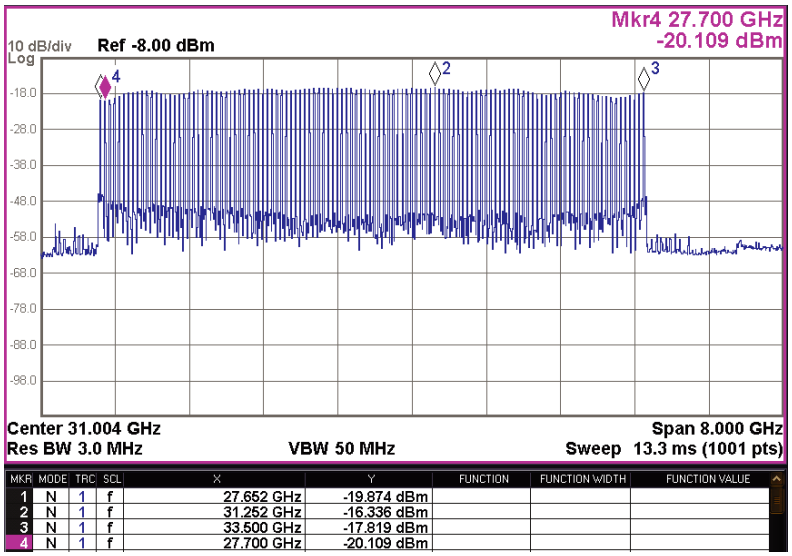

Figure 5. The spectrum of the output signal with 0 dBm input signal.

The output signal of the ILFD is measured by spectrum analyzer. Fig. 5 shows the measured locking range spectrum with 0 dBm injection signal. When the injection signal is swept from 55.3 to 67 GHz, the ILFD is locked, and a wide 19% (11.7 GHz) locking range is achieved. The output power during the whole locking range is −16 to −20 dBm without the cable and probe loss (about 5 dB). The DC power consumption of the ILFD is 3.95 mA with 0.5 V supply voltage. Table 1 summarizes the measured performances of the proposed ILFD which are compared with other ILFDs previously reported in the literatures. The most used figure of merit (FOM) of the ILFD is defined as locking range over DC power consumption. Sometimes the center frequency of the operating frequency range is included for the FOMc expression to make sure that ILFDs with different operating frequencies can be fairly compared.

Table 1. Performance summary and comparison.

	[2]	[3]	[4]	[5]	[8]	This work
Technology	0.18 µm	90 nm	0.13 µm	65 nm	65 nm	65 nm
Input frequency (GHz)	40	62.9–71.6	53–62.4	60.8–67	53.4–79.4	55.3–67
Supply (V)	1.0	0.5	0.7	0.75	0.8	0.5
Locking range (GHz)	10.6	8.7	9.4	6.2	26	11.7
Core power (mW)	6	2.75	3.93	6.3	2.9	1.98
Size (mm^2)	0.63 × 0.68	0.11 × 0.13[1]	0.57 × 0.57	0.24 × 0.24[1]	0.3 × 0.42[1]	0.55 × 0.42
FOM $(GHz/mW)^2$	1.77	3.16	2.39	0.98	8.97	5.91
FOMc[3]	70.8	212.5	137.9	62.6	595.6	361.4

[1] core area without pads.

[2] FOM = Locking Range/P_{DC}.

[3] FOMc = Center Frequency × Locking Range/P_{DC}.

4. CONCLUSION

A low-parasitic CMOS transistor structure for wide locking range ILFD is presented. It is fabricated in a 65 nm CMOS process. Measurements show the divider without using any frequency-adjustment mechanism, and a 19% (11.7 GHz) locking range from 55.3 GHz to 67 GHz is achieved. It consumes 1.98 mW at 0.5 V power supply without the output buffers.

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