Electromagnetic Hotspots Identification in Integrated Circuits

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Abstract—Advancements in functionalities and operating frequencies of integrated circuits lead to the necessity to study Electromagnetic Compatibility/Electromagnetic Emissions (EMC/EMEs) from these devices. In this work, a methodology is developed, which combines near field electromagnetic measurements and 3D layout simulation of an Integrated Circuit (IC), to identify the sources of EME from a commercial IC. This methodology can help to narrow down the area of key importance with respect to EME sources, instead of the entire IC, before it is fabricated. Consequently, IC designers can optimize their design to minimize the EME before fabrication, saving cost and time significantly.

1. INTRODUCTION

Operating frequency of High Frequency (HF) Integrated Circuits (ICs) is increasing for higher efficiency as shown in Fig. 1. This increasing operating frequency renders Electromagnetic Interference (EMI) from the ICs, making them and other neighboring circuits susceptible for the Electromagnetic Emissions (EMEs) [1, 2]. Consequently, HF ICs are to be designed according to Electromagnetic Compatibility (EMC) standards in the earlier design stages.

To ensure that EMC is successfully incorporated, electromagnetic measurement of fabricated chips is usually performed after their design. However, with the increasing complexity of circuits, such measurement can be limited, especially when the designed chip is implemented in 3D-IC, as illustrated in [3] where the authors show that the locations of high EMEs can be confusing or misleading from the measurement of 3D-IC, when the distance of the measuring probe from the surface of IC is more than 40 μm.

An effective way to handle this EMI issue is to compute the electromagnetic field distribution over the chip and identify the sources of the EME in an IC with their severity evaluation, so that necessary design revision may be made accordingly.

However, HF IC design imposes many modeling challenges to electromagnetic analysis. These challenges include conductor loss, large numbers of dielectric stacks, strong non-uniformity, substrate effect, large numbers of conductors, large aspect ratio, broadband, and 3-D complexity [4]. Every challenge increases the number of unknowns, and hence the size of the problem for computing EMI is complex.

Recently, Sangwan et al. [8] developed a 3D layout simulation approach for the study of the EMI from an IC layout prior to its fabrication. This simulation approach provides good precision in the results as compared to the measurement results. To overcome the above-mentioned computational challenges, we apply this simulation approach together with Near Field (NF) measurement to identify the EMI sources or hotspots in HF ICs in this work, and such an approach can be used for all HF ICs. The identification is obtained by narrowing down the area of importance, starting from Printed Circuit
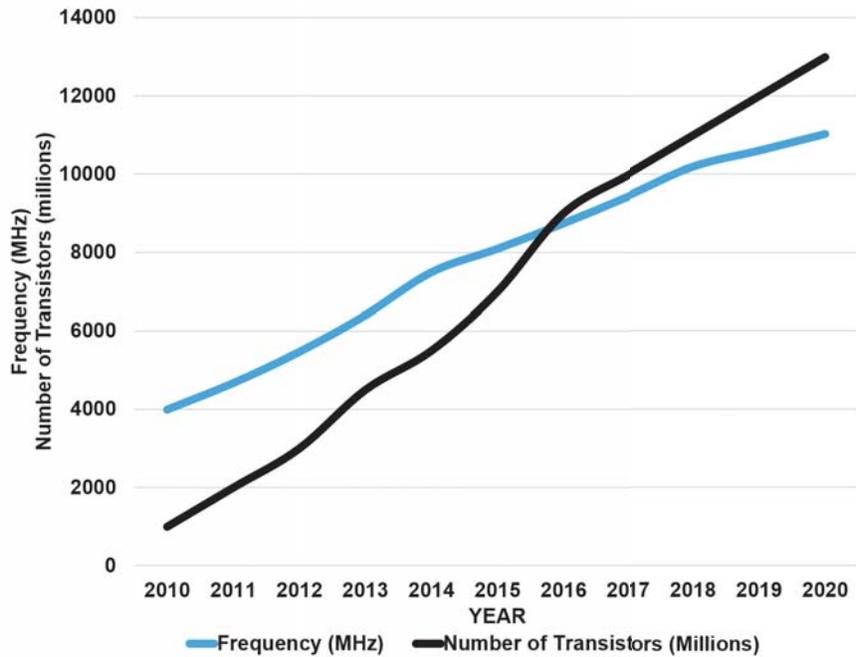
Figure 1. Trend of operating frequency and number of transistors from 2010–2020 [5–7].

Board (PCB) to inside the layout of IC. To illustrate this methodology, a commercial LED driver IC is employed.

2. DEVICE UNDER STUDY

With the increasing use of LED lighting system, LED driver ICs are becoming popular. The driver circuit converts the AC power source into constant current for LEDs, as constant current is needed to ensure display color gamut stability [9, 10] from the LEDs. There are two types of LED drivers, namely switched mode and linear mode LED drivers. The driver studied in this work is a linear mode driver.

The constant current from the driver requires Pulse Width Modulator (PWM). The high switching frequency of PWM creates EMI when a large number of LEDs are switched ON simultaneously, and this can generate a significant current spike on the power supply lines. This EMI in the power supply is difficult to remove because of its high power and broad frequency spectrum (up to 100 MHz) [11]. Several techniques are used to overcome the EMI generated by the LED systems, including converter designs [12], components design [13], EMI filter [14], and spread-spectrum techniques [15]. However, all these methods increase the overall cost of the products and size of the PCB. The LED driver circuitry under study in this work is shown in Fig. 2.

In order to identify the main sources of EMI in the LED Driver circuitry that consists of the PCB and IC, NF electromagnetic scanning is performed. The international standard used for the test is CISPR-25, which is designed to protect receivers from disturbances produced by conducted and radiated emissions arising in a vehicle.

FLS Langer 106 is used for the measurement; the Device Under Test (DUT) is operating under normal operating condition, i.e., $V_{IN} = 110$ V at 0.1 mA; and 12 LED's are series connected at the output. Chip scan software converts the voltage signals into dBμV unit from spectrum analyzer, which is connected to an H-field probe for measuring the magnetic field distribution. The spatial resolution of the measurement equipment is 100 μm.

The H-probe is used to measure the magnetic field at 200 μm above the DUT surface. This is also the minimum distance that the probe can be placed near the DUT, and it turns out to be the major distance for the near field pollution [16]. Increase in distance will make the magnetic field measurement
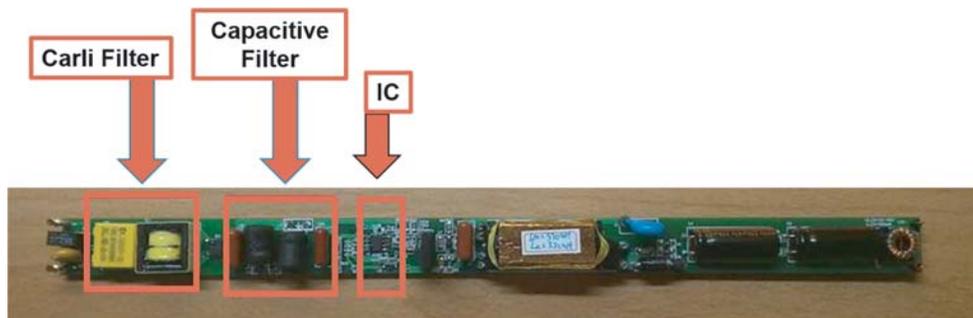
Figure 2. LED Driver PCB with EMI filters.

result more disperse, making it difficult to identify the hotspot as reported by [3].

NF scanning is done for frequency ranging from 150 MHz to 3 GHz. The NF scanning is performed on the PCB without EMI filters intentionally, in order to find the real magnitude of the emissions from the LED system. The NF scanning captures the emissions at 2851 frequency points with a step size of 1 MHz.

Measured NF emissions are found high at and around the IC. Three hotspot areas are identified from the NF scanning as shown in Fig. 4, and they are IC, CMOS discrete transistor, and capacitor area as marked in Fig. 3.

Figure 5 shows a pie chart indicating the respective percentage contributions of the three EMI sources. The percentage contribution is computed using the following equation, where the numerator is a number of discrete measurement frequency points where a particular EMI source is dominant, i.e.,
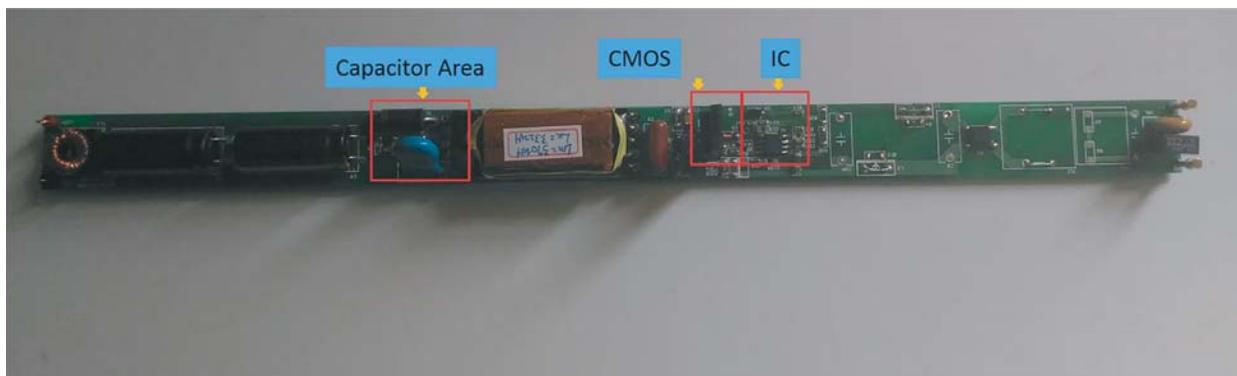

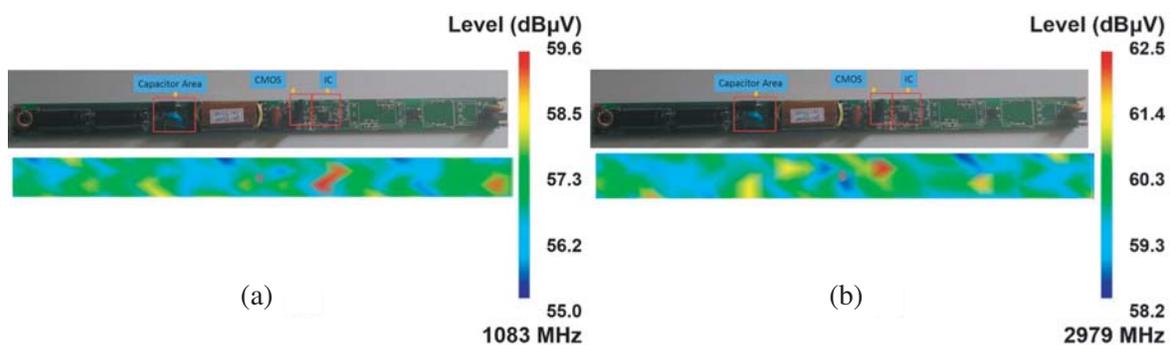**Figure 3.** Locations of respective sources of EMI in PCB.

Figure 4. Measured magnetic field distribution over PCB at (a) 1083 MHz and (b) 2979 MHz.
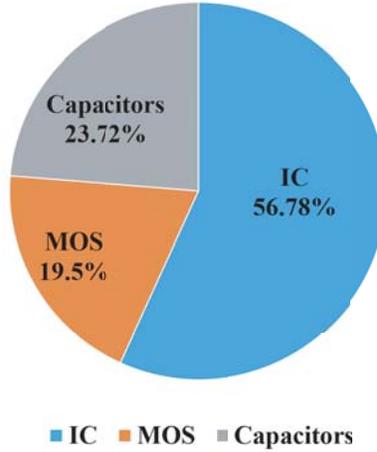
Figure 5. Percentage contribution of different components within PCB to EME.

emitting the highest electromagnetic intensity at a given frequency point.

$$Percentage\ Contribution\ of\ a\ EMI\ Source = \frac{Number\ of\ discrete\ frequency\ points\ for\ a\ source}{Total\ number\ of\ discrete\ frequency\ points\ (2851)} \tag{1}$$

For example, Table 1 shows an example of 10 discrete frequency points (among 2851 points) and the dominant EMI source at the respective frequency point with the corresponding maximum level of EME. Then the numerator in Equation 1 in this case will be 6 for IC, 2 for CMOS, and 2 for Capacitor area, while the denominator will be 10 for all. For the pie chart shown in Fig. 5, it is computed over all the 2851 frequency points.

Table 1. Listing the source of EMI and its magnitude at 10 discrete frequency points.

Frequency (MHz)	Source of EMI	Maximum level (dBμV)
97	IC	69.2
221	Capacitor area	62.7
452	IC	60.4
979	IC	59.8
1083	IC	59.6
1232	IC	59.9
1573	CMOS	58.9
1899	IC	59.1
2344	Capacitor area	60.1
2979	CMOS	62.5

From Fig. 5, it is clear that the IC is the main source of EME. To identify the EME hotspots within the LED driver IC, NF scanning is used again. NF scanning pinpoints the areas with high EME, so that one can focus on these areas in order to reduce the EME from the IC. Examination of the NF scanning floor map of the IC shown in Fig. 6 reveals that the PWM block is the main source of high emissions from the IC, as expected. LVBG and LSF also emit high electromagnetic field intensity, but their intensities are much less than PWM. LSF is a bi-directional multi-voltage level translator for Open-Drain and Push-Pull Application, and LVBG is low voltage bias generator. Fig. 7 shows the location of LVBG, PWM, and LSF with green, red, and grey color boxes, respectively.
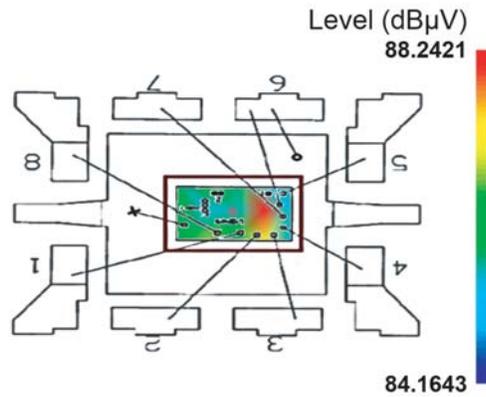
Figure 6. Measured magnetic field distribution over the LED Driver IC at 750 MHz.
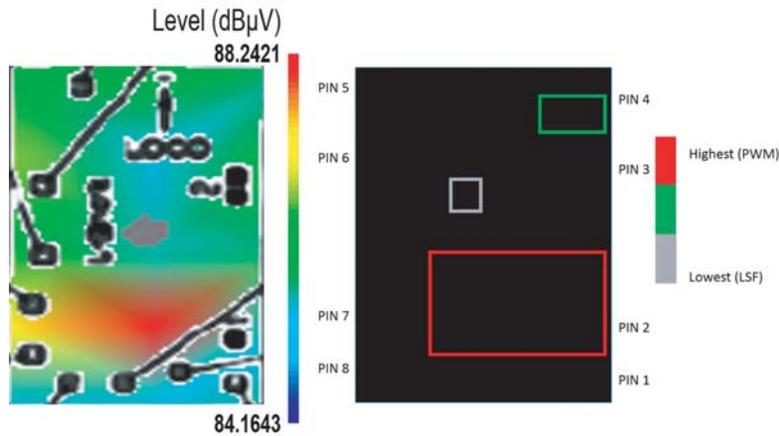

Figure 7. Pin diagram for the IC showing the block with highest and lowest near field emissions.

In order to further zoom into the IC layout to identify the EME hot spot, simulation method is needed, as the H-probe diameter, which is much larger than the area of PWM, is no longer able to perform such a task.

To perform electromagnetic field calculation, 3D layout of IC is necessary, as demonstrated by Sangwan et al. [8]. In [8], Sangwan et al. presented a method to fabricate 3D structure of IC in simulation using ANSYS from the corresponding layout GDSII files. However, due to company confidentiality, GDSII file of the circuit is not obtainable, and instead we reconstruct the DUT in 3D through the ANF file converted from the GDSII file using LinkCAD software.

With this 3D layout, we employ ANSYS High Frequency Structure Simulator (HFSS) to compute the electromagnetic field distribution over the surface of IC layout to mimic the real scenario. HFSS uses Finite Element Method (FEM) for electromagnetic computation, which is capable of performing numerical solutions of complex problems in solid materials and different structures [17].

3. EME SIMULATION RESULTS OF PWM

Figure 8 shows the simulation results of PWM. There are 44 lumped ports in the PWM circuit. As we increase the number of lumped ports from 1 to 44, the magnetic field strength increases as shown in Fig. 9. In particular, when ports 31–44 are added, the magnetic field increases significantly, indicating that the main sources of high EME should be due to ports 31–44, and they are named as INPUT, EN, ENClear, N1, N2, N4, N6, BACKUP, and TM.
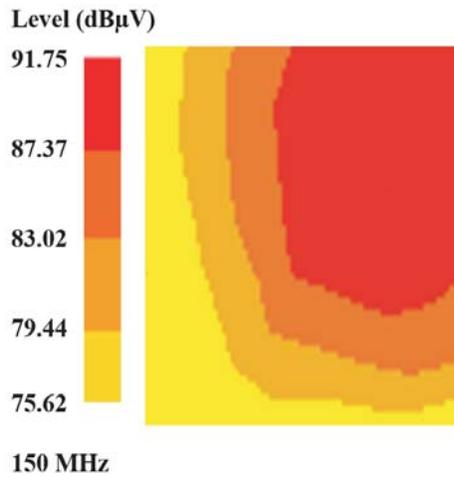
Figure 8. Simulation results at 200 μm height between the surface of the IC and the reference plane for PWM.
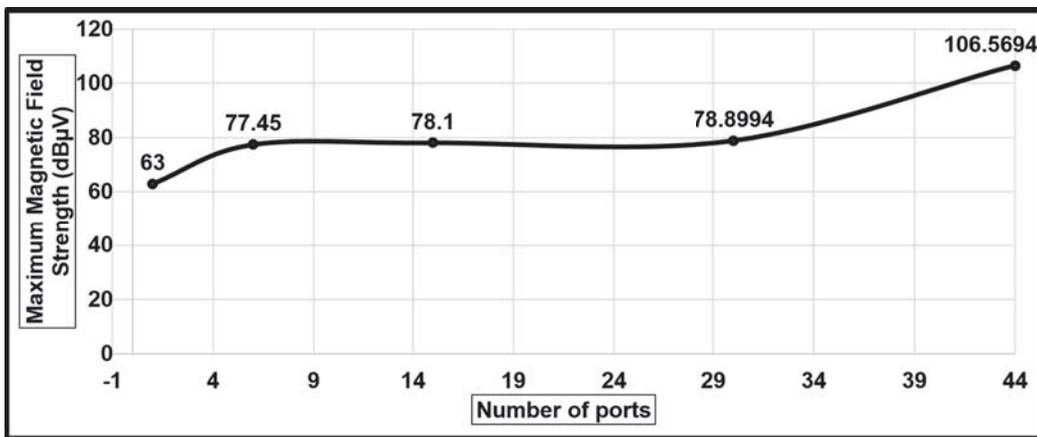

Figure 9. Maximum magnetic field distribution vs number of ports applied for excitation of PWM in HFSS.

Figure 10 shows the computed magnetic field distribution when the numbers of lumped ports are 1 and 44, respectively in the PWM layout. All these results are taken at the surface of the layout, i.e., 0 μm. One can vividly see that the location of hot spot changes for the two cases. Black box in Fig. 10 shows the location of main culprit of high EME within the PWM circuit.

With this proposed methodology, we can precisely pinpoint the areas of high electromagnetic emission hot spots from PCB to IC and down to PWM circuit within the IC. With such detailed identification, one can perform revision of the design only on the hot spot areas instead of the entire chip, reducing the cost and time of the product in the market.

As we perform our simulation on the GDSII or equivalent file, our method can also perform the hot spot identification in any IC design before it is fabricated, enabling optimization with respect to EME before tape out. To successfully implement the 3D layout simulation, mesh size must be small; RAM for computation should be adequate; and the layout file must be in either GDSII or ANF format. In this work, our mesh size is 0.1 m for PWM, and we use 256 GB RAM. More details can be found in [8].
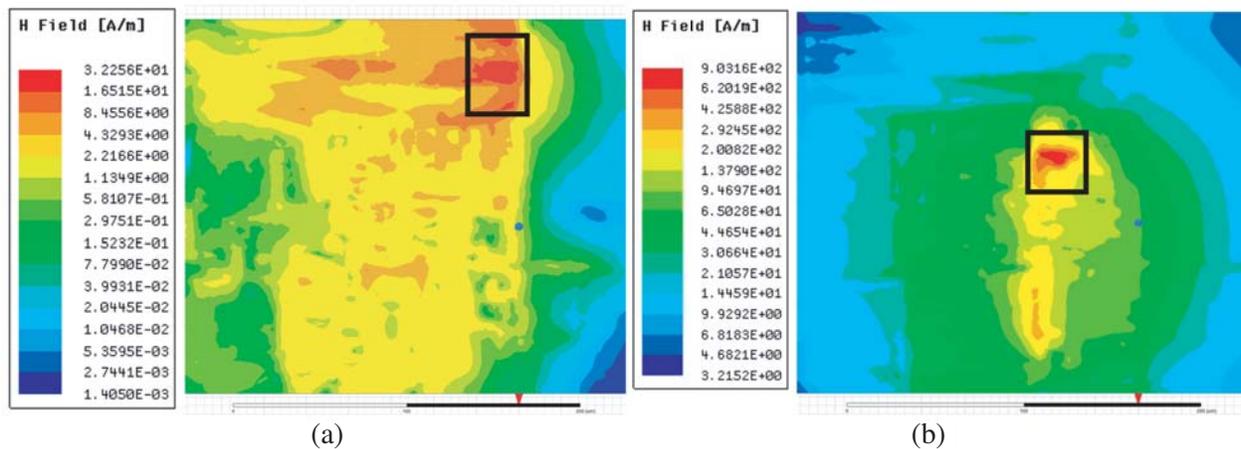
Figure 10. Magnetic field distribution as the number of applied ports are (a) 1 and (b) 44. Black box represents the area with maximum EMEs.

4. CONCLUSION

In this work, a methodology is demonstrated to identify electromagnetic emission hot spots in a commercial LED Driver circuit board down to circuit block within an IC. Near field measurement coupled with ANSYS HFSS simulation enables us to find the hot spot within an IC layout that emits high EME with high spatial resolution that cannot be achieved using the measurement equipment. This method can also be applied to any HF IC before it is fabricated. Thus, one can save significant time and cost in the design of any high frequency and high power integrated circuits while ensuring minimum EME using the method proposed in this work.

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