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A Compact Dispersive Delay Line Using Microstrip Lines and Opened Slot Lines

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Abstract—A dispersive delay line (DDL) with compact size, good group delay, and all pass response in 200–800 MHz band is presented. The proposed DDL is composed of a main microstrip transmission line with two shunted open stubs and two complementary slot lines, and a coupling slot line in ground plane. The length of the complementary slot line is reduced approximately from $\lambda_g/2$ to $\lambda_g/4$ through the upper end being opened, hence achieves miniaturization for the proposed DDL (λ_g is the guided wavelength at the center frequency). The overall area is $0.196 \times 0.093\lambda_g^2$ with a peak group delay time of 3.2 ns. The proposed DDL has the advantages of compactness, good capability, and easy fabrication without any external matching network.

1. INTRODUCTION

A dispersive delay line (DDL) can provide frequency dependent group delay. It is widely used in many areas, such as group delay equalization, novel phase array elements, compressive receiver, and analog signal processing [1–9]. At present, a key research challenge for DDL is to achieve high delay from a compact structure with an acceptable insertion loss (IL). In [10], a DDL using microstrip line technology that contains shunt open-stub overlapping a shorted slot line is presented. The DDL has all-pass magnitude response over ultra-wideband frequency range and provides a smooth and continuous group delay profile. In [11], the DDL theories of microstrip line technology are further developed, and analytical expressions that contain the transmission coefficient ($|S_{21}|$) and group delay (GD) are derived. In [12], two deformed open stubs and their complementary slot lines are used to obtain a DDL with all-pass magnitude respond and good group delay. Although there are some distinguished advantages in [10–12] for the DDL using microstrip line technology, the miniaturization of the DDL is crucial to the practical application, especially for operating in the low frequency band. However, both the open stubs and their complementary short slot lines in [10–12] are about a half guide wavelength ($\lambda_g/2$) and located on both sides of the main transmission line symmetrically, which occupy a relative large space accordingly.

In this letter, we propose a novel compact DDL design that can locate the open stubs and their complementary slot lines on the same side of the main transmission line. The proposed complementary slot line has the length about $\lambda_g/4$, rather than about $\lambda_g/2$ in [10–12]. Moreover, an additional coupling slot line is embedded transversely in ground plane for fine-tuning the impedance matching.

2. DESIGN OF THE DDL

The configuration of the proposed DDL is shown in Fig. 1. The DDL is built on an IT-8350G substrate with relative permittivity of 3.5, loss tangent of 0.0025, and thickness of 0.5 mm, respectively. Two

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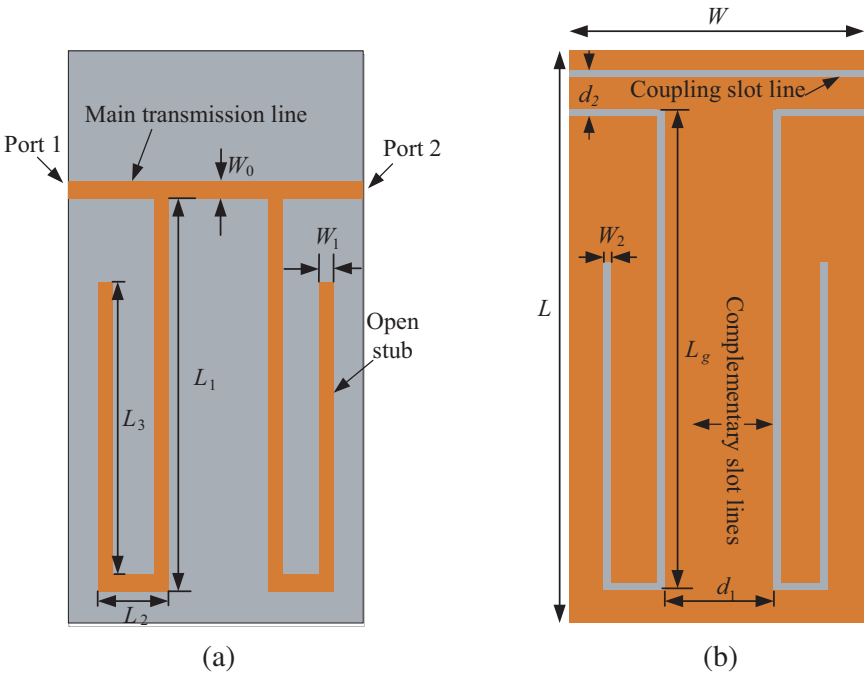


Figure 1. Geometry of the proposed DDL, (a) top view, (b) bottom view.

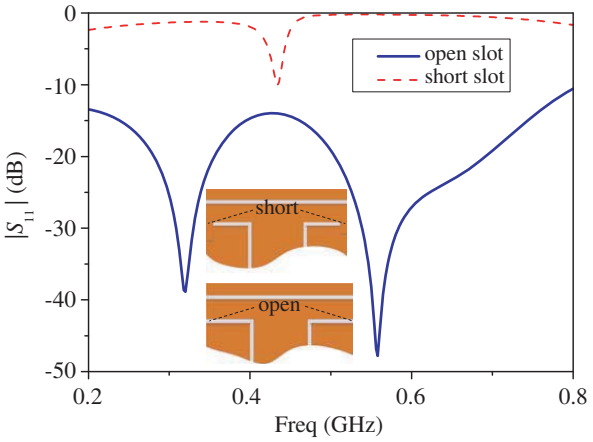


Figure 2. Simulated $|S_{11}|$ for the open slot and short slot of the upper end.

shunted open stubs with each length about $\lambda_g/4$ are located on the same side of the main transmission line, where open stubs are folded back for saving space, as shown in Fig. 1(a). Three slot lines with the same width of W_2 are etched in ground plane, where two slot lines of them act as the complementary slot lines, and the third slot line acts as the coupling line, as shown in Fig. 1(b).

The two complementary slot lines whose upper end is opened, and the lower end shorted can cancel the effects of the open stubs on the main transmission line when the length of the open stub is around $\lambda_g/4$. Therefore, the proposed wideband DDL can be achieved. The third slot line is a coupling line for fine-tuning the S-parameters through adjusting the distance between the coupling line and the complementary slot lines. Compared with the conventional DDL with microstrip line technology, the length of the complementary slot line of the proposed DDL is only about $\lambda_g/4$, rather than around $\lambda_g/2$ in [10–12]. The reason for the length reduction can be explained as that the upper end is opened and the lower end shorted for the proposed complementary slot line, while both ends are shorted for the conventional complementary slot lines. To illustrate the effects on the port reflection coefficient of

$|S_{11}|$ for the proposed DDL, Fig. 2 gives the simulated curves when the upper end is shorted or opened, computed by Ansys HFSS 18.0. It can be observed that the $|S_{11}|$ are deteriorated remarkably when the upper end of the complementary slot line is shorted, as shown in Fig. 2.

The performance of the proposed DDL is simulated, and the optimized design parameters are as follows (mm): $L = 63$, $W = 30$, $L_1 = 47.3$, $L_2 = 7$, $L_3 = 36$, $W_0 = 1.9$, $W_1 = 2$, $W_2 = 0.7$, $L_g = 55$, $d_1 = 14$, $d_2 = 3.5$ mm.

3. PARAMETRIC STUDIES

Parametric studies are performed by simulating the DDL parameters of $|S_{11}|$, $|S_{21}|$, and group delay. Only one geometrical parameter is varied each time, and the rest parameters are kept unchanged at a time in the following investigations.

The effects of the width of the open stub, W_1, on $|S_{11}|$, $|S_{21}|$, and group delay of the proposed DDL are shown in Figs. 3(a)–(c). When W_1 varies from 1 mm to 3 mm with a step width of 1 mm, both $|S_{11}|$ and $|S_{21}|$ first become better and then worse, while the proposed DDL shows the maximum group delay time at the center frequency of 500 MHz when $w_1 = 1$ mm. The reason can be explained as that the mutual coupling between the open stubs and the complementary slot lines is changed with the variation of W_1.

Figure 4 shows the effects of various widths of the main microstrip transmission line, w_0, on $|S_{11}|$, $|S_{21}|$, and group delay. When w_0 varies from 0.9 mm to 2.9 mm with a step width, $|S_{11}|$, $|S_{21}|$, and group delay have obvious variations. The reason is that the variation of width changes the characteristic impedance of the main microstrip transmission line.

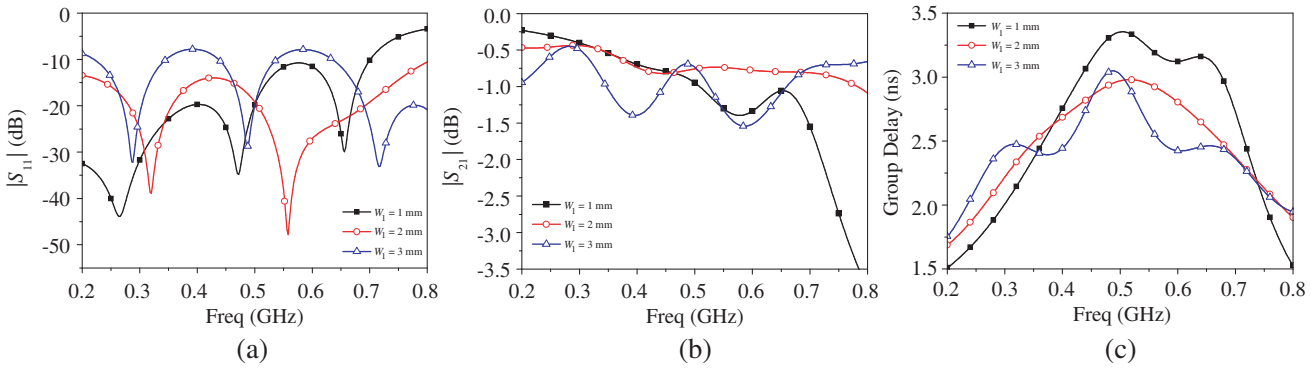


Figure 3. Simulated $|S_{11}|$, $|S_{21}|$ and group delay with the variation of W_1. (a) $|S_{11}|$, (b) $|S_{21}|$ and (c) group delay.

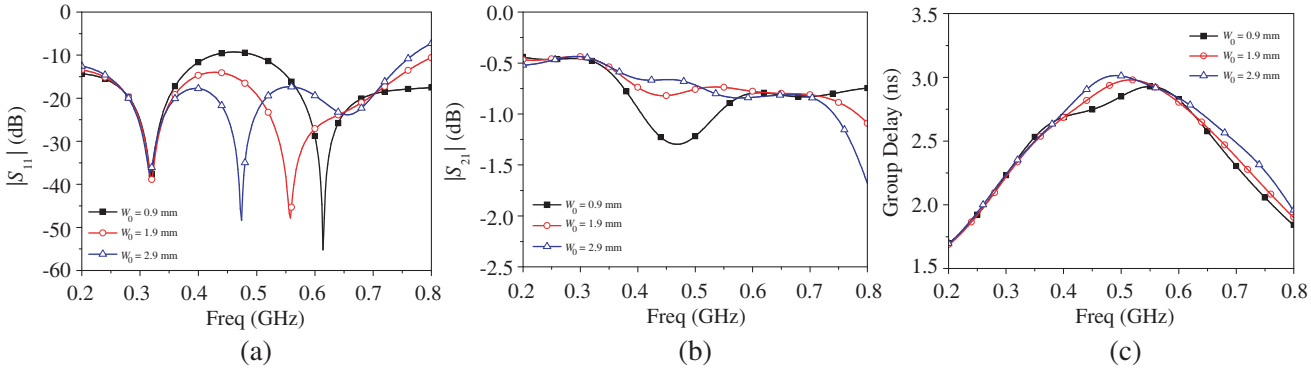
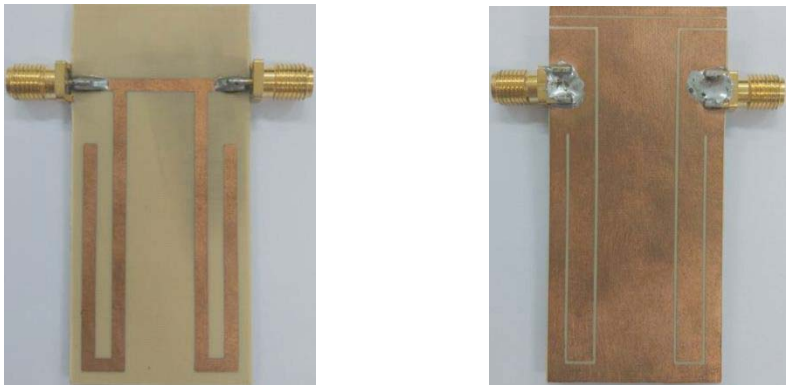


Figure 4. Simulated $|S_{11}|$, $|S_{21}|$ and group delay with the variation of W_0. (a) $|S_{11}|$, (b) $|S_{21}|$ and (c) group delay.

4. RESULTS AND DISCUSSION

To verify the performance of the proposed DDL, the prototype with optimized parameters is fabricated and shown in Fig. 5. The group delay is measured using the vector network analyzer of R&S ZNB20, and the simulated and measured curves are depicted in Fig. 6. It can be observed that the measured results show good corroborations with the simulated ones. The measured peak delay time is 3.2 ns at the frequency of 534 MHz.



(a) (b)

Figure 5. Photograph of the proposed DDL, (a) top view, (b) bottom view.

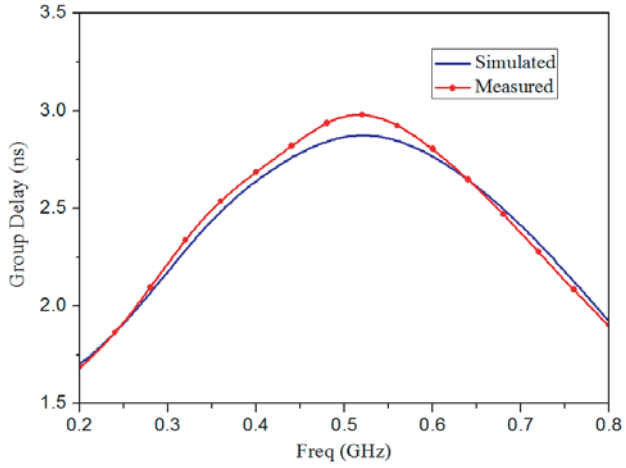


Figure 6. Simulated and measured group delay of the proposed DDL.

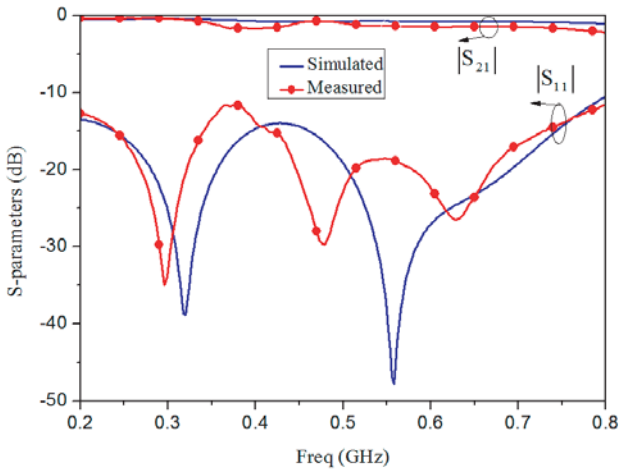


Figure 7. Simulated and measured S parameters of the proposed DDL.

The S-parameters of the prototype are measured, and Fig. 7 gives the measured and simulated S-parameters of the proposed DDL. It can be observed that the measured results agree well with the simulated ones. The $|S_{11}|$ are less than -10 dB in the 200–800 MHz band, and its lowest value can reach -35 dB. The $|S_{21}|$ are close to 0 dB, and the measured maximum insertion loss is 1.68 dB at the frequency of 385 MHz over the frequency band 200–800 MHz. The insertion loss is 0.76 dB at the center frequency of 534 MHz, which corresponds to the maximum delay time. The insertion losses are mainly due to transmission losses and slot radiation losses. The discrepancies between the simulated and measured plots may be attributed to unavoidable errors in the fabrication and measurement. This proposed DDL can also be viewed as a wideband bandpass filter, because it exhibits an all-pass response across the frequency band 200–800 MHz, and meanwhile, a desired group delay can be obtained.

Table 1 shows the comparisons of the prototype dimensions and performance between the proposed DDL and other recently published works. It can be summarized that the proposed DDL has the smallest electric size without compromising the performance, which is only 6.2%, 10.3%, and 11.6% in area compared with the ones in [10, 11] and [12], respectively.

Table 1. Comparison of the DDL electrical size and performance between this and other recently published works.

Ref.	f_0 (GHz)	IL @ f_0 (dB)	Delay	Area ($\lambda_g * \lambda_g$) @ f_0
10	2.5	–	0.52 ns	$0.766 * 0.383$
11	1	1.9	2.0 ns	$0.942 * 0.188$
12	2.5	0.9	0.8 ns	$0.549 * 0.286$
This paper	0.5	0.76	3.2 ns	$0.196 * 0.093$

5. CONCLUSION

A compact DDL with microstrip line technology has been obtained in this letter. The required length of the complementary slot line in the proposed DDL is reduced approximately from $\lambda_g/2$ to $\lambda_g/4$ and hence significantly decreases its required area. According to the measurement results, the insertion loss, group delay, and element area have obvious advantages compared with the existing DDL, which has promising application in phase array elements and signal processing.

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