Progress In Electromagnetics Research Letters, Vol. 86, 53–58, 2019

Differential Far-End Crosstalk Mitigation with Polarity Reversal

Xiaofeng Song[1, 2] and Deheng Li[2, *]

Abstract—In order to reduce far-end crosstalk between two differential line pairs of microstrip, this paper proposes a method of reducing far end crosstalk by polarity inversion. In this way, the signal line is placed in the middle of PAD of one capacitor to achieve polarity reversal at the AC coupling capacitor of the differential line. The simulation results show that, in this way, the far end crosstalk can be reduced by 63.6%, and this method of far end crosstalk suppression has an effect on both pairs of differential lines.

1. INTRODUCTION

With the gradual increase of high-speed signal rate, the technology on signal integrity has been gradually developed into a research focus in the field of high-speed circuit design. Research on signal integrity mainly includes impedance matching, reflection, crosstalk, loss, etc. [1], and among them, the most common one is the study of impedance matching and impedance continuity improvement [2]. In recent years, as the frequency of signals has increased, crosstalk problem cannot be ignored.

Crosstalk can cause timing and signal integrity issue, and can interfere with other high speed signal lines [3]. At present, the research on crosstalk mainly focuses on establishing and simulating the crosstalk model [4], reducing crosstalk by design optimization from layout [5–8], adding protection band to signals that may have crosstalk [9], etc. However, it is more difficult to reduce crosstalk as the PCB components become more numerous, and the wiring space becomes more limited.

Ref. [10] proposes a crosstalk suppression method for differential signals, and the polarity inversion of the differential pair can be achieved by adding two vias during signal transmission, thereby reducing far-end crosstalk. However, via holes can cause additional problems. According to [11], via holes, especially via stubs, have a substantial effect on the signal. In this case, it is necessary to fully consider the reduction of far-end crosstalk and the effect of vias on the signal. Therefore, in combination with patents [12–14], this paper proposes a new far end crosstalk suppression method that does not require the addition of vias, thereby achieving direct reduction of far-end crosstalk between two differential line pairs of microstrip by achieving polarity reversion at the AC coupling capacitors directly.

2. THEORY OF CROSSTALK MITIGATION

Crosstalk is the result of superposition of capacitive coupled noise and inductively coupled noise between signals. From [15], we can get

$$K_C = \frac{C_m}{C_0} = \frac{C_m}{C_g + C_m} \tag{1}$$

$$K_L = \frac{L_m}{L_0} \tag{2}$$

$$V_{fext} = \frac{1}{2}\frac{L_e}{v}\frac{V_a}{T_r}(K_C - K_L) \tag{3}$$

Received 30 April 2019, Accepted 26 July 2019, Scheduled 6 August 2019

* Corresponding author: Deheng Li (freezing616@163.com).

[1] Shanghai Key Laboratory of Scalable Computing and Systems, Shanghai Jiao Tong University, Shanghai 200240, China. [2] State Key Laboratory of High-end Server & Storage Technology, Inspur Electronic Information Industry Co., Ltd, Jinan 250101, China.

where K_C is the capacitive coupling coefficient, K_L the inductive coupling coefficient, V_{fext} the far-end crosstalk, K_C the capacitive coupling coefficient, K_L the inductive coupling coefficient, L_e the line length, v the signal transmission speed, T_r the signal rising time, and V_a the voltage amplitude.

Suppose that there are four signal lines, of which 1 and 2 are a pair of differential lines 1; 3 and 4 are a pair of differential lines 2; the difference line 1 is aggressor; and the differential line 2 is victim. Capacitive coupling is shown in Fig. 1, and inductive coupling is shown in Fig. 2.

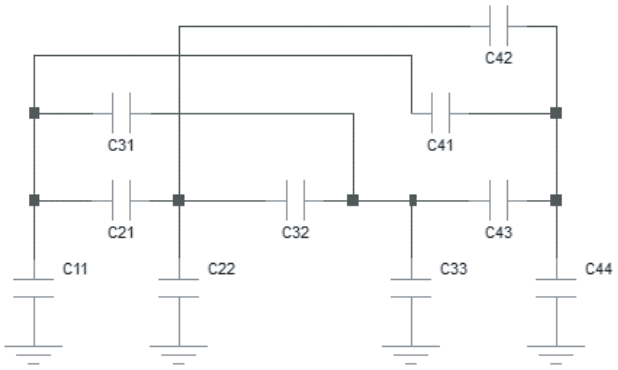

Figure 1. Capacitive coupling diagram of differential line.

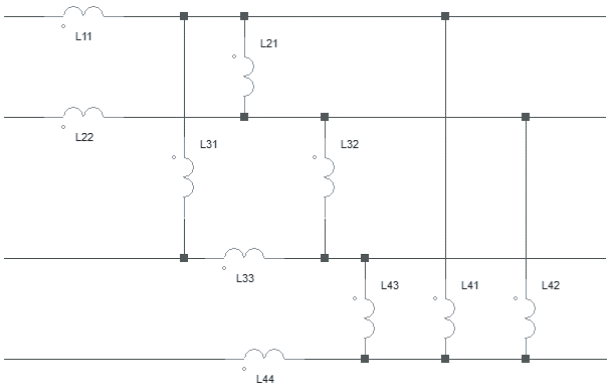

Figure 2. Inductive coupling diagram of differential line.

According to Formulas (1), (2), (3), the interference of differential line 1 to differential line 2 is considered to be the crosstalk between individual lines, and the far-end crosstalks (FEXTs) of signal lines 1 and 2 received by signal line 3 are

$$V_{f13} = \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C31}{C33+C31} - \frac{L31}{L33}\right) \tag{4}$$

$$V_{f23} = \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C32}{C33+C32} - \frac{L32}{L33}\right) \tag{5}$$

The FEXTs of signal lines 1 and 2 received by the signal line 4 are

$$V_{f14} = \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C41}{C44+C41} - \frac{L41}{L44}\right) \tag{6}$$

$$V_{f24} = \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C42}{C44+C42} - \frac{L42}{L44}\right) \tag{7}$$

The total FEXT received by the differential line 2 is

$$\begin{aligned} V_f &= V_{f3} - V_{f4} = (V_{f13} + V_{f23}) - (V_{f14} + V_{f24}) = \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C31}{C33+C31} - \frac{L31}{L33}\right) \\ &+ \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C32}{C33+C32} - \frac{L32}{L33}\right) - \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C41}{C44+C41} - \frac{L41}{L44}\right) - \frac{1}{2}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C42}{C44+C42} - \frac{L42}{L44}\right) \end{aligned} \tag{8}$$

The FEXT received by differential line 2 is shown in Fig. 3, and the final FEXT is positive.

If the positions of 4 and 3 are exchanged at the intermediate position of the differential transmission line, the signal corresponding to 4 is represented as 3′, and the signal corresponding to 3 is represented as 4′, as shown in Fig. 4. Ideally, the effect of 1 to 3 is the same as the effect of 1 to 3′ (assuming that the lengths of the transmission line are equal before and after the polarity reversal), and the effect of 1 to 4 is the same as the effect 1 to 4′, which means:

$$C31 = C3'1 \;\; C41 = C4'1 \;\; L31 = L3'1 \;\; L41 = L4'1 \tag{9}$$

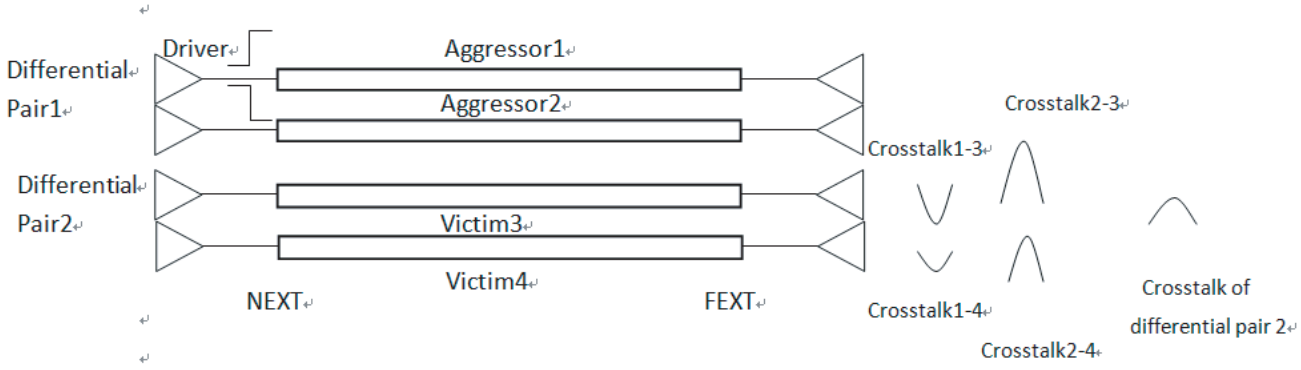

Figure 3. The FEXT diagram between differential line pairs.

Figure 4. The diagram of polarity reversal.

For the same reason:

$$C32 = C3'2 \;\; C42 = C4'2 \;\; L32 = L3'2 \;\; L42 = L4'2 \tag{10}$$

From Fig. 4, we can know that the FEXT received by the differential line 2 before polarity reversal is

$$\begin{aligned} V_{fext2} \;=\; V_{f3} - V_{f4} = {} & \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C31}{C33+C31} - \frac{L31}{L33}\right) + \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C32}{C33+C32} - \frac{L32}{L33}\right) \\ & -\frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C41}{C44+C41} - \frac{L41}{L44}\right) - \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C42}{C44+C42} - \frac{L42}{L44}\right) \end{aligned} \tag{11}$$

The FEXT received by the differential line 2 after polarity reversal is

$$\begin{aligned} V_{fext2'} \;=\; V_{f4'} - V_{f3'} = {} & \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C4'1}{C4'4'+C4'1} - \frac{L4'1}{L4'4'}\right) + \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C4'2}{C4'4'+C4'2} - \frac{L4'2}{L4'4'}\right) \\ & -\frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C3'1}{C3'3'+C3'1} - \frac{L3'1}{L3'3'}\right) - \frac{1}{4}\frac{L_e}{V}\frac{V_a}{T_r}\left(\frac{C3'2}{C3'3'+C3'2} - \frac{L3'2}{L3'3'}\right) \end{aligned} \tag{12}$$

Using Equations (9), (10), (11) and (12) together, we can get

$$V_{fext} = V_{fext2} - V_{fext2'} = 0 \tag{13}$$

So ideally, through polarity reversal, the FEXT of differential line 2 is zero.

3. DIFFERENTIAL LINE FEXT SUPPRESSION

According to Section 2, the initial design shown in Fig. 5 and the polarity reversal design of AC coupling capacitor shown in Fig. 6 are designed, and the AC capacitor is placed in the middle of the transmission line, 1.1 inches on the left and 1.1 inches on the right. The upper side is aggressor differential line, and the lower side is victim differential line. The line width is 5 mils, and the line spacing is 7.5 mils. The distance from the differential line to the reference plane is 2.7 mils, and the distance between the differential pairs is 8.1 mil. The left side is the transmitting end of the transmission line, and the right side is the receiving end.

Based on PCIE 3.0, referring to Fig. 3, in the differential pair 1's positive port of driver interface, a pulse with magnitude of 0.5 V and rising edge of 35 ps is injected, and in the negative port, a pulse with magnitude of −0.5 V and falling edge of 35 ps is injected. The receiver end of the aggressor differential pair 1 and the 4 ports of the victim differential pair 2 are respectively terminated with a 45 ohm resistor that is matched with the

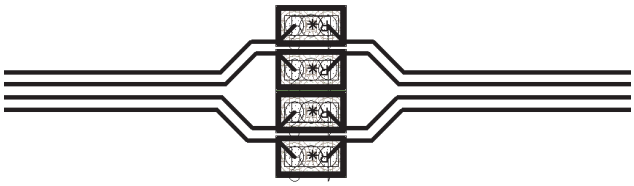

Figure 5. Initial design.

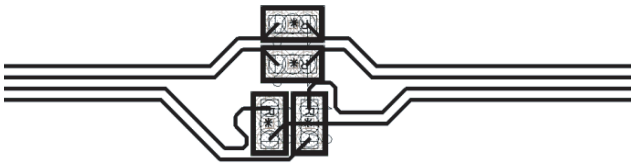

Figure 6. The polarity reversal design at the AC coupling capacitor.

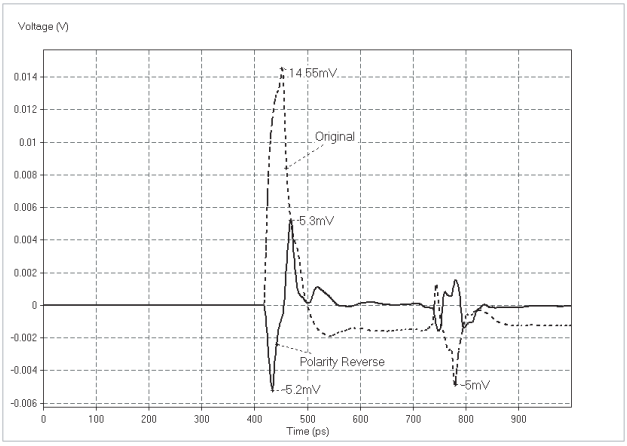

Figure 7. The comparison of initial design and polarity reversal design.

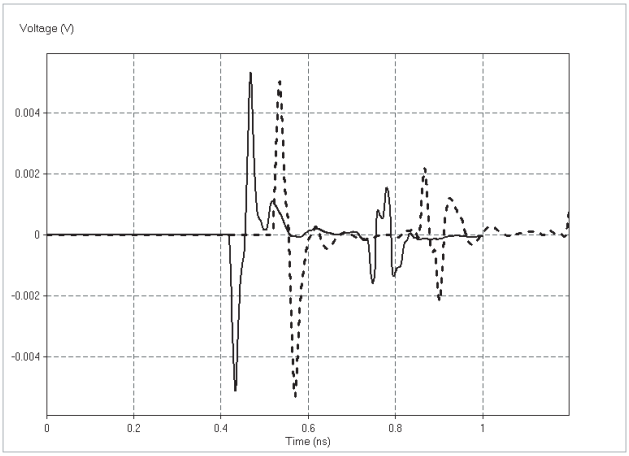

Figure 8. FEXT waveform after the position exchange of aggressor and victim.

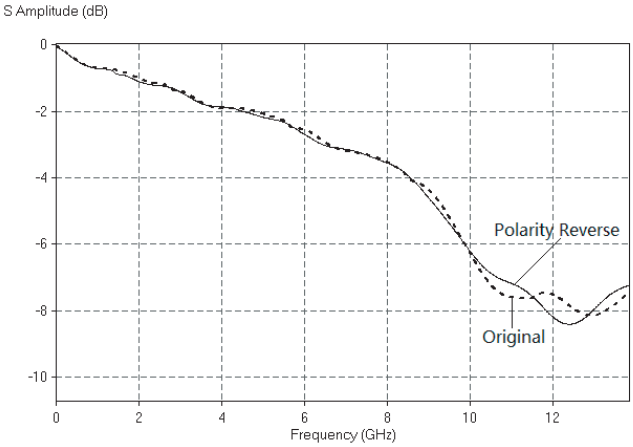

Figure 9. Insertion loss comparison.

transmission line impedance, and the 220 nF ac coupling capacitor is modeled as SPICE model. Based on the above conditions, the initial design and the polarity reversal design of the AC coupling capacitor are simulated and analyzed by Sigrity software. The FEXT waveform result is shown in Fig. 7. The dashed line is the waveform of the initial design, and the solid line is the waveform after polarity inversion design. It can be seen that after polarity reversal of the AC coupling capacitor, the positive amplitude of FEXT is reduced from 14.55 mV to 5.3 mV, in which the reduction is 63.6%, and the negative amplitude is basically unchanged.

After exchanging the above aggressor and the victim, the FEXT of victim line is also simulated. The simulation results are shown in Fig. 8. It can be seen that the FEXTs of these two are basically the same.

Table 1. The comparison of proposed crosstalk cancelation methods and existing methods.

Item	Cost	Effectivity	Difficulty	PCB area required	Availability limits
Existing Methods	●●○○○	●●●○○	●●●○○	●●○○○	●●●●○
Proposed Method	●●●●●	●●●●○	●●●●○	●●●●●	●●○○○

Therefore, the method for suppressing FEXT is applied to the differential line of the polarity inversion of the AC coupling capacitor and the differential line of non-polarity inversion.

Insertion loss is one of the key indicators for evaluating the quality of transmission link in parallel. In order to verify the feasibility of this polarity reversal design approach. We simulate and analyze the insertion loss of the initial design and polarity reversal design, and the simulation results are shown in Fig. 9. It can be seen that the loss only slightly fluctuates around 12 GHz. For PCIE 3.0 signal whose fundamental frequency is 4 GHz, the impact is small, thus verifying the feasibility of this design method. Based on "Ignore crosstalk", eye diagram is also simulated and analyzed. The result shows that there is no jitter and eye width impact with the polarity reverse, and the eye height will reduce 5 mV, considering that the polarity reverse design will reduce crosstalk about 9.25 mV, so the polarity reverse design is better than initial design.

To illustrate the practicability of this method, a comparison with existing methods is also proposed as shown in Table 1. More solid circles mean lower cost, more effectivity, less difficulty, less PCB area required, and less availability limits. It can be seen that the proposed method has advantage in four items except on availability limits. This is because the study is based on microstrip line now, and implementation on an inner layer will be our next step of the research.

4. CONCLUSION

As the signal rate increases, it is more important to reduce the effects of high speed signal crosstalk. This paper proposes a method to suppress far-end crosstalk by inverting the high-speed signal polarity on an AC coupling capacitor. The simulation model is established, and the FEXT suppression theory is simulated and verified. The results show that it is better to place the AC coupling capacitor and polarity reversal coupling capacitor of the differential pairs in the middle of the transmission line, which can reduce the voltage amplitude of FEXT to 63.6%. Exchanging the aggressor and the victim differential pair is also analyzed, and it verifies that the FEXT reduction is suitable for both of the differential pairs.

REFERENCES

1. Shao, J. and Z. Jie, "Design of a high density connector for high-speed backplane," *Chinese Journal of Electron Devices*, Vol. 39, No. 2, 291–297, Apr. 2016.
2. Huang, B., X.-B. Li, Z. Zeng, et al., "Study on signal integrity analysis method for electrical connector," *Instrument Technique and Sensor*, No. 5, 95–99, May 2017.
3. Wang, Y., Y. Zhao, and X. Li, "Crosstalk suppression by applying multilevel transmission," *Progress In Electromagnetics Research Letters*, Vol. 81, 45–50, 2019.
4. Mudavath, R. and B. R. Naik, "Estimation of far end crosstalk and near end crosstalk noise with mutually coupled RLC interconnect models," *2018 International Conference on Communication and Signal Processing (ICCSP)*, 182–185, Chennai, 2018.
5. Chhay, S. K., R. K. Kunze, and Y. Chu, "Crosstalk mitigation in dense microstrip wiring using stubby lines," *2013 IEEE 22nd Conference on Electrical Performance of Electronic Packaging and Systems*, 231–234, San Jose, CA, 2013.
6. Ye, X., K. Xiao, and R. Enriquez, "Differential far-end crosstalk cancellation — Implementations and challenges," *2012 IEEE International Symposium on Electromagnetic Compatibility*, 193–198, Pittsburgh, PA, 2012.
7. Enriquez, R., K. Xiao, B. Lee, and M. Tlaxcalteco, "Differential symmetry principle for differential

crosstalk cancellation," *2013 IEEE International Symposium on Electromagnetic Compatibility*, 730–734, Denver, CO, 2013.

8. Wang, Y. and X. Li, "Crosstalk cancellation method based on unitary transformation of coupled transmission lines-channel transmission matrix," *Progress In Electromagnetics Research Letters*, Vol. 52, 45–50, 2015.
9. Tani, L. and N. E. Ouazzani, "Minimizing crosstalk on printed circuit board using non uniform guard traces," *2016 International Conference on Information Technology for Organizations Development (IT4OD)*, 1–4, Fez, 2016.
10. Lee, B., et al., "Design optimization for minimal crosstalk in differential interconnect," *Proceeding of the DesignCon*, 1263–1292, 2012.
11. Fan, J., A. Hardock, R. Rimolo-Donadio, S. Müller, Y. H. Kwark, and C. Schuster, "Signal integrity: Efficient, physics-based via modeling: Return path, impedance, and stub effect control," *IEEE Electromagnetic Compatibility Magazine*, Vol. 3, No. 1, 76–84, 1st Quarter, 2014.
12. Wu, N. and F. K. Wu, "A design method for reducing the influence of crosstalk between high speed differential pairs," C.N. Patent 104182576, May 3, 2017.
13. Ye, X. N., "Differential signal crosstalk reduction," U.S. Patent 8624687, 2014.
14. Ye, X. N., "Signal routing with reduced crosstalk," U.S. Patent 9893761, 2018.
15. Bogatin, E., *Signal and Power Integrity — Simplified*, Prentice Hall PTR, 2010.