A CMOS Power Amplifier Using an Asymmetrical Input Transformer to Enhance the Gain for IEEE 802.11n WLAN Applications

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Abstract—In this study, we propose an asymmetrical input transformer for the input baluns in a differential RF CMOS power amplifier to minimize the loss induced by the input transformer. To reduce the loss caused by the magnetic coupling between the primary and secondary parts of a typical transformer, we modify the interconnection between the input transformer and the differential input of the driver stage. Unlike a typical transformer, the primary and secondary parts of the proposed transformer are directly connected to the input of the driver stage. As a result, the input signal in the primary part can reach one of the inputs of the differential driver stage, thereby reducing the loss caused by magnetic coupling. To verify the functionality of the proposed asymmetrical input transformer, we designed a 4.5-GHz differential CMOS power amplifier for IEEE 802.11n WLAN applications with 64-QAM, 9.6 dB PAPR, and a bandwidth of 20 MHz. The designed power amplifier is fabricated using the 180-nm SOI RF CMOS process. The measured maximum linear output power is 17.59 dBm with a gain of 29.23 dB.

1. INTRODUCTION

Recently, the internet of things (IoT) has rapidly developed in the field of wireless communications [1, 2]. Therefore, RF systems with a compact chip size and a low unit cost have received considerable attention [3–5]. However, because most power amplifiers essential in RF systems are designed using the HBT process for mobile and sensor applications, these power amplifiers cannot be integrated with other RF ICs or with analog or digital ICs. More recently, many studies related to CMOS power amplifiers have been conducted with fully integrated RF systems in an effort to reduce the unit cost of production [6–10]. Although low breakdown voltages and nonlinear characteristics of CMOS devices have been regarded as obstacles in the designs of power amplifiers using the CMOS process, many useful techniques which can be used to overcome the problems associated with CMOS power amplifiers have been introduced and published [11–16].

One of the most popular structures which can be used to overcome the problems associated with CMOS power amplifiers is differential structure, as shown in Fig. 1 [17–19]. Since differential structure provides a virtual ground in an integrated CMOS power amplifier, the gain reduction problem induced by the parasitic inductance and bond wires is easily solved. However, as shown in Fig. 1, the requirement of input and output baluns for the differential structure raises other problems that do not arise in HBT power amplifiers. For example, the loss induced by the input and output baluns degrades the overall power gain of the CMOS power amplifier. In particular, since the loss of the output balun directly degrades the overall efficiency and output power of the CMOS power amplifier, several attempts have been made to minimize the loss of the output balun. Fortunately, a proper structure for the output balun of a CMOS power amplifier was devised by Aoki et al. to solve the problems related to power
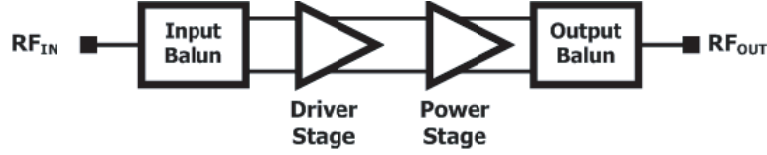
Figure 1. Simple block diagrams of a typical RF CMOS power amplifier with a differential structures.

losses in the output balun [20, 21]. On the other hand, few studies have focused on issues that affect the input balun. However, there are still several obstacles to be overcome with regard to the input balun.

In this study, we investigate the problems associated with input balun and propose an asymmetrical transformer which acts as an input balun to enhance the gain of CMOS power amplifiers.

2. TYPICAL INPUT BALUN FOR A CMOS POWER AMPLIFIER

Compared to a single-ended structure, a differential structure requires input baluns. Fig. 2(a) shows a differential driver stage and an input transformer as the input balun. In general, an input balun is composed of a transformer and MIM capacitors, as shown in Fig. 2(a). In this figure, for the sake of simplicity, MIM capacitors are omitted. If we assume that input transformer is a 1 : 1 transmission line transformer with ideal magnetic coupling (k-factor $= 1$), as shown in Fig. 2(b), the current in the secondary part, I_S, is identical to that in the primary part, I_P, while the direction of I_S is opposite to that of I_P [22, 23]. Accordingly, with single-ended input power, the ideal differential signal is generated in the input of the driver stage. However, in reality, k-factor is always lower than one, thereby introducing a power loss in the input transformer. In general, the k-factor of input transformer ranges from 0.5 to 0.8 for the GHz-order frequency with the CMOS process.
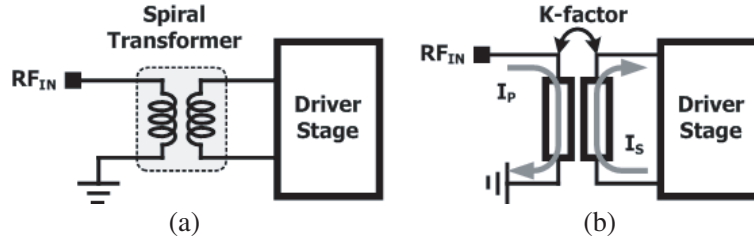

Figure 2. Simple block diagrams of input transformer and differential driver stage: (a) spiral-type transformer and (b) transmission line transformer.

Given that the loss of the input transformer does not have a direct effect on the output power or efficiency of the CMOS power amplifier, the input transformer has not received considerable attention from researchers. However, the overall gain of the CMOS power amplifier is in fact degraded more by the input balun (or transformer) than it is by the output balun. In general, given that the input impedance of the driver stage of a CMOS power amplifier is high, the input transformer should be designed as the spiral type to ensure that it has high inductance, as shown in Fig. 2(a). Accordingly, the resistive loss increases as the parasitic resistance increases in proportion to the length of the primary and secondary parts of the transformer. Additionally, due to the bulky input transformer, the loss induced by the magnetic coupling between the transformer and the lossy silicon substrate affects the gain of CMOS power amplifiers considerably.

Because the considerable loss in the input transformer necessitates an additional driver stage to compensate for the gain reduction induced by the input transformer, the overall power consumption of the CMOS power amplifier increases. Although the loss in the input transformer does not directly affect the output power or the power efficiency of the CMOS power amplifier, new efforts to minimize the loss of the input transformer related to the power gain of the CMOS power amplifier are required.

The mitigation of the losses of the input transformer has no effects on the maximum output power

of the power amplifier. However, the improvement of the gain of the CMOS power amplifier could remove the requirement of additional gain stage, thereby improving the efficiency and reducing the chip area of the power amplifier. The main aim of this work is to mitigate losses in the spiral-type input transformer and thus enhance the gain of the CMOS power amplifier.

3. PROPOSED ASYMMETRICAL INPUT TRANSFORMER AS AN INPUT BALUN

Figure 3 shows the conceptual structure of the proposed input transformer, which acts as an input balun in a CMOS power amplifier with a differential structure. Unlike the typical input transformer shown in Fig. 2(b), the primary and secondary parts of the proposed transformer are directly connected to the input of the driver stage. In this case, one of the differential inputs of the driver stage is directly connected to the primary part. The loss induced by the loose magnetic coupling is removed and thereby the power loss in I_P and V_P in Fig. 3(a) is reduced compared to the use of the typical transformer shown in Fig. 2. Although, the power loss caused by the loose magnetic coupling to induce I_S and V_S of the Fig. 3(a) exists, the overall loss in the proposed asymmetrical transformer is reduced compared to that in the typical input transformer shown in Fig. 2.
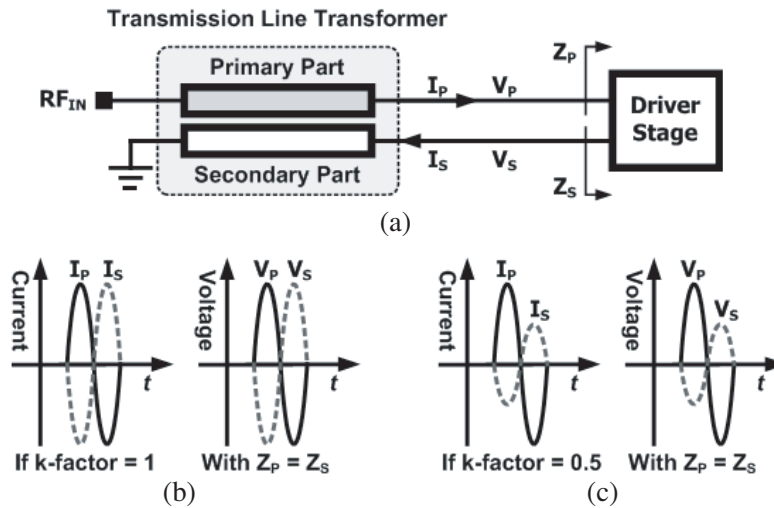

Figure 3. Proposed asymmetrical input transformer with a $1:1$ turn ratio: (a) structure, (b) current and voltage waveforms when k-factor $= 1$, and (c) current and voltage waveforms when k-factor $= 0.5$.

The operating principle of the proposed asymmetrical transformer is as follows. First, for the sake of simplicity, we assume that the k-factor is one and that the input impedances, Z_P and Z_S, of the differential inputs of the driver stage are identical to each other. With the assumption of the k-factor being equal to 1 and with a transformer structure with a $1:1$ turn ratio, as shown in Fig. 3(a), the magnitude of the current in the secondary part, I_S, should be identical to that of I_P, whereas the direction of I_S is opposite to that of I_P. Given that Z_S is identical to Z_P, the voltages of V_P and V_S exist in a differential relationship, as shown in Fig. 3(b). In an ideal case, the proposed transformer with a turn ratio of $1:1$ acts as an input balun to convert single-ended signals into differential signals, as shown in Fig. 3(b).

However, in reality, k-factor is always less than one. If the k-factor is degraded to 0.5, the magnitude of I_S becomes lower than that of I_P, as shown in Fig. 3(c). Thus, V_S becomes lower than V_P because $Z_S = Z_P$, breaking the differential relationship between V_S and V_P.

To determine the differential relationship between V_S and V_P with the actual k-factor, we modify the turn ratio of the proposed asymmetrical input transformer. In this case, we investigate the proposed transformer with a turn ratio of $2:1$, as shown in Fig. 4(a). Here, if the k-factor equals one, the magnitude of I_S becomes higher than that of I_P. In turn, because $Z_S = Z_P$, V_S is also higher than V_P, as shown in Fig. 4(b). With an ideal k-factor, the differential signal cannot be obtained using the
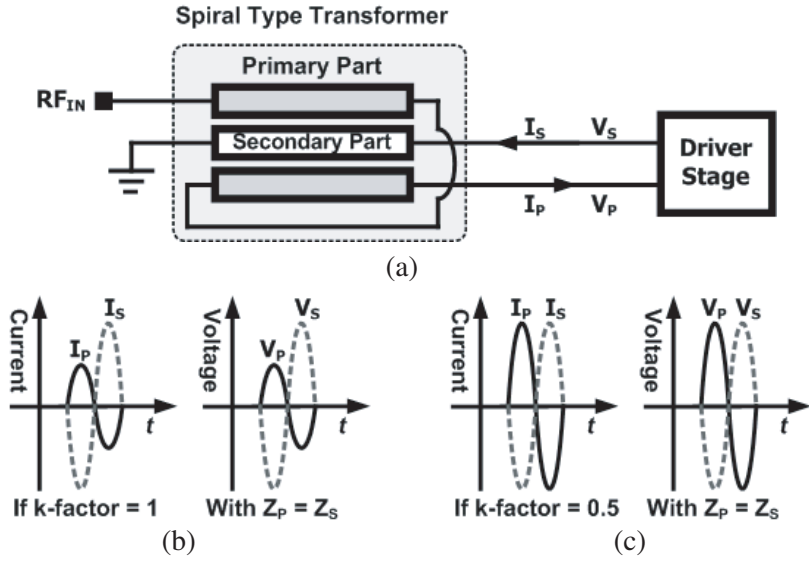
Figure 4. Proposed asymmetrical input transformer with a $2:1$ turn ratio: (a) structure, (b) current and voltage waveforms when k-factor $= 1$, and (c) current and voltage waveforms when k-factor $= 0.5$.

proposed asymmetrical transformer with a turn ratio of $2:1$. However, when the k-factor equals 0.5, the magnitude of I_S closely approximates that of I_P, as shown in Fig. 4(c). Subsequently, V_S and V_P exist in a differential relationship because $Z_S = Z_P$.

Consequently, for a given k-factor, the turn ratio of the proposed transformer can be designed to generate proper differential signals in the output of the transformer. Additionally, considering that one of the differential inputs of the driver stage is directly driven through the primary part of the transformer, the loss caused by magnetic coupling can be reduced. This improves the overall gain of the power amplifier.
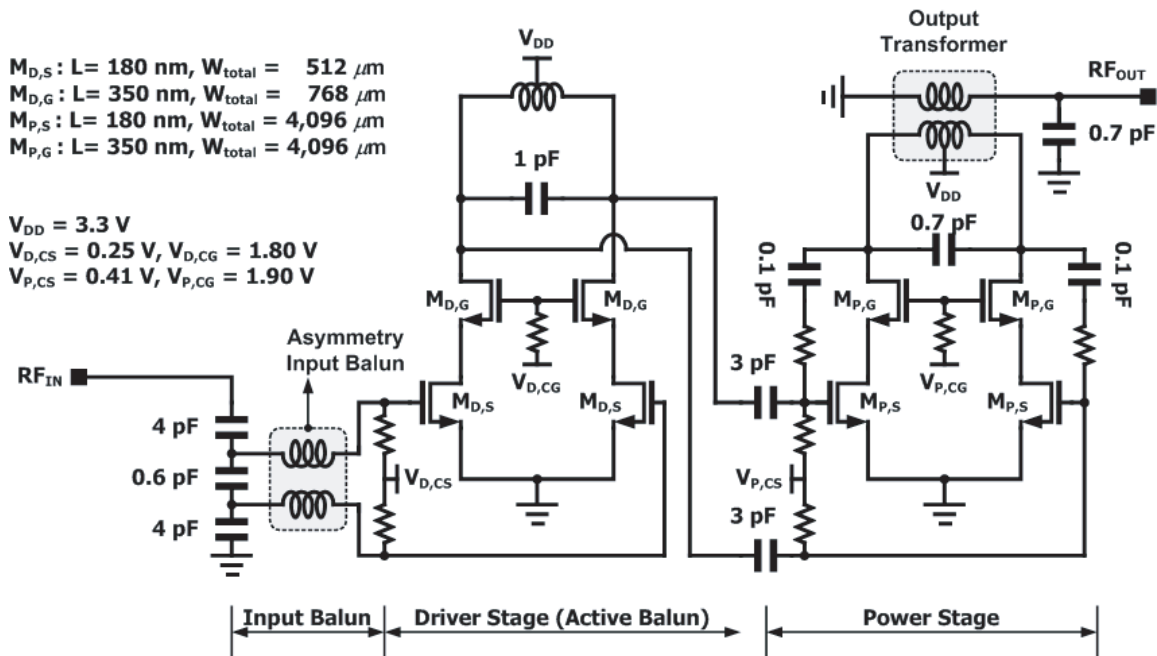

Figure 5. Schematic of the differential CMOS power amplifier using the proposed asymmetrical input transformer.

4. DESIGN OF THE CMOS POWER AMPLIFIER WITH THE PROPOSED ASYMMETRICAL INPUT TRANSFORMER

To verify the functionality of the proposed asymmetrical input transformer, we design a differential 4.5-GHz power amplifier for IEEE 802.11n WLAN applications. Fig. 5 shows a schematic of the designed CMOS power amplifier with two stages. The input matching network is completed with the proposed asymmetrical transformer and three MIM capacitors. Taking into account the k-factor of the transformer, we set the turn ratio of the transformer to $2:1$. The main role of the MIM capacitors is as a DC block for the gate bias of the driver stage. Additionally, the MIM capacitors in the input part of the power amplifier are used to match the input transformer to $50\,\Omega$ at a 4.5-GHz. The MIM capacitor of $0.6\,\mathrm{pF}$ in the input part is tuned to obtain the differential signals in the inputs of the differential driver stage.

To mitigate the reliability problem, a cascode structure is used in the driver and power stages. The output balun is designed using a typical transformer, as shown in Fig. 5. RC feedback is used in the power stage to improve the stability characteristics.
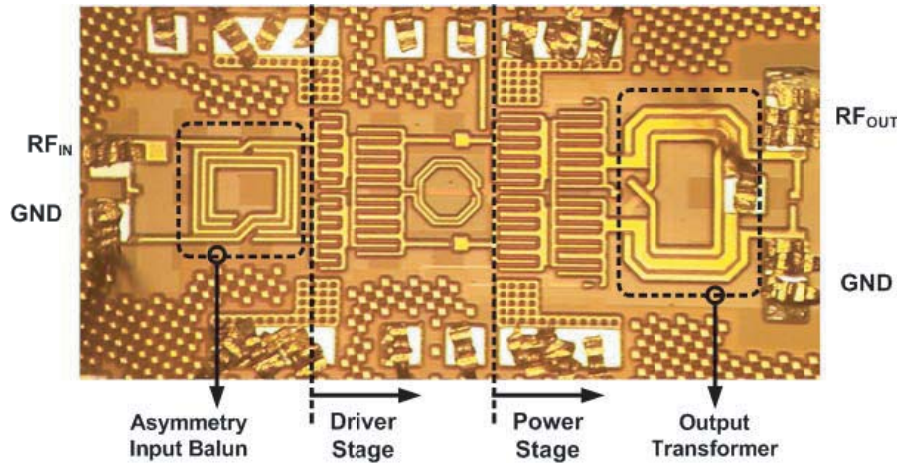

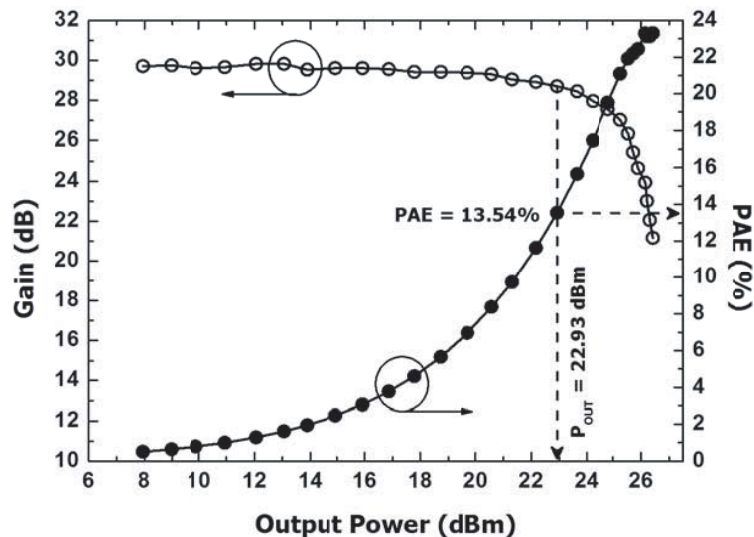**Figure 6.** Chip photograph of the designed CMOS power amplifier.

Figure 7. Measured results: gain and PAE according to the output power with the CW input signal.

5. MEASUREMENT RESULTS

Figure 6 shows a chip photograph of the designed differential CMOS power amplifier with the proposed asymmetrical input transformer. The amplifier is fabricated using the 180-nm SOI RF CMOS process, which provides four metal layers. The input and output transformers are designed using a fourth metal layer with a thickness of $4\,\mu m$ to minimize both the resistive loss and any undesired magnetic coupling to adjacent devices.

The overall chip size is $1.18 \times 0.75\,mm^2$, including the complete input and output matching network and the test pads. The supplied voltage for the driver and power stages is $3.3\,V$, making it feasible for mobile applications. The input and output load impedances are set to $50\,\Omega$. To verify the functionality of the designed power amplifier, we use a continuous-wave (CW) input signal and an IEEE 802.11n WLAN-modulated signal with 64-QAM and a bandwidth of $20\,MHz$.

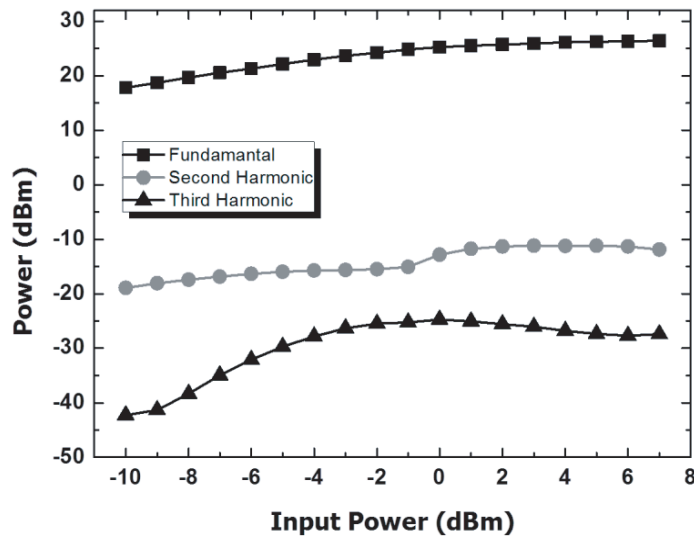Figure 7 shows the measured gain and power-added efficiency (PAE) according to the output power

Figure 8. Measured results: second and third harmonics according to the CW input signal.
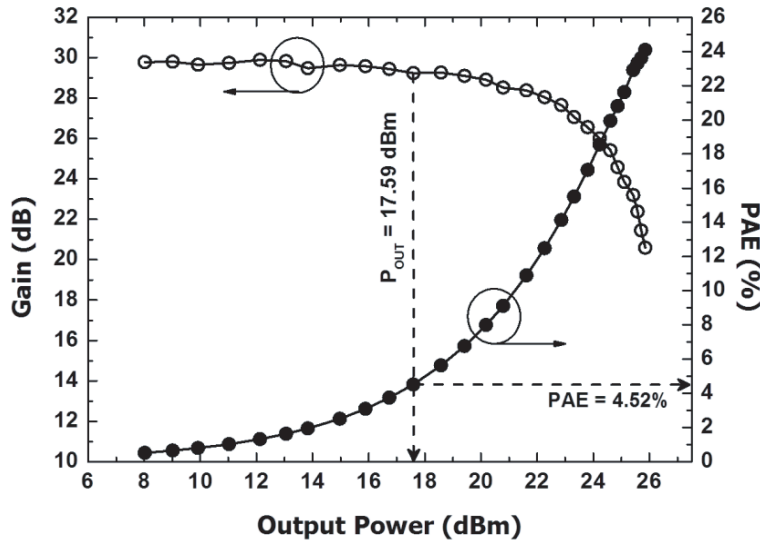

Figure 9. Measured results: gain and PAE according to the output power with a 802.11n WLAN-modulated input signal (64-QAM, 9.6 dB PAPR, 20-MHz bandwidth).

with a 4.5-GHz CW input signal. As indicated in Fig. 7, the measured P1dB is 22.93 dBm with a PAE of 13.54%. The measured gain at the P1 dB is 28.70 dB. Given that the loss in the input transformer is reduced, in spite of two-stage structure, the obtained gain is higher than that of a typical CMOS power amplifier. The measured peak output power is 26.42 dBm with a PAE of 23.30%. Fig. 8 shows the measured second and third harmonics according to the CW input signal. The measured harmonics are lower than -36 dBc in the range of input power used.

Figure 9 shows the measured gain and PAE according to the output power with the WLAN-modulated input signal (64-QAM, 9.6 dB PAPR, 20-MHz bandwidth). The measured maximum linear output power at which the WLAN specification is satisfied is 17.59 dBm with a gain of 29.23 dB. The measured peak output power with the modulated input signal is 25.85 dBm with a PAE of 24.08%.

Figure 10 shows the measured EVM. To meet the standard of an IEEE 802.11n WLAN with 64-QAM and 20-MHz bandwidth, the measured EVM should be lower than -28 dB. As shown in Fig. 10, the measured maximum output power, P_{MAX}, is 17.59 dBm. In Fig. 11, the measured signal constellation at the P_{MAX} value of 17.59 dBm is shown. Fig. 12 shows the measured frequency spectrum at P_{MAX}.
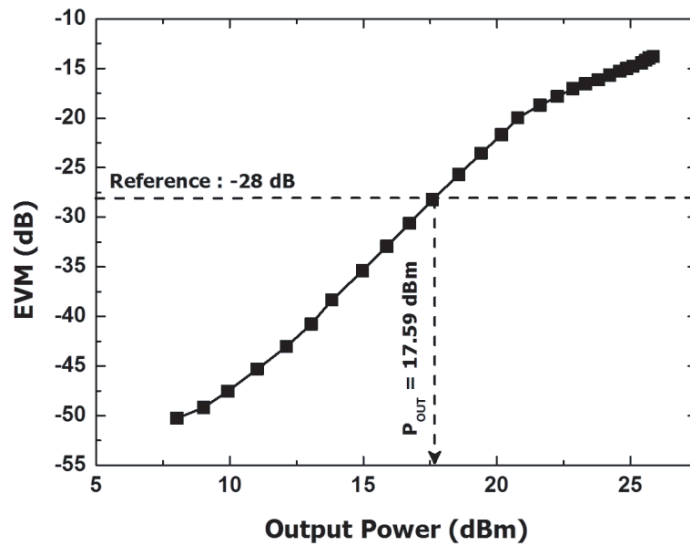

Figure 10. Measured results: EVM according to the output power with a 802.11n WLAN-modulated input signal (64-QAM, 9.6 dB PAPR, 20-MHz bandwidth).

Table 1 shows the summary and performance comparison of CMOS power amplifier for WLAN applications. As can be seen in Table 1, the proposed power amplifier has the highest gain. Although the maximum linear output power, P_{OUT}, is somewhat low, the output power could be improved when the linearization technique is applied.

Table 1. Summary and performance comparison of recent CMOS PAs for WLAN.

| Ref.	Tech./V_{DD}	Signal	P_{OUT} (dBm)	Gain (dB)	EVM (dB)	Freq. (GHz)	Matching Integration	Characteristic
[24] 2010 JSSC	CMOS 65 nm/3.3 V	802.11n 64-QAM 20 MHz	20.5	12	-25	5.5	Input/ Output	Dual-Band (2.4 & 5-GHz band)
[25] 2009 JSSC	SiGe HBT 180 nm/3.3 V	802.11n 64-QAM 20 MHz	18.3 (17.0)	27	-25 (-28)	5.0	Input/ Output	Dual-Band (2.4 & 5-GHz band)
This work	CMOS 180 nm/3.3 V	802.11n 64-QAM 20 MHz	17.59	29.23	-28	4.5	Input/ Output	Asymmetrical Input Transformer
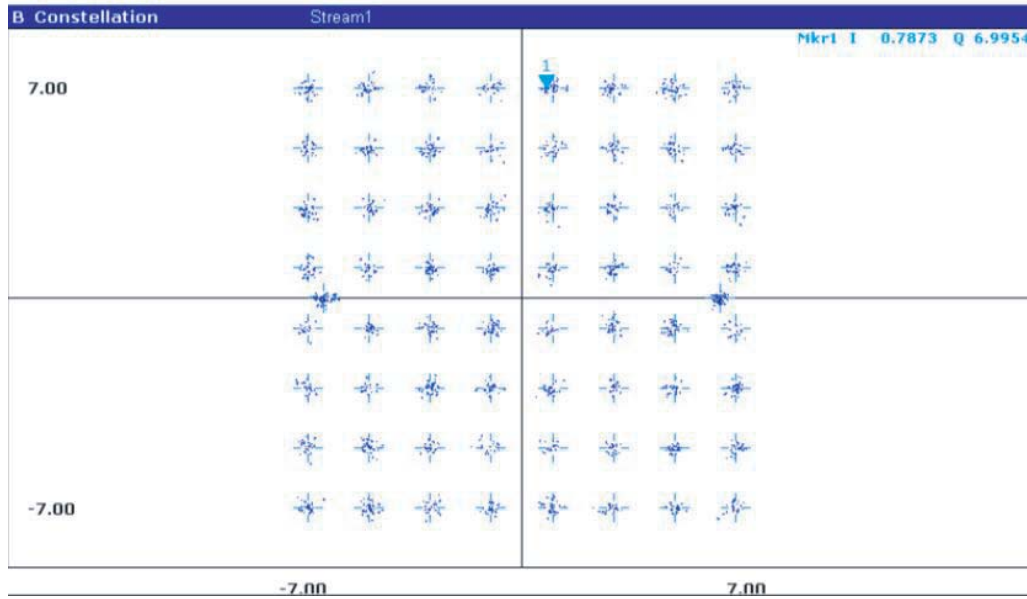
Figure 11. Measured results: signal constellation with a 802.11n WLAN-modulated input signal.
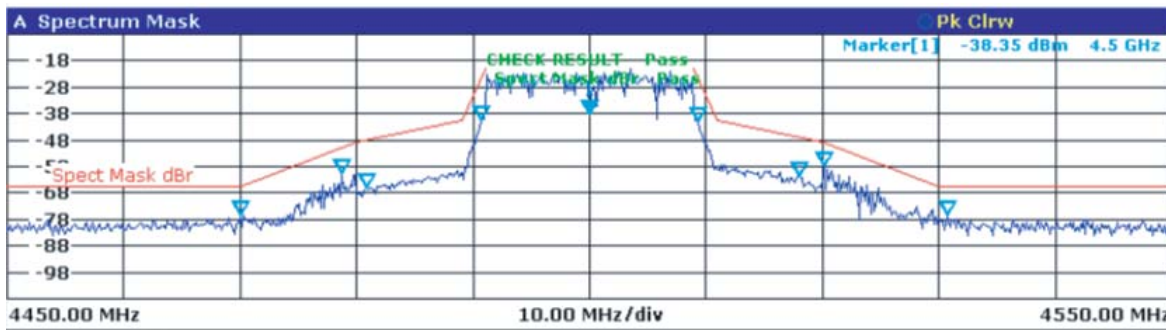

Figure 12. Measured results: spectrum with a 802.11n WLAN-modulated input signal.

6. CONCLUSION

In this study, to mitigate the losses caused by the magnetic coupling of the input transformers utilized in RF CMOS power amplifiers, we propose an asymmetrical input transformer which acts as an input balun. Unlike the typical input transformer, the primary part of the proposed asymmetrical input transformer is directly connected to one of the inputs of a differential driver stage. One of the inputs of the differential driver stage can then be driven without losses caused by magnetic coupling in the transformer. To obtain the differential signal in the output of the proposed transformer, the turn ratio of the proposed transformer is determined upon consideration of the coupling factor of the transformer. In this work, the transformer has a turn ratio of 2 : 1 to ensure proper differential operation. Considering the loss caused by magnetic coupling in only one of the differential inputs of the driver stage, the overall gain of the differential CMOS power amplifier is improved. To verify the functionality of the proposed asymmetrical input transformer for a differential CMOS power amplifier, we design a differential CMOS power amplifier using the 180-nm SOI RF CMOS process. In the measurements, an IEEE 802.11n WLAN modulated signal with a 64-QAM, 9.6 dB PAPR, and a signal bandwidth of 20 MHz is used. We obtain maximum linear output power of 17.59 dBm with a gain of 29.23 dB. The chip size of the designed fully integrated CMOS power amplifier is 0.885 mm². From the measured results of the power amplifier, the functionality of the proposed asymmetrical transformer as the input balun is successfully verified.

ACKNOWLEDGMENT

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