An Asymmetric-Width Broad-Side Coupled Transformer to Reduce the Parasitic Coupling Capacitance for CMOS Power Amplifier Applications

Jonghoon Park, Changhyun Lee, and Changkun Park[1]

Abstract—In this study, we propose a broad-side coupled transformer with reduced capacitance for RF CMOS power amplifier applications. The width of the secondary winding is decreased to reduce parasitic coupling capacitance. Additionally, an auxiliary primary winding is added to improve the coupling between the primary and secondary windings. To prove feasibility of the proposed transformer, we design the transformer using 180-nm RF CMOS technology. From the simulated results of a typical transformer and the proposed broad-side coupled transformer, we successfully find that the parasitic coupling capacitance of the proposed structure is reduced compared to that of a typical structure. Additionally, the auxiliary primary winding increases the maximum available gain of the proposed transformer.

1. INTRODUCTION

Recently, on-chip transformers have become essential in fully-integrated RF CMOS power amplifiers [1–3]. In general, this type of transformer serves as an output balun and as a key component of the output matching network in RF CMOS power amplifiers, as shown in Figure 1, assuming that the typical CMOS power amplifier is designed using a differential structure [4–7]. Although there has been much active research to improve the overall efficiency of RF CMOS power amplifiers, most studies related to CMOS power amplifiers have focused on improving the circuit structure [8–11].
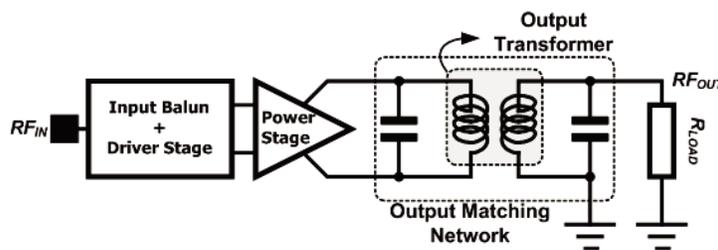

Figure 1. Simple block-diagram of the typical CMOS power amplifier using transformers as an output balun.

Given that loss and parasitic components of the output transformer directly influence the overall efficiency and maximum output power of the CMOS power amplifier, research related to the output transformer is required [3, 12, 13]. Accordingly, first, we simulate a typical broad-side coupled

transformer, which is one of the most popular transformers used as an output balun. Next, we describe the proposed broad-side transformer structure, which reduces the parasitic coupling capacitance compared to that of the typical structure.

2. TYPICAL ON-CHIP TRANSFORMER

In general, the most popular transformers for RF CMOS power amplifier applications are the edge-side coupled and broad-side coupled transformers [14, 15]. Given that edge-side coupled transformers use a top metal layer which is the thickest among all of the metal layers used for the primary and secondary windings, the loss induced by the lossy silicon substrate and the parasitic coupling capacitance between the primary and secondary windings can be minimized. This allows the edge-side coupled transformer to find wide use in RF CMOS power amplifiers. However, the magnetic coupling between the primary and secondary windings is limited to the edges of these windings, which degrades the coupling factor k.

On the other hand, the broad-side coupled transformer shown in Figure 2 uses a secondary winding implemented with a fifth metal layer with the sixth metal layer being the top layer of the semiconductor manufacturing process used. As shown in Figure 2, the primary and secondary windings of the transformer are overlapped to enhance the interaction between the two windings. Accordingly, the coupling factor, k, of the broad-side coupled transformer is higher than that of the edge-side coupled transformer in general. However, excessive parasitic coupling capacitance between the two windings of the broad-side coupled transformer restricts the bandwidth of circuits which use the broad-side coupled transformer. Additionally, given that the fifth metal layer used for the secondary winding is closer to the substrate than the sixth metal layer, the substrate loss may be higher than that of an edge-side coupled transformer. Consequently, the edge-side coupled transformer is more popular than the broad-side coupled transformer in spite of the good coupling characteristics of the broad-side coupled transformer.
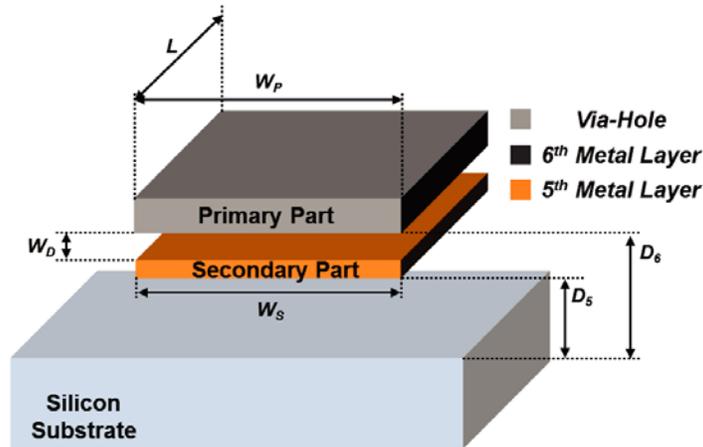

Figure 2. Structure of a typical broad-side coupled transformer.

3. PROPOSED BROAD-SIDE COUPLED TRANSFORMER WITH AN AUXILIARY PRIMARY WINDING

Figure 3 shows the structure of the proposed on-chip broad-side coupled transformer with a reduced width of the secondary winding (W_S) compared to that of the primary winding (W_P). In general, the current through the secondary winding is lower than that of the primary winding given that the coupling factor is always lower than one. Accordingly, the optimum value of W_S is smaller than that of W_P. If the DC power supply entering the virtual ground occurring at the primary winding for the differential RF CMOS power amplifier is considered, the difference between the optimum values of W_P and W_S increases. Consequently, to reduce the parasitic coupling capacitance between the primary
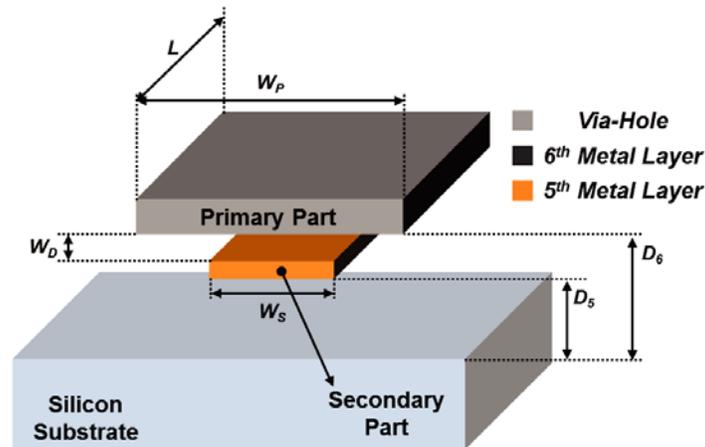
Figure 3. Structure of the proposed asymmetric-width broad-side coupled transformer.
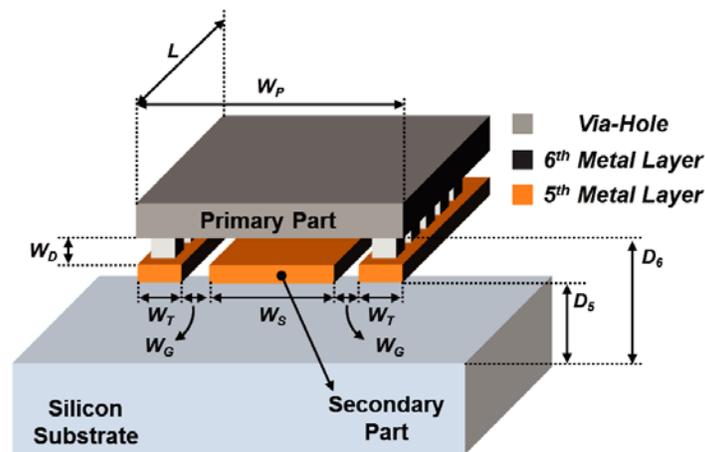

Figure 4. Structure of the proposed asymmetric-width broad-side coupled transformer with an auxiliary primary winding.

and secondary windings, an asymmetric-width structure, as shown in Figure 3, can be a solution for a typical broad-side coupled transformer. However, although the parasitic coupling capacitance of the asymmetric-width structure can be reduced, the magnetic coupling of the asymmetric-width structure should also be lowered compared to that of a typical broad-side coupled transformer.

In this study, we propose an asymmetric-width broad-side coupled transformer with an auxiliary primary winding (APW) to improve the magnetic coupling compared to that of an asymmetric-width broad-side coupled transformer. The parasitic coupling capacitance is also reduced compared to that of a typical broad-side coupled transformer. Figure 4 shows a cross-section of the proposed asymmetric-width broad-side coupled transformer with an APW.

The width of the secondary winding in Figure 4 is also reduced, as that in Figure 3. However, to improve the magnetic coupling between the primary and secondary windings of the transformer, an auxiliary winding is added using the fifth metal layer; in this work, we simulate the transformers using 180-nm RF CMOS technology, which provides six metal layers. The APW is connected to the primary winding, consisting of the sixth metal layer, through a via-hole. Accordingly, the edge sides of the APW and the secondary winding contribute to the additional magnetic coupling. Although the edge sides of the APW and the secondary winding face each other, given that the thickness of the fifth metal layer is much thinner than that of the width of the secondary winding, the increase in the parasitic coupling capacitance is typically negligible, as will be simulated in the following sections.

4. INVESTIGATION AND COMPARISON OF THE TYPICAL AND PROPOSED TRANSFORMER

To prove feasibility of the proposed transformer, we design a typical transformer and the proposed transformer, as depicted in Figures 2, 3, and 4. This study utilizes the 180-nm RF CMOS technology, in which a sixth metal layer is used as the top layer. With this technology, D_5 and D_6 are 6.5 μm and 8 μm, respectively. The thicknesses of the fifth and sixth metal layers are 0.5 μm and 2.34 μm, respectively. W_D and W_G are identical at 1 μm. W_T for the proposed transformer with APW is varied according to W_S and hence equals $0.5W_P - 0.5W_S - (W_G + 1)$. The W_S value of the typical transformer is fixed at 50 μm. The geometries of transformers used for electrometric simulation are identical to the geometries shown in Figures 2, 3, and 4 while the lengths L of the primary and secondary windings are fixed at 1.0 mm.
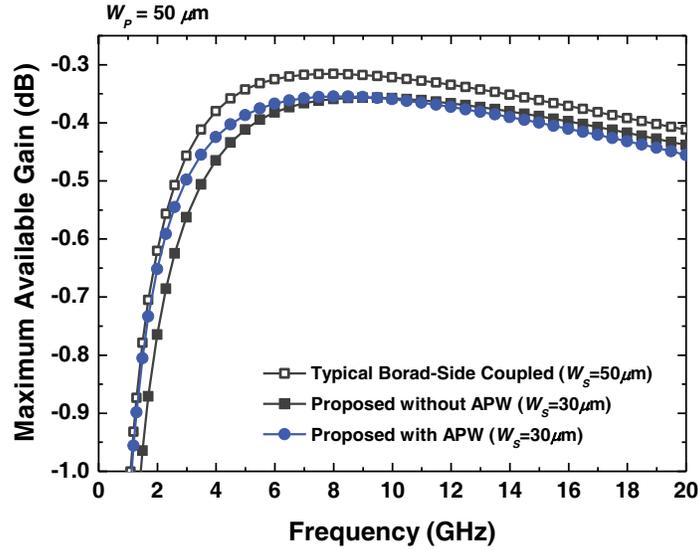

Figure 5. Maximum available gains of a typical transformer and the proposed transformer according to the frequency.

Figure 5 shows the simulated maximum available gain (MAG) for the proposed and typical transformers. In Figure 5, W_S values for the proposed and typical transformers are 30 μm and 50 μm, respectively. As predicted in the previous section, the MAG of the proposed transformer with the APW is located between those of the typical and the proposed transformer without an APW for a frequency lower than 10 GHz.

Figure 6 shows the simulated maximum available gain (MAG) for the proposed and typical transformers according to W_S at an operating frequency of 1.9 GHz. In this work, we assume that the transformers would be applied to the 1.9-GHz CMOS power amplifier. Except when $W_S = 45$ μm, the MAG of the proposed transformer with an APW is higher than the proposed transformer without an APW. As shown in Figure 6, with $W_S = 38$ μm, the MAG of the proposed transformer with an APW is nearly identical to that of a typical broad-side coupled transformer while the proposed transformer without an APW is continuously degraded as the value of W_S decreases. This phenomenon occurs because the APW increases the magnetic coupling in the proposed transformer with an APW while the magnetic coupling in the proposed transformer without an APW is nearly proportional to the value of W_S.

Figure 7 shows the estimated relative coupling capacitances occurring between the primary and secondary windings of the transformers. The normalized relative coupling capacitance is calculated using the normalized area of the secondary winding facing the primary winding. During this normalization process, the area of the typical broad-side coupled transformer is used as the reference. As shown in Figure 7, the parasitic coupling capacitance of the proposed transformer with an APW is nearly identical
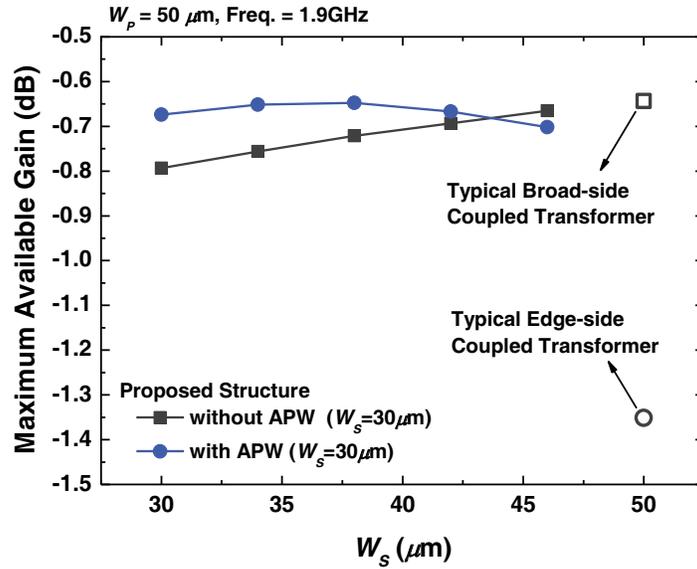
$W_P = 50 \ \mu m$, Freq. = 1.9GHz

Figure 6. Maximum available gains of the typical and proposed transformers according to the width of the secondary winding.
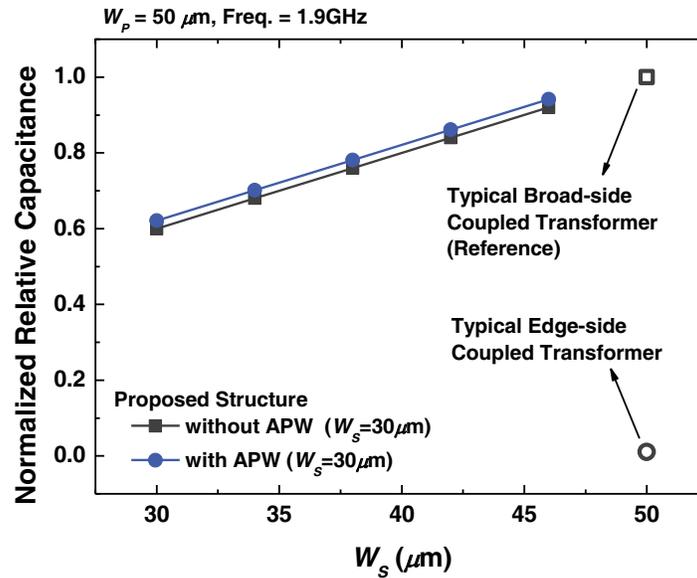

Figure 7. Estimated normalized relative coupling capacitances of the typical and proposed transformers.

to that without an APW. For example, with $W_S = 38 \ \mu m$, the parasitic coupling capacitance of the proposed transformers with an APW and without an APW decreases to 78% and 76%, respectively, of that of a typical broad-side coupled transformer, while the MAG of the proposed transformer with an APW is 0.8 dB higher than that without an APW.

Consequently, the proposed transformer with an APW has reduced parasitic coupling capacitance compared to that of a typical broad-side coupled transformer, while the degradation of the MAG is nearly negligible.

Figure 8 shows the simulated coupling factors for the proposed and typical transformers. In Figure 8, the W_S values for the proposed and typical transformers are 38 μm and 50 μm, respectively. Because the magnetic coupling in the proposed transformer without APW is nearly proportional to the value

of W_S, the coupling factor of the proposed transformer without APW is lower than that of typical broad-side coupled transformer. However, by virtue of the APW, the proposed transformer with APW has the highest coupling factor among the transformers.

Figure 9 shows the simulated quality factors of primary and secondary windings. As shown in Figure 9(a), given that the parasitic resistance of the primary winding of the transformer with APW is reduced by virtue of APW, the transformer with APW has the highest quality factor among the transformers for a frequency lower than 6.5 GHz. Although the widths of primary windings of the typical broad-side transformer and the proposed transformer without APW are identical, because the parasitic coupling capacitance of the proposed transformer without APW is smaller than that of the typical transformer, the quality factor of the transformer without APW is slightly higher than that of the typical transformer.

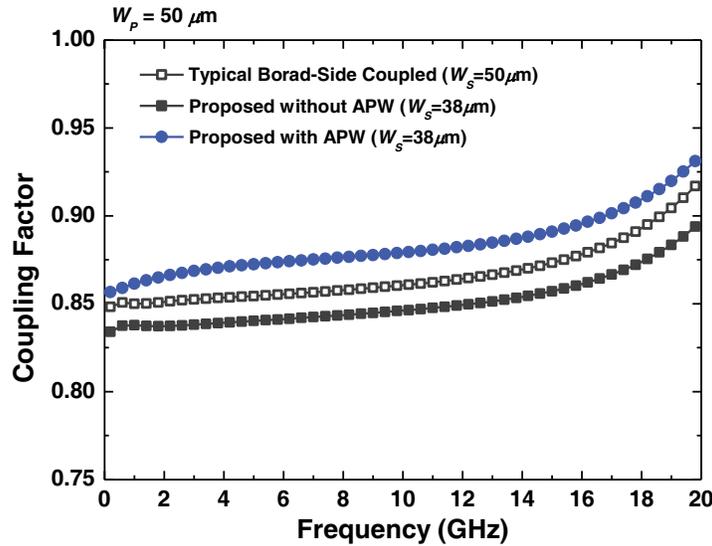Conversely, as shown in Figure 9(b), because the widths of the secondary windings of the proposed

Figure 8. Coupling factors of a typical transformer and the proposed transformer according to the frequency.
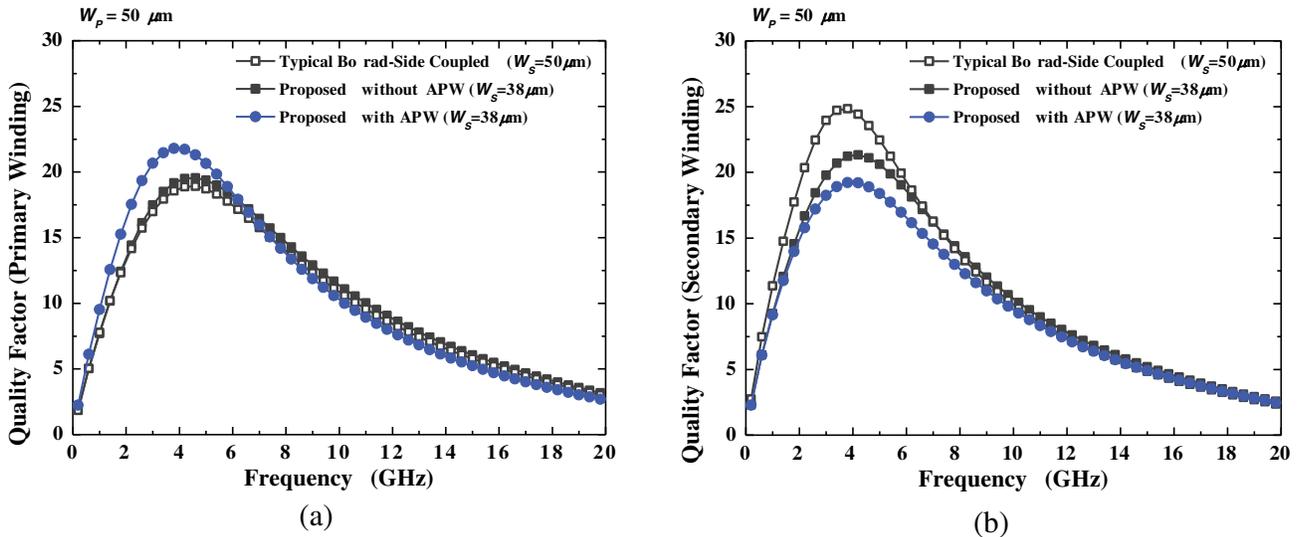

Figure 9. Simulated quality factors of (a) primary and (b) secondary windings.

transformers are smaller than that of the typical broad-side coupled transformer, the typical transformer has the highest quality factor among the transformers. Additionally, given that the parasitic coupling capacitance of the proposed transformer without APW is smaller than that of the transformer with APW, the quality factor of the transformer without APW is higher than that of the transformer with APW.

Figure 10 shows the simulated inductances of primary and secondary windings. As shown in Figure 10(a), given that the APW decreases the inductance of the primary winding, the inductance of the proposed transformer with APW is lowest among the transformer. Conversely, as shown in Figure 10(b), because the typical broad-side coupled transformer has the widest width of the secondary winding among the transformers, the typical transformer has the lowest inductance of secondary winding among the transformers.
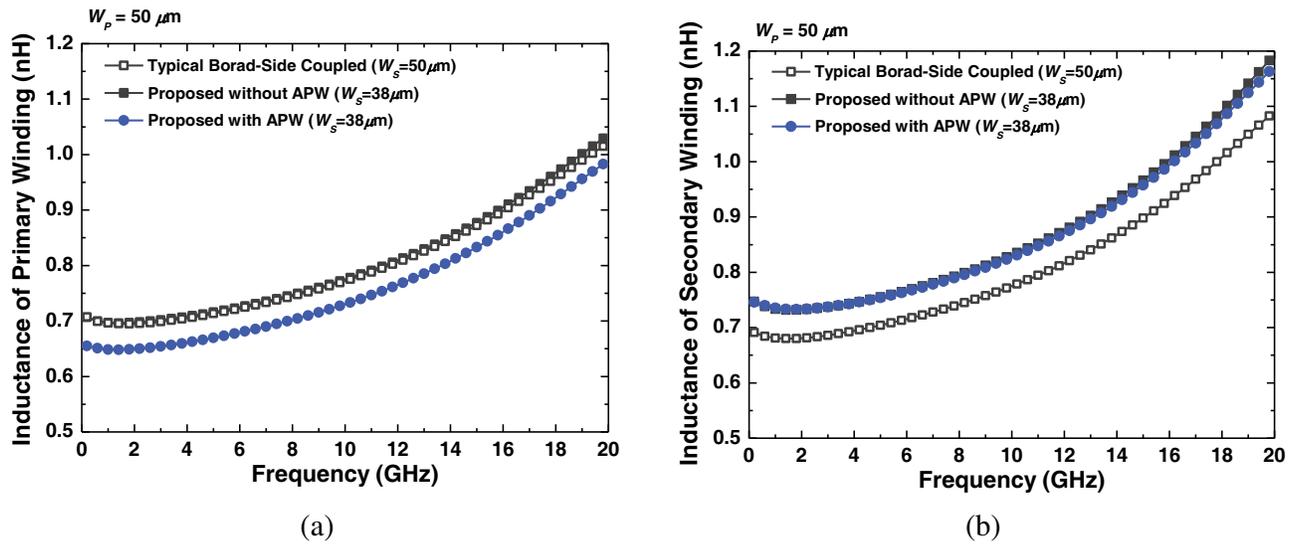

(a)   (b)

Figure 10. Simulated inductances of (a) primary winding and (b) secondary winding.
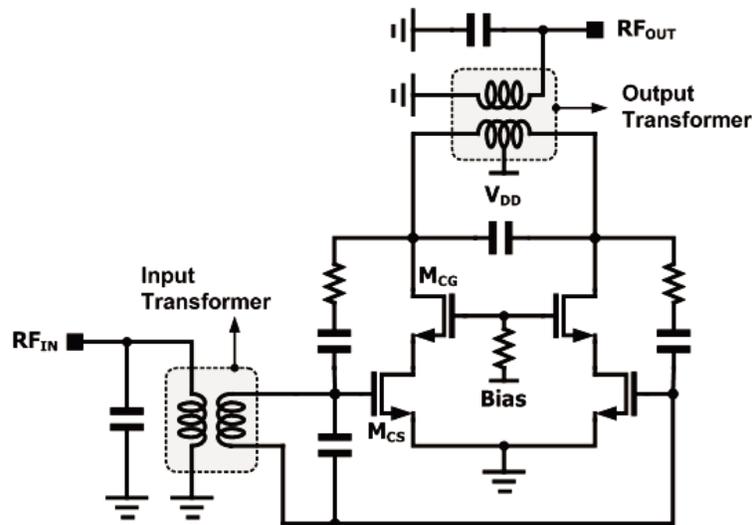

Figure 11. Schematic of the CMOS power amplifier using an output transformer.

5. DESIGN OF CMOS POWER AMPLIFIER USING PROPOSED TRANSFORMERS

We design a differential 1.9-GHz CMOS power amplifier using the 180-nm CMOS process, which provides on poly and six metal layers. Figure 11 shows a schematic of the designed power amplifier with typical and proposed output transformers. The total gate lengths of M_{CS} and M_{CG} are $5,120\,\mu m$. M_{CS} and M_{CG} are designed with 180-nm and 350-nm unit transistors, respectively. The R-C feedback network comprises power amplifier to obtain linearity and stability. The typical and proposed transformers are used for the output matching network of the power amplifier to convert it from a differential signal to a single-ended one. The transformer has a 1:1 turn-ratio with $50\,\mu m$ of width for primary winding. The outer size of the output transformer is $600\,\mu m \times 600\,\mu m$. The W_G and W_T for the proposed transformer with APW are $1\,\mu m$ and $5\,\mu m$, respectively.
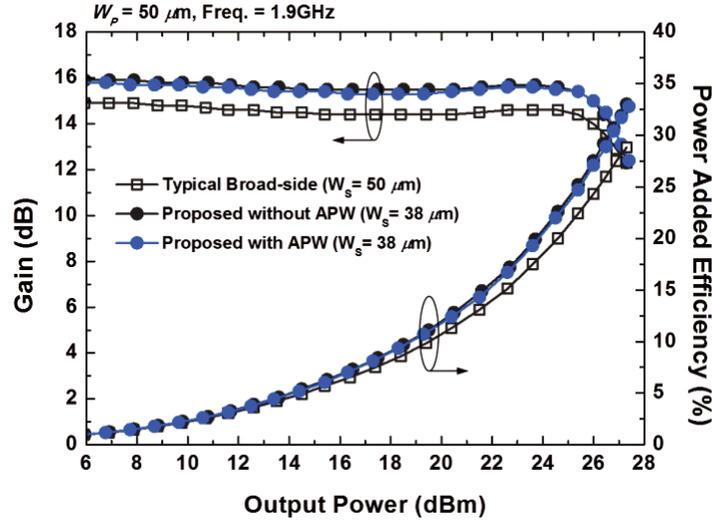

Figure 12. Simulated gain and power added efficiency.

Figure 12 shows the simulated gain and power added efficiency of the designed CMOS power amplifier using typical and proposed transformers. As provided in Figure 12, the gains and power added efficiencies for the proposed transformers are higher than those for typical transformer.

6. CONCLUSION

Although a typical broad-side coupled transformer has high magnetic coupling characteristics, the excessive parasitic coupling capacitance between the primary and secondary winding prevents the wider use of these transformers in RF CMOS power amplifier applications. In this study, we propose a broad-side coupled transformer with an auxiliary primary winding (APW) to minimize the parasitic coupling capacitance while the degradation of the maximum available gain (MAG) is held mostly steady. To prove the feasibility of the proposed structure, we design a typical transformer and the proposed transformer using 180-nm RF CMOS technology. From simulated results, we successfully find that the proposed structure has low parasitic coupling capacitance and nearly identical MAG values compared to those of a typical broad-side coupled transformer. We also show that the proposed transformer improves the gain, efficiency, and output power of CMOS power amplifiers without additional chip area.

ACKNOWLEDGMENT

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