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Switching-Mode CMOS Power Amplifier Using a Differentially Coupled Series Inductor

Changhyun Lee and Changkun Park*

Abstract—In this work, we propose a compact CMOS power amplifier using a differentially coupled series inductor for motion detection radar applications. The proposed switching-mode power amplifier is designed with a cascode and differential structure. To realize a compact size matching network, a differentially coupled series inductor is used in the input matching network. In the proposed power amplifier, two typical spiral series inductors for the input matching network are replaced with a single differentially coupled series inductor. As a result, the used chip area of the differentially coupled series inductor is smaller than half that of a typical inductor for the given inductances of each inductor. Additionally, to obtain a high gain characteristic, we adapt modified mode-locking techniques for the power stage of the power amplifier. To verify the feasibility of the power amplifier, we design a 9.5-GHz power amplifier with a 130-nm RFCMOS process. We obtain saturation power of 15 dBm while the power-added efficiency is approximately 28%.

1. INTRODUCTION

Power amplifier is an essential component to complete wireless sensor networks (WSNs) [1–4]. Generally, power amplifiers occupy considerable chip area and consume the greatest amount of battery power among all RFICs [5–9]. Accordingly, to reduce the unit cost of production, compact design of power amplifiers is essential [10–13]. To this end, the matching networks for power amplifiers should be fully integrated. Furthermore, the number of spiral inductors, which are the most bulky device in the integrated-circuit (IC), should be minimized. Additionally, to extend battery lifetime, the power-added efficiency (PAE) of the power amplifier should be improved. Although various studies to improve the efficiency of power amplifiers have been reported, sophisticated efficiency-enhancement techniques that require additional chip area are unsuitable for compact and low-cost WSN system applications.

In this work, we propose a nonlinear CMOS power amplifier using a differentially coupled series inductor as a component of the input matching network to reduce the number of required spiral inductors and hence the whole chip area. At the same time, to obtain high efficiency, we adapt a modified mode-locking technique in the power stage of the amplifier. Compared to the typical mode-locking technique, the closed loop is removed in the modified mode-locking technique while the advantage of the cross coupled structure of the typical mode-locking is maintained.

2. TYPICAL NONLINEAR CMOS POWER AMPLIFIER

Figure 1 shows the input part of the typical CMOS power amplifier structure to describe the necessity of the inductor in the input matching network. As can be seen in Fig. 1, given that the size of the transistor used for the power stage of the power amplifier is generally largest in the RFICs, the

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* Corresponding author: Changkun Park (pck77@ssu.ac.kr).
The authors are with School of Electronic Engineering, Soongsil University, 369, Sangdo-ro, Dongjak-gu, Seoul 06978, Republic of Korea.

unavoidable gate-source parasitic capacitance C_{GS} considerably affects the input impedance of the power amplifier. Furthermore, the parasitic capacitance C_{PAD} induced by the input pad should also be taken into consideration for the input matching network. Accordingly, given that the parasitic capacitances of C_{GS} and C_{PAD} should be cancelled out to obtain 50-Ω input impedance, the usage of a series or shunt inductor is essential in the input matching network. If the shunt inductor is used to cancel out the parasitic capacitance, the inductor can also act as the gate bias circuit of the power amplifier. Alternatively, in Fig. 1, we illustrate the case where the series inductor L_{IN} is used to cancel out the parasitic capacitance.

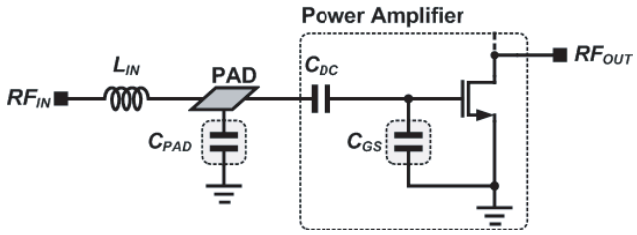
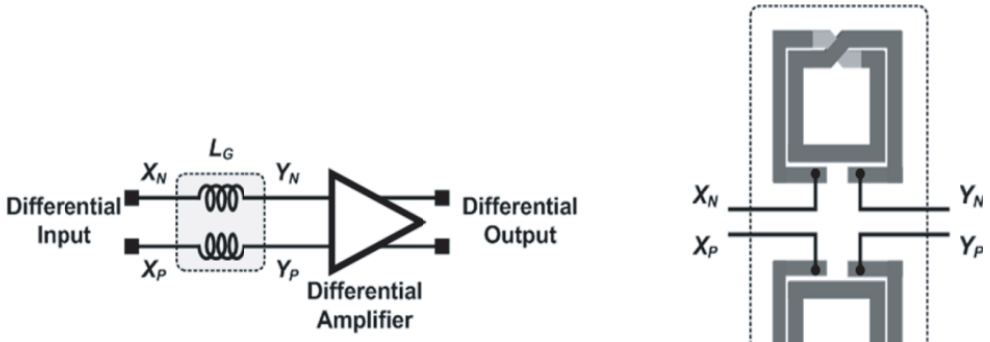


Figure 1. Input part of the typical CMOS power amplifier structure.

Although we describe the necessity of the inductor L_{IN} in the input matching network through the single-ended structure in Fig. 1, the same description can be applied to the differential structure. As shown in Fig. 2(a), for the case of the differential structure of the power amplifier, the number of required inductors for the input matching network should be double compared to the case of a single-ended structure. Moreover, given that the inductor L_G is the bulkiest device in the RFIC, the inductors in the input matching network for the differential structure require considerable chip area, as can be easily predicted in Fig. 2(b). Consequently, the inductors are regarded as one of the crucial obstacles to design fully integrated compact RFICs. Additionally, the low quality-factor of an integrated inductor L_G degrades the gain of the power amplifier, and hence the power-added efficiency [14].



(a) (b)

Figure 2. Typical series inductor: (a) differential CMOS power amplifier with series inductors and (b) layout of series inductors.

3. PROPOSED POWER AMPLIFIER USING A DIFFERENTIALLY COUPLED SERIES INDUCTOR

We propose a nonlinear CMOS power amplifier using a differentially coupled series inductor in the input matching network to solve the problems that arise in the typical fully integrated power amplifier.

For the case of single-ended input and a differential structure of the amplifier, the input balun that is generally designed using a transformer provides parasitic shunt inductance. Accordingly, in this case, the parasitic shunt inductance can cancel out the unavoidable input capacitances. However, if the differential power amplifier has differential inputs, there is no parasitic inductance, which is available by virtue of the input balun for the case of the singled-ended input of the differential amplifier.

In this work, we replace the typical input inductor shown in Fig. 2(a) with the differentially coupled series inductor shown in Fig. 3. As can be easily predicted, the required chip area of the differentially coupled series inductor is smaller than half that of a typical inductor for the given inductances of each inductor [14]. Additionally, the inductance of the differentially coupled inductor is higher than that of a typical inductor by virtue of the mutual inductance of the differentially coupled inductor while the parasitic resistance is identical [14]. Accordingly, the power loss of the differentially coupled series inductor is lower than that of the typical inductor [14]. Consequently, by virtue of the differentially coupled series inductor, the gain and the PAE of the power amplifier can be improved with compact chip size.

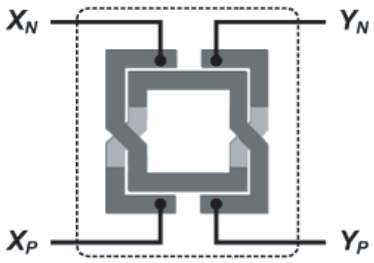


Figure 3. Differentially coupled series inductor for input-matching networks.

Figure 4 shows a simple schematic of the proposed nonlinear CMOS power amplifier using the differentially coupled series inductor. The amplifier is designed with a differential cascode structure to mitigate the gain reduction and reliability problems. The modified mode-locking structure proposed in the previous work is used to obtain high gain and stability at the same time [15]. Since the closed loop in the typical mode-locking structure is removed, the stability is enhanced in the modified mode-locking structure. At the same time, the advantages of the cross coupled structure of the typical mode-locking amplifier are maintained in the modified mode-locking amplifier [15].

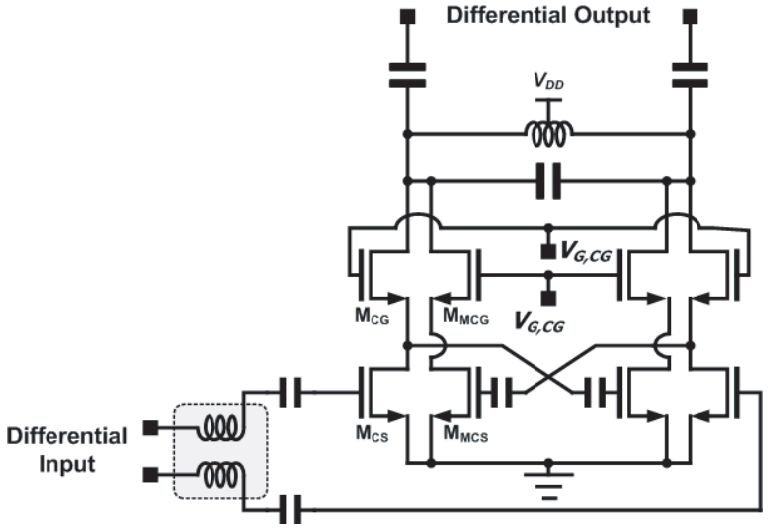


Figure 4. Simple schematic of the proposed power amplifier using a differentially coupled series inductor.

The load impedance designed by the inductor shown in Fig. 4 is shared by two amplifiers: one is composed of M_{CS} and M_{CG}, and the other is composed of M_{MCS} and M_{MCG}. Although a modified mode-locking structure was proposed for the linear amplifier applications in the previous work [15], we adjust the gate bias and the transistor size for the amplifier to operate as an overdriven class-E amplifier in this work. To extract the characteristics of the proposed structure, we designed the amplifier with a single-stage structure. Given that the designed power amplifier has differential inputs and outputs, there are no input and output baluns. The transistor sizes of the designed power amplifier are summarized in Table 1. To mitigate reliability problems, 300-nm transistors are used in the common-gate transistors, M_{CG} and M_{MCG}.

Table 1. Transistor sizes in the designed power amplifier.

Transistor	Length (nm)	Unit gate width (μm)	Number of fingers	Number of multipliers
M_{CS}	130	10	15	1
M_{MCS}	130	10	4	1
M_{CG}	300	10	15	1
M_{MCG}	300	10	8	1

4. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed amplifier, we design a 9.5-GHz nonlinear CMOS power amplifier using 130-nm RF CMOS technology, which provides eight metal layers. Fig. 5 shows a chip photograph of the designed power amplifier with chip area of $0.84 \times 0.64\,\text{mm}^2$. All of the components, including the input- and output-matching networks and test pads, are fully integrated. Compared with a previous work [1], the designed power amplifier has more compact size and higher output power.

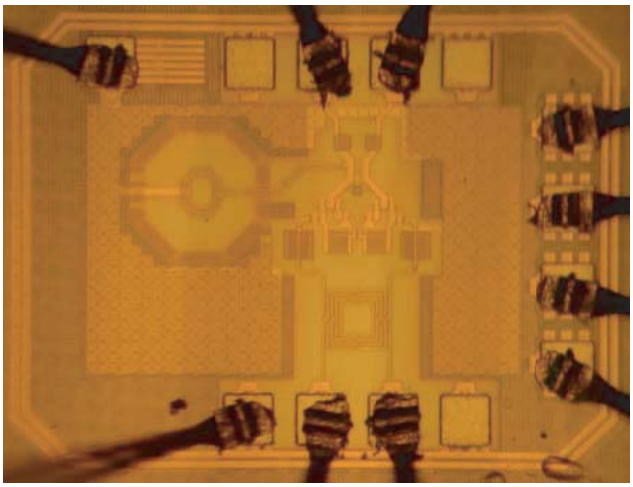


Figure 5. Chip photograph of the designed power amplifier.

Figure 6 shows the measured power gain according to the output power at various operating frequencies. As can be seen in Fig. 6, the measured saturation power is approximately 15 dBm while the gain is 12.5 dB at a frequency of 9.5-GHz. Fig. 7 shows the measured PAE according to the output power. The highest PAE value is approximately 28% at operation frequency of 9.5 GHz.

The performance results are compared with other fully integrated CMOS power amplifiers in Table 2. Compared with other CMOS power amplifiers, the designed power amplifier has more compact size.

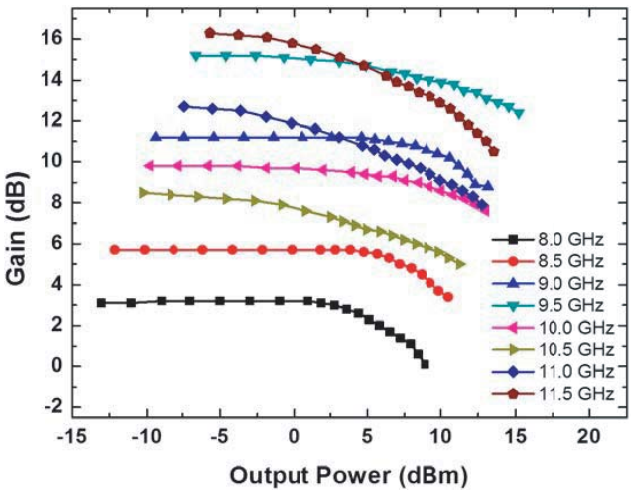


Figure 6. Measured gain according to the output power.

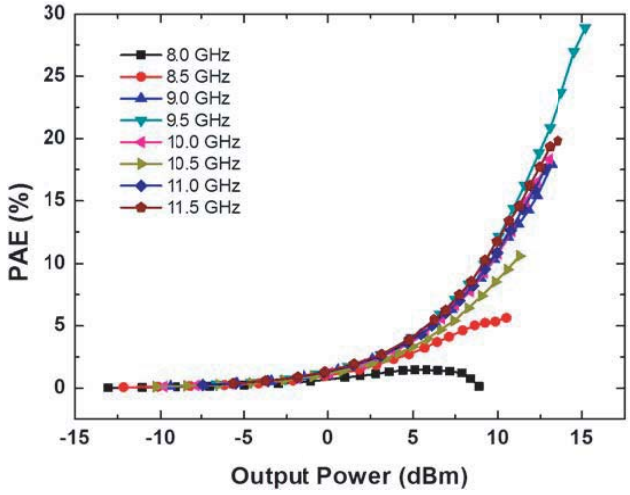


Figure 7. Measured power added efficiency according to the output power.

Table 2. Performance comparison with other fully integrated CMOS power amplifiers.

Reference	Tech. (nm)	Frequency (GHz)	Gain (dB)	P_{SAT} (dBm)	PAE (%)	V_{DD} (V)	Area (mm^2)
[1]	300 (CMOS)	8	19.3	12	32	2.5	0.74
[16]	180 (CMOS)	8.5	29	23.5	19	3.3	1.28
[17]	180 (CMOS)	3.7–8.8	8.2	19	25	N/A	2.8
[18]	250 (SiGe)	8.5	12.2	21.2	27.4	3.3	0.86
[19]	250 (SiGe)	10	12	16.2	10.3	5.0	2.1
This work	130 (CMOS)	9.5	15	15	28	2.0	0.54

5. CONCLUSION

In this work, we propose a nonlinear CMOS power amplifier using a differentially coupled series inductor as one of the input matching components. The differentially coupled series inductor cancels out the unavoidable parasitic capacitance of the input part of the CMOS power amplifier with compact chip area. Using an input matching network with the differentially coupled series inductor, the chip size of a differential power amplifier that has differential inputs can be effectively reduced. To verify the feasibility of the proposed power amplifier, we design the power amplifier using a 130-nm RFCMOS process for WSN applications. From the measured results, we successfully prove the feasibility of the proposed power amplifier.

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REFERENCES

1. Park, J., C. Lee, and C. Park, "X-band CMOS power amplifier with high efficiency for motion detection radar," *Microw. Opt. Technol.*, Vol. 56, 2552–2557, 2014.

2. Yang, J.-R., S. Hong, and D.-W. Kim, "A distance-compensated radar sensor with a six-port network for remote distinction of objects with different dielectric constants," *Journal of Electromagnetic Waves and Applications*, Vol. 24, No. 11/12, 1429–1437, 2010.
3. Chang, C. H., S. Wang, H. S. Wu, E.-C. Liang, A.-S. Liu, K.-H. Tsai, M.-J. Chiang, P.-J. Yang, Y.-J. Wu, H. Lee, and C.-K. C. Tzuang, "Design of X-band complementary metal-oxide semiconductor-based frequency-modulation continuous-wave sensor," *IET Circ. Devices Syst.*, Vol. 3, 331–339, 2009.
4. Haridas, K., T. H. Teo, and X. Yuan, "A 2.4-GHz CMOS power amplifier design for low power wireless sensors network," *IEEE International Symposium on Radio-Frequency Integration Technology*, 299–302, 2009.
5. Lee, J., D.-H. Lee, and S. Hong, "A doherty power amplifier with a GaN MMIC for femtocell base stations," *IEEE Microw. Wireless Compon. Lett.*, Vol. 24, 194–196, 2014.
6. Wilk, S. J., W. Lepkowski, and T. J. Thornton, "32 dBm power amplifier on 45 nm SOI CMOS," *IEEE Microw. Wireless Compon. Lett.*, Vol. 23, 161–163, 2013.
7. Chen, J.-H., S. R. Helmi, A. Y.-S. Jou, and S. Mohammadi, "A wideband power amplifier in 45 nm CMOS SOI technology for X band applications," *IEEE Microw. Wireless Compon. Lett.*, Vol. 23, 587–589, 2013.
8. Lee, G., J. Jung, J. Jang, and J. Song, "A multiband power amplifier using a switch-based reconfigurable matching network for optimized power performance," *Microw. Opt. Technol.*, Vol. 56, 2881–2884, 2014.
9. Mohadeskasaei, S. A., F. Lin, X. Zhou, and S. U. Abdullahi, "Novel design theory for high-efficiency and high-linearity microwave power amplifier based on 2nd harmonic: Enhanced class-J," *Progress In Electromagnetics Research M*, Vol. 57, 103–111, 2017.
10. Tai, H.-Q., W. Hong, B. Zhang, and X.-M. Yu, "A compact 60 W X-band GaN HEMT power amplifier MMIC," *IEEE Microw. Wireless Compon. Lett.*, Vol. 27, 73–75, 2017.
11. Lee, H., W. Lim, W. Lee, H. Kang, J. Bae, C.-S. Park, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Compact load network for GaN-HEMT doherty power amplifier IC using left-handed and right-handed transmission lines," *IEEE Microw. Wireless Compon. Lett.*, Vol. 27, 293–295, 2017.
12. Zhang, Y. and K. Ma, "A 2–22 GHz CMOS distributed power amplifier with combined artificial transmission lines," *IEEE Microw. Wireless Compon. Lett.*, Vol. 27, 1122–1124, 2017.
13. Liu, B., M. Mao, D. Khanna, P. Choi, C. C. Boon, and E. A. Fitzgerald, "A highly efficient fully integrated GaN power amplifier for 5-GHz WLAN 802.11ac application," *IEEE Microw. Wireless Compon. Lett.*, Vol. 28, 437–439, 2018.
14. Lee, C., S. Yoon, and C. Park, "A differentially coupled series inductor for differential RFICs," *Microw. Opt. Technol.*, Vol. 57, 2223–2225, 2015.
15. Lee, C. and C. Park, "A 2.4-GHz CMOS power amplifier using a gain and stability enhancement technique for IEEE 802.11n WLAN applications," *Microw. Opt. Technol.*, Vol. 58, 2265–2268, 2016.
16. Ku, B.-H., S.-H. Baek, and S. Hong, "A X-band CMOS power amplifier with on-chip transmission line transformers," *Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, 523–526, April 2008.
17. Lu, C., A.-V. H. Pham, M. Shaw, and C. Saint, "Linearization of CMOS broadband power amplifiers through combined multigated transistors and capacitance compensation," *IEEE Trans. Microw. Theory Tech.*, Vol. 55, 2320–2328, 2007.
18. Kim, H. S., K. Y. Kim, W. Y. Kim, Y. S. Noh, I. B. Yom, I. Y. Oh, and C. S. Park, "SiGe MMIC power amplifier with on-chip lineariser for X-band applications," *Electron. Lett.*, Vol. 45, 1036–1037, 2009.
19. Sewiolo, B., G. Fischer, and R. Weigel, "A 12-GHz high-efficiency tapered traveling-wave power amplifier with novel power matched cascode gain cells using SiGe HBT transistors," *IEEE Trans. Microw. Theory Tech.*, Vol. 57, 2329–2336, 2009.