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Compact Quad-Channel Diplexer Using Defected Stepped Impedance Resonators

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Abstract—This paper proposes a new compact quad-channel diplexer (2.45/4.2 GHz and 3.5/5.2 GHz) using defected stepped impedance resonators (DSIRs). The proposed quad-channel diplexer is composed of one common input feeding line, sixteen folded DSIRs, and two output feeding lines. Every four DSIRs are designed to determine passband characteristics of one individual channel, and two passbands are filtered out eventually at each output port. The distributed coupling technique featured by small loading effect is introduced to eliminate the necessity of extra impedance matching networks, which consequently results in a reduced circuit size. A diplexer prototype operated at 2.45/4.2 GHz and 3.5/5.2 GHz bands with measured 3-dB fractional bandwidths of 12.5%, 7.2%, 6.4%, and 5.0% has been implemented, showing a high isolation of larger than 33 dB between the two output ports. Experimental results coincide well with the theoretical predictions and simulation results.

1. INTRODUCTION

Diplexers are extensively used in modern communication systems to separate one common input signals into two distinct output signals centered at different frequencies, and vice versa [1]. In modern multi-standard and multi-service wireless communication systems, increasingly stringent requirements, including high compactness, low insertion loss, high port isolation, and multi-band response, have been imposed upon diplexer designs. To satisfy these demands, considerable research efforts on designing diplexers can be easily found in the open literature [2–6]. In [2], a compact diplexer using hybrid resonators was proposed to achieve rather high port isolation, but the T-junction combining circuit and shorting vias undoubtedly increased structural complexity and circuit size. Novel microstrip line resonators were invented to realize diplexers [3]. When being loaded by different elements such as resistors, open stubs, and shorted stubs, these resonators can hence be employed to implement diplexers owning diverse characteristics. Common resonator configurations were investigated to construct size-reduced diplexers [4, 5]. Nevertheless, the passband-choosing freedom and capability of multi-band operation are constrained due to the limited coupling area allowed by the common resonator. To accommodate modern wide-band communication systems, a six-channel multiplexer based on parallel-coupled microstrip bandpass filters (BPFs) was introduced in [6]. However, it needs one seven-port input and two four-port output impedance matching networks, occupying an enlarged circuit space. In addition, laboursome design iteration and optimization are indispensable as a result of the strong loading effect.

Recently, microstrip stepped impedance resonators (SIRs) have drawn widespread attention to develop all kinds of microwave devices such as filters [7–9], diplexers [10–12], as well as antennas [13], because the fundamental and spurious resonances can be conveniently tuned by adjusting impedance

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ratio ($K = Z_2/Z_1$) and electrical length ratio ($\alpha = \theta_2/(\theta_1 + \theta_2)$) at the same time [14] to meet desired specifications. Two compact quad-channel diplexers were proposed in [10] and [11], respectively, with the combination of coupled SIRs and distributed coupling technique, wherein each pair of SIRs was elaborated to perform as a two-pole dual-passband BPF. In [12], sixteen microstrip SIRs were employed to fulfill an eight-channel diplexer with wide stopband, and every two SIRs were used to decide one individual two-pole BPF. As the dual of microstrip SIRs, defected SIRs (DSIRs), also well recognized as slotline SIRs, besides flexible passband location mentioned above, have merits of much more compact size and higher power-handling capacity. Hence, several diplexer designs have been investigated with the use of DSIRs [15, 16]. A compact diplexer utilizing T-shaped input feeding line and hairpin DSIRs was proposed for GSM and WLAN applications [15]. A balanced diplexer and a balun diplexer at WLAN and WiMAX bands were studied based on DSIRs [16], possessing high common-mode suppression and differential-mode isolation.

In this work, a new three-port quad-channel diplexer is proposed by combining sixteen folded DSIRs and three distributed coupling microstrip lines. The diplexer shows compact size, high isolation, low insertion loss, and flexible passband location. Thanks to the employment of the distributed coupling technique, additional impedance matching network is needless, and small inter-channel loading effect is maintained, which permits a time-saving design procedure. The feasibility of the proposed diplexer has been confirmed by numerical simulations carried out using Ansoft HFSS 14.0 and experimental measurements with the aid of an Agilent network analyzer E8363B.

2. THREE-PORT QUAD-CHANNEL DIPLEXER DESIGN

Figure 1 depicts the traditional and proposed schematic coupling structures of a quad-channel diplexer, respectively, where dark circles indicate resonators. As found from Figure 1(a), one five-port and two three-port impedance matching networks are needed, in addition to the four channel BPFs, to implement a quad-channel diplexer. On the contrary, multi-port impedance matching networks are circumvented in the proposed scheme, due to the employed distributed coupling technique. When operating in the receive mode, Port 1 indicates a common input port, whereas Port 2 and Port 3 denote output ports. Two dual-passband signals centered at 2.45/4.2 GHz and 3.5/5.2 GHz are filtered out, respectively, for Port 2 and Port 3. It can be observed in Figure 1 that each channel comprises an individual four-pole BPF, and the center frequencies of BPF I–BPF IV are 2.45 GHz, 4.2 GHz, 3.5 GHz, and 5.2 GHz, respectively. Four DSIRs resonating at the fundamental modes are utilized to construct respective BPFs, which supply the proposed diplexer much more design freedoms.

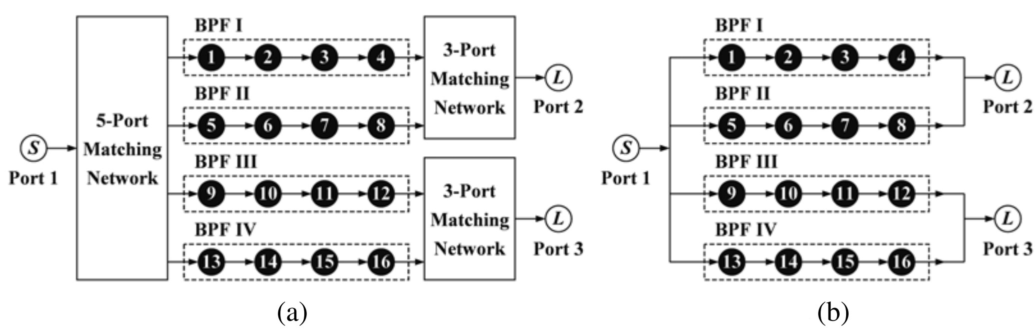


Figure 1. Schematic coupling structures of a three-port quad-channel diplexer. (a) Traditional scheme. (b) Proposed scheme.

To begin with, we firstly investigate the resonance characteristics of a typical folded DSIR by simulations. The geometrical layout of the DSIR etched on a 1.0 mm thick F4B substrate with relative dielectric constant $\varepsilon_r = 2.65$ and loss tangent $\tan\delta = 0.003$ is given in Figure 2(a). The full-wave electromagnetic simulations are performed to analyze the reflection response of the DSIR. Supposing that all other parameters are kept unchanged, Figure 2(b) plots the simulated reflection coefficients when the length L is increased from 1.5 to 5.5 mm, and accordingly we can find apparently that the resonant frequency of the DSIR is decreased from 4.1 to 3.0 GHz. In theory, other parameters can also be tuned to attain desired resonant frequency, but the simulation results are not shown here for brevity. To summarize, the channel passbands of the proposed diplex can be allocated flexibly under the assistance of the folded DSIRs. Thus, the detailed parameters of resonators for each channel BPF are initially determined as tabulated in Table 1.

Table 1. Detailed parameters of the DSIRs for each channel BPF (mm).

Parameter	a	b	w_1	w_2	g	L
BPF I	7.4	7.4	0.5	2.5	0.2	5.4
BPF II	7.4	5.4	0.5	1.5	0.4	2.9
BPF III	5.0	6.0	0.5	1.0	0.4	2.7
BPF IV	5.0	5.0	0.5	1.0	0.4	1.6

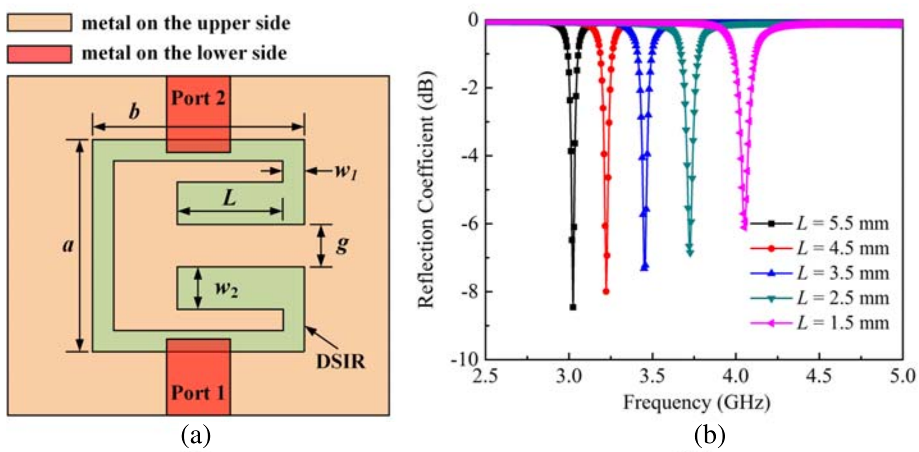


Figure 2. Resonance characteristic of the folded DSIR. (a) Geometrical layout. (b) Reflection coefficient. Other parameters are as follows: $a = 7.0$ mm, $b = 7.0$ mm, $w_1 = 0.5$ mm, $w_2 = 1.0$ mm, and $g = 1.0$ mm.

The specification of the proposed quad-channel diplexer is set as the corresponding 3-dB fractional bandwidths of BPF I–BPF IV are 10.0%, 6.2%, 7.0%, and 5.0%. For 20 dB passband return loss Chebyshev response, the required coupling coefficients (M_{ij}) and external quality factors (Q_e) are $M_{12} = M_{34} = 0.091$, $M_{23} = 0.07$, and $Q_e = 9.33$ at 2.45 GHz, $M_{12} = M_{34} = 0.056$, $M_{23} = 0.043$, and $Q_e = 15.05$ at 4.2 GHz, $M_{12} = M_{34} = 0.064$, $M_{23} = 0.049$, and $Q_e = 13.33$ at 3.5 GHz, and $M_{12} = M_{34} = 0.046$, $M_{23} = 0.035$, and $Q_e = 18.66$ at 5.2 GHz. To obtain the required input external quality factors and minimize the channel interaction concurrently, the locations of the first DSIRs for each channel along the common input feeding line should be optimized carefully, as illustrated in Figure 3. The length of the input feeding line is pre-determined as $L_4 = 42$ mm. In our proposed design, the group delay method is used to roughly estimate the external quality factor, which can be written as [17]:

$$Q_e = \frac{\pi f_0 \tau}{2} \tag{1}$$

where f_0 indicates the resonant frequency, and τ indicates the group delay. The group delay that varies with different inserted distances (D_1, D_2, D_3, and D_4) and positions (L_1, L_2, and L_3) can then be extracted from the full-wave electromagnetic simulations. Figure 4 compares the final simulated and

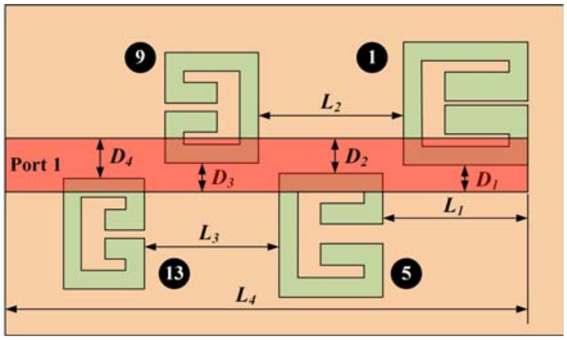


Figure 3. Locations of the first DSIRs of each channel along the common input feeding line.

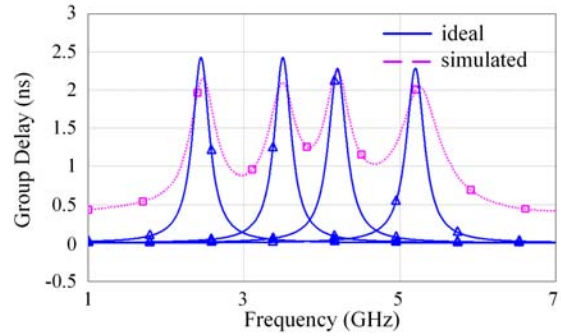


Figure 4. Comparison between the ideal and simulated group delays.

ideal group delays. Good alignment can be apparently seen. Here, we should note that the ideal group delay has been obtained using the simulation results of the equivalent lumped circuit performed by the ADS simulator. The reason that the simulated group delay is smaller than the ideal one is that the coupling of the three-dimensional electromagnetic model in the Ansoft HFSS is larger than that of the equivalent lumped circuit model used in the ADS simulator. Resultantly, in accordance to the group delays at the common input port, i.e., Port 1, the locations of the first DSIRs for BPF I–BPF IV can be determined sequentially.

Once the input external quality factors are obtained, the other DSIRs of the proposed diplexer can be determined readily based on the classical filter design theory [17]. Using the full-wave electromagnetic simulations, the coupling coefficients can be estimated as:

$$M_{ij} = \frac{f_H^2 - f_L^2}{f_H^2 + f_L^2} \tag{2}$$

where f_H and f_L indicate the higher and lower resonant frequencies of the two coupled DSIRs with respect to f_0. Furthermore, the output external quality factors of each channel can also be determined similarly according to the group delay method. Figure 5 presents the final layout of the proposed three-port quad-channel diplexer together with detailed optimal parameters. We should point out that the lengths of the output microstrip feeding lines for Port2 and Port 3 are 53 mm and 58 mm, respectively.

3. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 6 presents photographs of the fabricated quad-channel diplexer. The simulated and measured transmission and reflection characteristics are depicted in Figure 7. Simulations and measurements have a good agreement. The measured center frequencies of the four passbands are 2.45 GHz, 3.5 GHz, 4.24 GHz, and 5.22 GHz with measured insertion losses of 0.22 dB, 0.3 dB, 1.32 dB, and 2.12 dB, respectively. Besides, the corresponding measured 3 dB fractional bandwidths are 12.5%, 7.2%, 6.4%, and 5%, respectively. As can be observed in Figure 7(b), the measured return losses for all channels are greater than 12 dB within respective passbands. Differences between the measured and simulated results are probably due to fabrication errors, radiation loss, as well as the influence of SMA connectors. Figure 8 presents the simulated and measured isolations between the two output ports. It can be clearly seen that the measured isolation is maintained above 33 dB amongst different channels. The diplexer has an overall size around $0.88\lambda_g \times 1.02\lambda_g$, where λ_g indicates the guided wavelength at the lowest center frequency.

The performance of the proposed quad-channel diplexer has been compared with the previously reported ones, as summarized in Table 2. It can be seen that the proposed diplexer possesses the largest channel isolation. In comparison with the diplexers based on second-order BPFs using microstrip SIRs [10, 11] and DSIRs or slotline SIRs [15, 18], the proposed diplexer utilizing fourth-order BPFs has a larger circuit size as expected.

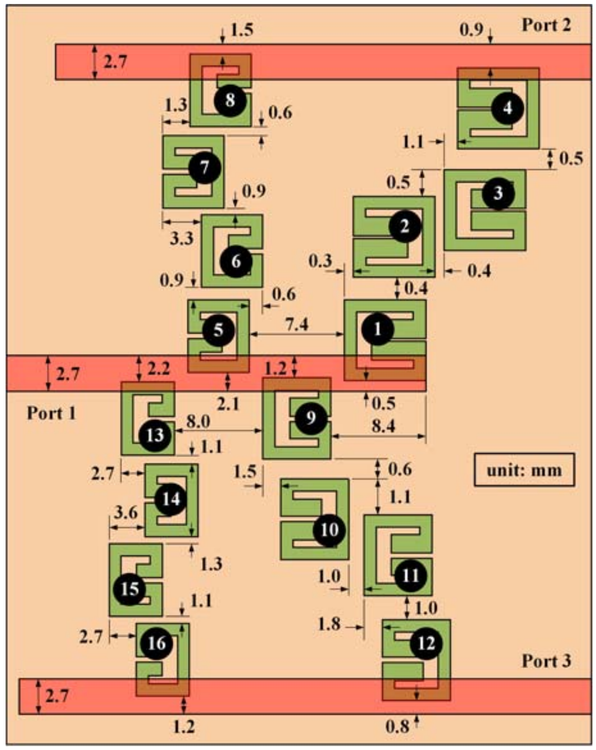
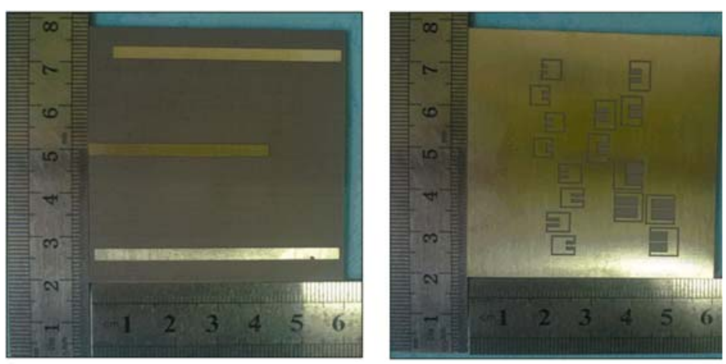


Figure 5. Schematic layout of the proposed three-port quad-channel diplexer.



(a) (b)

Figure 6. Photograph of the fabricated diplexer. (a) Top view. (b) Bottom view.

Table 2. Performance comparison between the proposed diplexer and previous similar ones.

Ref.	L/C	Filter order	Passbands (GHz)	Isolation (dB)	Circuit size ($\lambda_g \times \lambda_g$)
[10]	2/4	2	1.5/2.0/2.4/3.5	> 30	0.19×0.40
[11]	2/4	2	0.9/1.5/2.4/3.5	> 29	0.23×0.18
[15]	2/2	2	1.8/2.45	> 25	0.42×0.38
[18]	4/4	2	1.9/2.5/1.8/2.7	> 26	0.35×0.41
This work	**2/4**	**4**	**2.45/3.5/4.2/5.2**	$> \mathbf{33}$	$\mathbf{0.88} \times \mathbf{1.02}$

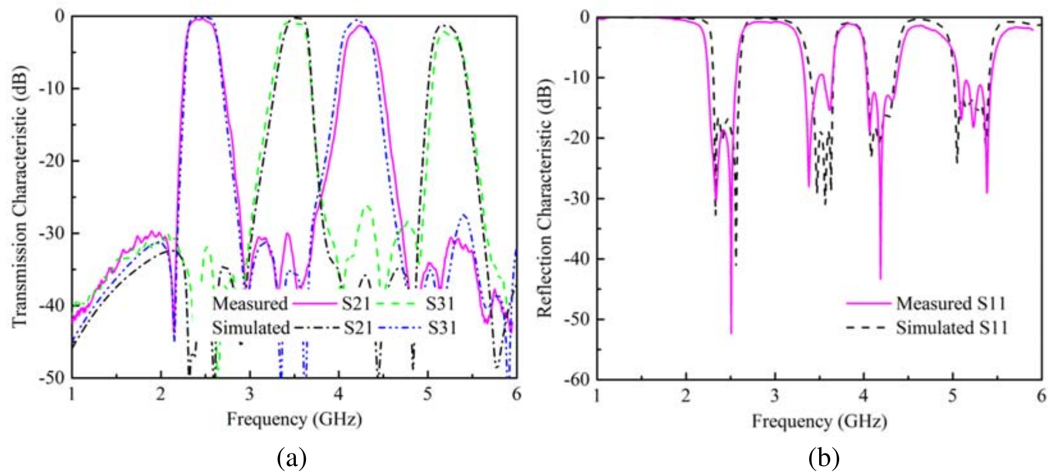


Figure 7. Simulated and measured results of the diplexer. (a) Transmission characteristic. (b) Reflection characteristic.

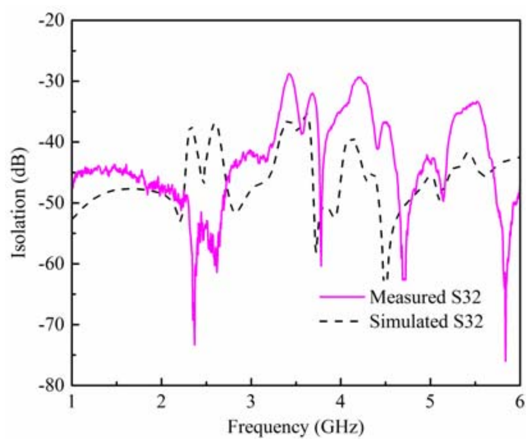


Figure 8. Simulated and measured isolation between the two output ports of the diplexer.

4. CONCLUSION

A novel compact three-port quad-channel diplexer is proposed in this paper with low insertion loss and high isolation. The diplexer is implemented based on sixteen folded DSIRs. By using the distributed coupling technique possessing small loading effect, the diplexer avoids extra impedance matching networks and time-consuming design and optimization procedures. The measured results of a fabricated prototype demonstrate the proposed diplexer. Therefore, it is suited for modern multi-standard and multi-service wireless communication applications. In addition, the proposed diplexer can be conveniently transplanted to other frequency bands and expanded to enclose even more channels.

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