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Chip-Package Co-Design for Optimization of 5.8 GHz LNA Performance Based on Embedded Inductors

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Abstract—This paper presents the design and demonstration of an optimized land grid array (LGA) structure for low noise amplifier (LNA). In order to achieve better circuit performance, the novel chip-package co-design method based on embedded inductors is used. The optimized structure is accurately modeled by ANSYS software. S-parameter is utilized to help in understanding the contributing to the optimized LGA structure. The simulation results for the novel LNA co-design structure show the gain 14.35 dB (> 10 dB), input reflection coefficient −15.63 dB (< −10 dB), output reflection coefficient −24.43 dB (< −10 dB), reverse-isolation −44.7 dB (< −20 dB), and noise figure 2.99 dB (< 4 dB), and indicate that the optimized LGA structure based on embedded inductors is fully capable of supporting 5.8 GHz LNA application.

1. INTRODUCTION

With the continuous development of information technology, the demand for low cost and high performance communication systems is increasing. In most RF circuit blocks, low noise amplifiers are usually designed as a single-port circuit for connecting with the band-pass filter or antenna [1, 2]. In order to achieve an efficient input power matching, many on-chip inductors are used in LNA design. These on-chip inductors, implemented in Complementary Metal Oxide Semiconductor transistor (CMOS) technology, not only consume high silicon area, but also have poor electrical performances [3], such as low quality factors. On the other hand, as the operating frequency or bandwidth increases for high data rate, the LNAs become more susceptible to package effects. Those package parasitic effects will cause significant degradation in gain and impedance of LNAs [4]. In previous works, the conventional ceramic quad flat no-lead (QFN) package is usually used for LNA design to satisfy high-performance [5, 6]. The low-pass filter models are used for wire bond packaged LNAs to reveal the package input/output interconnect behave and like an impedance transformer in altering the matching network for optimization design.

In this paper, a chip-package co-design of 5.8 GHz cascade common-source LNA based on embedded inductors is presented. In view of electrical performance design, the matching networks on the package substrate by using embedded inductor are constructed. Designing embedded inductor elements can reduce the number of passive elements and achieve special matching values. In Section 2, a special cascade common-source LNA chip with an on-chip matching network and its performance is discussed in detail. Then, the embedded inductor on the LGA substrate is built and analyzed in Section 3. By taking advantage of the packaging parasitic of bond wire, the LNA co-design architecture is established and optimized in Sections 4–5. Finally, a brief conclusion is given in Section 6.

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2. ON-CHIP MATCHED LNA AND ITS PERFORMANCE

2.1. LNA

Commercially available CMOS 0.18 µm technology, used in this paper, is optimized for high frequency LNA applications. Figure 1 shows the on-chip matched cascode CMOS LNA and its layout. As shown in Figure 1(a), the inductors L_1, L_2 and gate-source capacitance C_{gs} of the transistor M_2 are employed for the input matching network, while the inductor L_4 and capacitor C_4 serve as an output matching network. The LNA is biased to 1.8 V DC voltage and driven from a 50 ohm single ended port. Figure 1(b) shows the layout of the CMOS LNA, where the core part is located in the center, with the large-area matching inductors around the side. Including the bond pads, the die size is $1.13 * 1.1\,\text{mm}^2$.

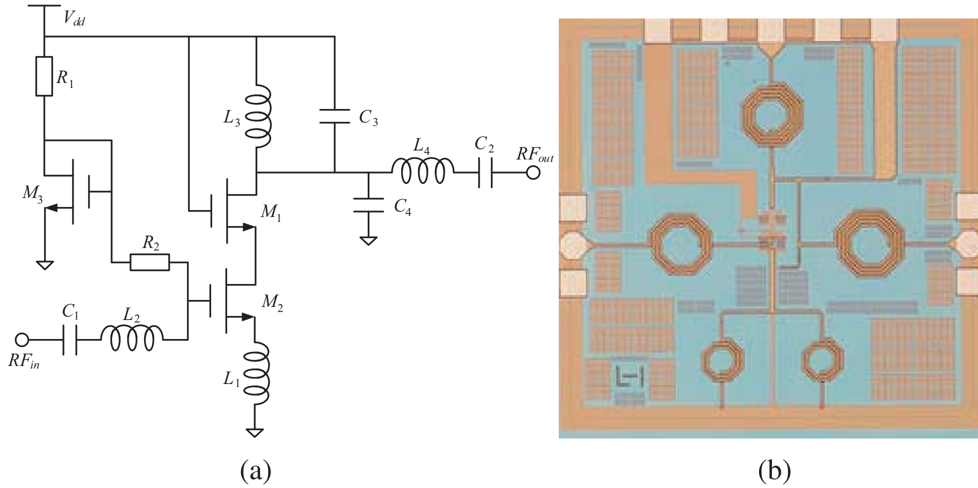

Figure 1. The cascode CMOS LNA: (a) circuit schematic, (b) layout.

Table 1. LNA circuit parameters.

Name	Parameter
V_{dd}	1.8 V
R_1	Length = 10 µm Width = 2 µm
R_2	Length = 2 µm Width = 13 µm
L_1	Inner Radius = 48 µm Turns = 2.14 Multiplier = 2
L_2	Inner Radius = 46 µm Turns = 3.8 Multiplier = 1
L_3	Inner Radius = 39 µm Turns = 4.5 Multiplier = 1
L_4	Inner Radius = 77 µm Turns = 4.5 Multiplier = 1
C_1	100 µF
C_2	100 µF
C_3	Width = Length = 8 µm
C_4	Width = Length = 9.4 µm
M_3	Width = 2.5 µm Length = 180 nm Fingers = 8
M_2	Width = 2.5 µm Length = 180 nm Fingers = 24 Multiplier = 2
M_1	Width = 2.5 µm Length = 180 nm Fingers = 24 Multiplier = 2

2.2. LNA Circuit Parameters and Analysis

The parameters of the cascode CMOS LNA in Figure 1 are shown in Table 1. In Linear Network Analysis, the sweep frequency is chosen from 10 MHz to 8 GHz, and the step size is set as 10 MHz. In order to evaluate the design performance, the magnitudes of −10 dB, 10 dB, −20 dB, −10 dB, 4 dB are considered as criterions for the input reflection coefficient S_{11}, gain S_{21}, reverse-isolation S_{12}, output reflection coefficient S_{22} and noise figure NF, respectively. Figure 2 gives the post-simulation results, which show that S_{21}, $|S_{12}|$, S_{11}, S_{22} and NF are 15.29 dB, 31.23 dB, −13.06 dB, −19.76 dB and 3.13 dB. All the results satisfy the design criterions.

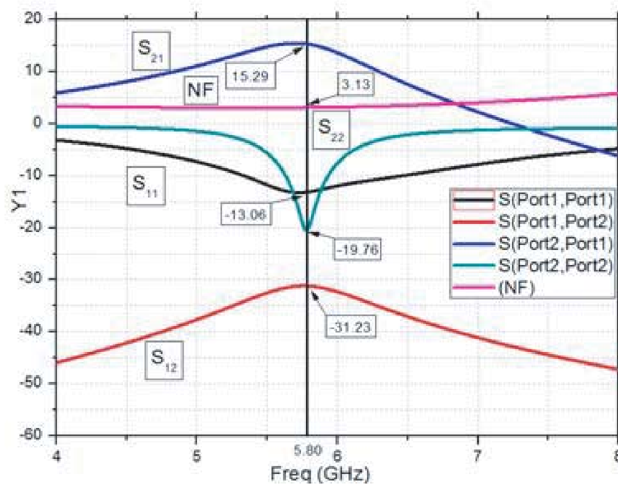

Figure 2. On-chip LNA circuit simulation results.

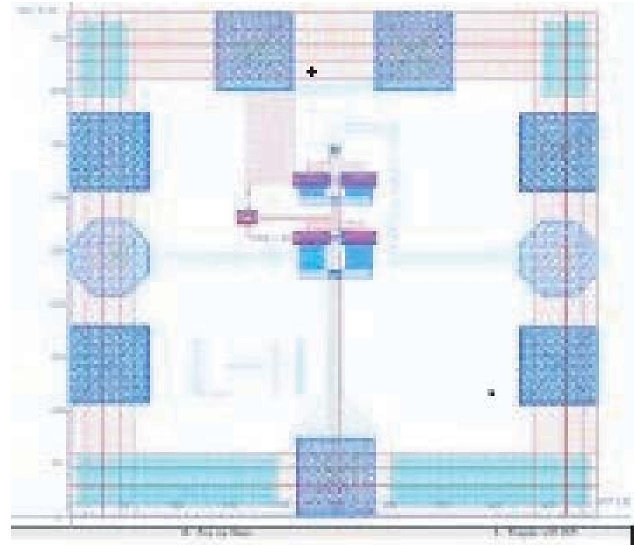

Figure 3. The layout without on-chip inductors.

3. DESIGN AND ANALYSIS EMBEDDED INDUCTOR

3.1. The Layout without Inductors

In order to reduce the silicon area for low cost and perform chip-package co-design, the on-chip input and output matching networks are removed. These matching networks will be designed by using embedded inductor elements on the LGA substrate. Figure 3 shows the unmatched LNA layout, and the die size is reduced from $1.13 * 1.1\,\text{mm}^2$ to $0.497 * 0.473\,\text{mm}^2$. Compared with the structure shown in Figure 1(b), the area is reduced by 81%.

3.2. Stand-Alone Inductor Structure

The inductors can be generally divided into surface mount technology (SMT) inductor, embedded inductor and bond-wire inductor. The embedded inductor is preferred over the other types of inductors because of its high integration and ease of customizing special inductance values [7]. In this paper, the structure of embedded inductor is shown in Figure 4, which has the simplicity of configuration. In this structure, the magnetic field generated by adjacent lines changes the current distribution of the wire. If spaces between traces are reduced, the magnetic field will be stronger, and the current density in the metal lines will be more asymmetric.

The inductance value and quality factor are related with the width of metal line (w), space between traces (s), number of turns (N) and inner diameter (d_{in}). These dimensions of spiral inductors are listed in Table 2.

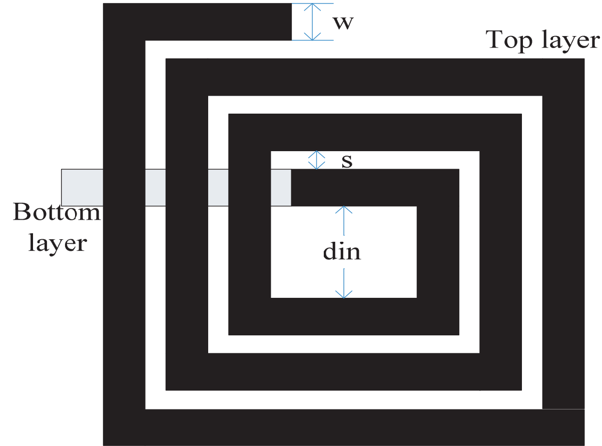

Figure 4. Structure of square spiral inductor.

Table 2. Parameters of embedded inductor.

Name	Parameter
w	50 µm
s	30 µm
d_{in}	90 µm
n	3
d_{out}	510 µm
d_{avg}	300 µm

The formula that is valid for planar spiral integrated inductors can be defined as [8]:

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{1}$$

where d_{avg} is the average diameter, $d_{avg} = 0.5(d_{in} + d_{out})$, and the fill ratio ρ is given by the formula $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$. The coefficients K_1 and K_2 are 2.34 and 2.75 [9, 10]. According to Table 2 and Equation (1), the calculated value of embedded inductor is 2.7143 nH.

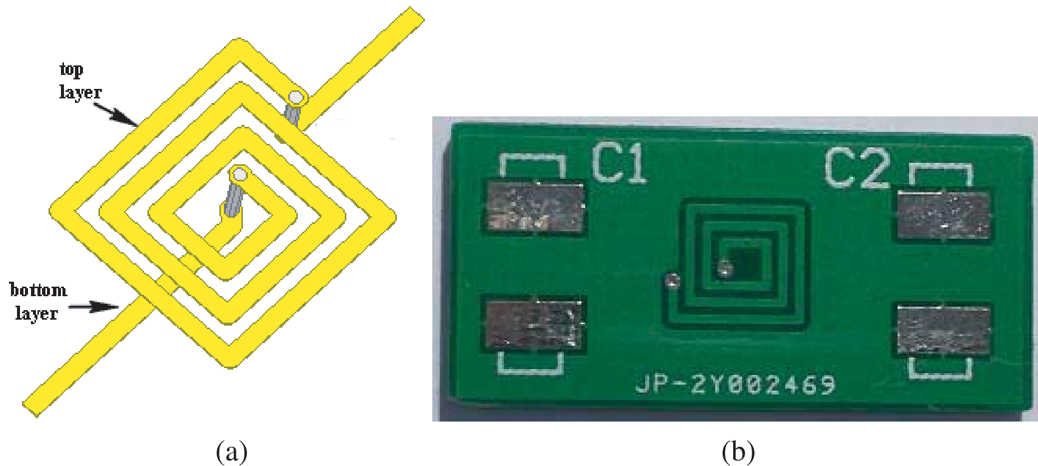

Figure 5. Embedded inductor: (a) 3D architecture, (b) manufactured footprint.

3.3. Modeling and Comparison with Field Solvers

To compare with calculated value, the scattering parameter (S) and admittance matrix (Y) can be obtained by ANSYS HFSS. By matrix Y, the inductance (L) and Q-factor (Q) can be obtained according to Equations (2) and (3), respectively.

$$L = \frac{im\left(\frac{1}{Y_{11}}\right)}{2\pi f} \tag{2}$$

$$Q = abs\left(\frac{im\left(\frac{1}{Y_{11}}\right)}{re\left(\frac{1}{Y_{11}}\right)}\right) \tag{3}$$

Based on Figure 4 and Table 2, the 3D architecture and manufactured footprint are given in

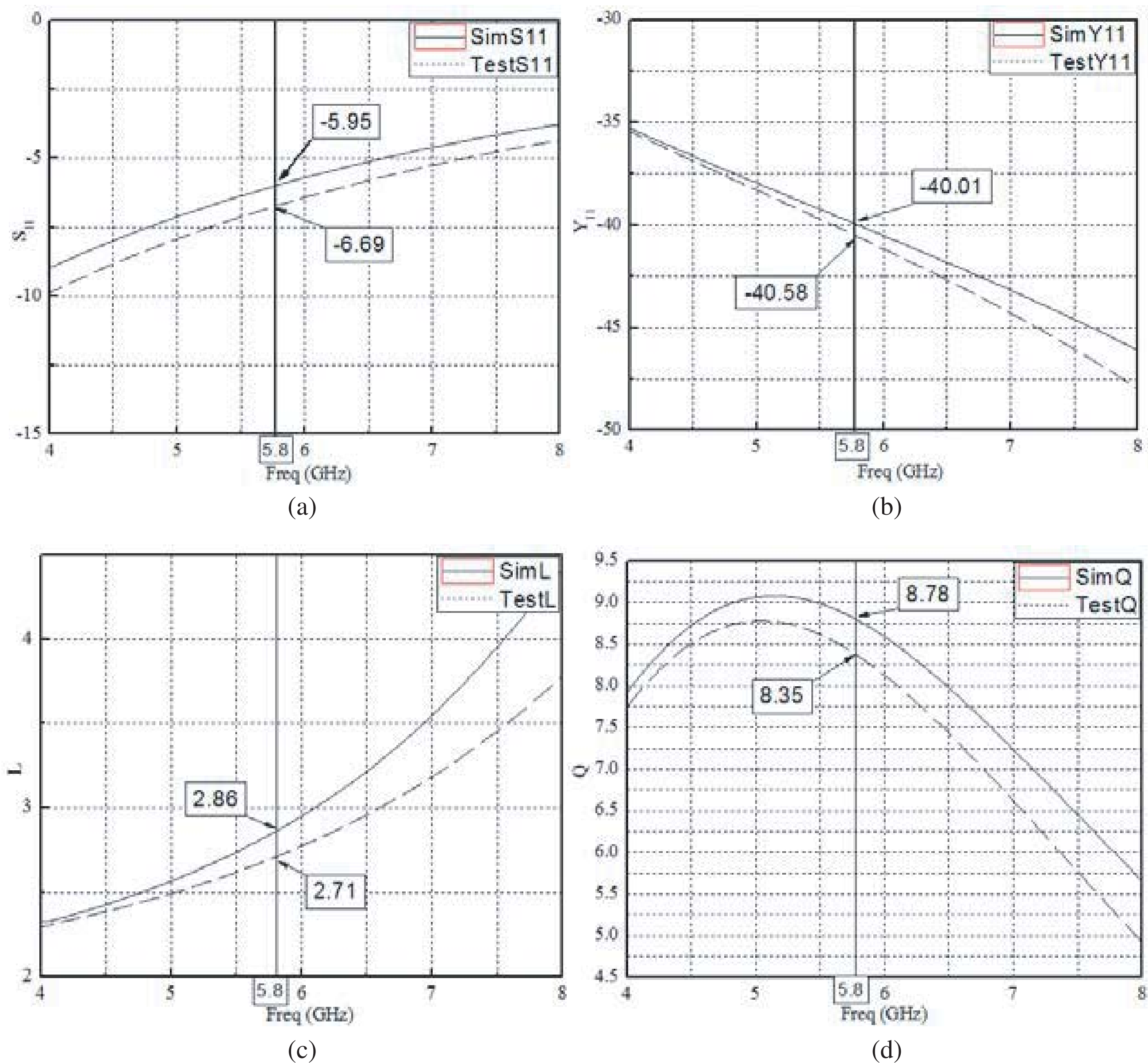

Figure 6. Simulation and test results: (a) S_{11}, (b) Y_{11}, (c) L, (d) Q.

Figure 5. The embedded inductor consists of 2 metal-layers with an FR4 dielectric and simulated by ANSYS HFSS.

Figure 6 gives the simulated results. To validate the simulated accuracy, Figure 6 also adds the test results. Figure 6(a) and Figure 6(b) depict the simulated results against measured data of s-parameters and y-parameters. It can be seen that the simulation and measurement results follow the same trends and show good agreements over the whole 4–8 GHz bandwidth. The bandwidth measured for S_{11} and Y_{11} is -6.69 dB (at 5.8 GHz) and -40.58 dB (at 5.8 GHz) from measured data. In Figure 6(c), at the point of 5.8 GHz, the value of simulation is 2.86 nH, and the test value is 2.71 nH. In Figure 6(d), the quality factor of simulation is 8.78, and the test is 8.35. The errors of the simulation results and test results are very small. Furthermore, compared with the calculated value 2.86 nH, the relative error between the simulated and calculated results is only 5.24%. The results indicate that the embedded inductor is fully capable of supporting 5.8 GHz LNA design.

4. CHIP-PACKAGE CO-DESIGN FOR MATCHING NETWORK

4.1. The 3D Co-Design Architecture Based on LGA Package

A commercial wire bond LGA package is adopted to perform the chip-package co-design. Figure 7 shows the proposed 3D co-design architecture based on LGA package. The LGA package size is $3.7 * 3.9\,\mathrm{mm}^2$ with two metal-layers. The unmatched CMOS LNA chip is epoxy-attached to the top layer. The whole model is composed of Source channel, RF input channel and RF output channel. Each inductance should be carefully designed to achieve a good impedance matching. Table 3 provides the prospective values for embedded inductors, which infer from the geometric parameters of on-chip inductors in Table 1.

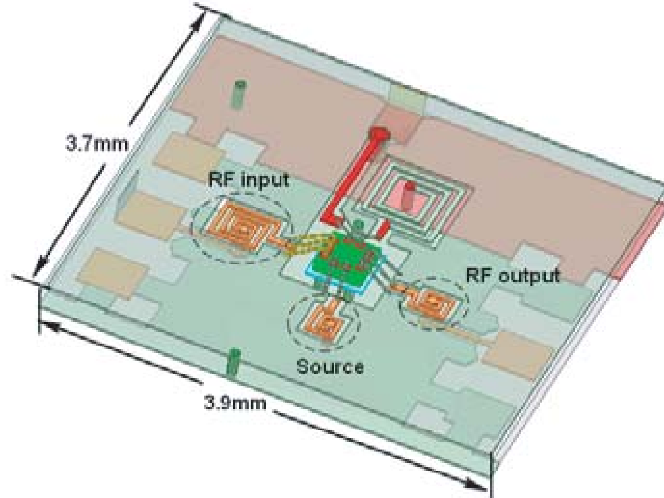

Figure 7. 3D co-design architecture based on LGA package.

Table 3. Geometric parameters of embedded inductors.

Name	Element	L (nH)	N	d_{in} (mm)	d_{out} (mm)
RF input	L_2	2	3	0.09	0.27
RF output	L_3	0.25	2	0.01	0.12
Source	L_4	0.06	2	0.006	0.012

The unmatched CMOS LNA pads are designed in a ground-signal-ground (GSG) configuration. The signal and ground pads of the LNA are bonded directly to the coplanar waveguide (CPW) line on the LGA substrate. The parameters of the CPW line are shown in Table 4. The LGA substrate also

has the shortest ground vias to connect the top and bottom layers in order to minimize the potential difference between the ground planes. The bond wire diameter is about 25 µm. For each wire, the horizontal distance between the first and second bonds is about 700 µm, with loop height of 125 µm and dies thickness of 300 µm. Some papers give the design of a wide-band interface by using bond wires and traces. In those papers, the bond wire is viewed as a high performance inductor applied to a matching network. In this paper, we first devote to developing a common design method of matching network by using embedded inductors while keeping the package parasitic as it is. So the bond wires are designed as short as possible for the smallest parasitic effects, and the main matching networks are designed by embedded inductors.

Table 4. LGA CPW parameters.

Parameter	Value
Type	Conductor-backed CPW
Dielectric constant	4.2
Dissipation factor	0.002 Tan
Substrate thickness	100 µm
Conductor thickness	10 µm
CPW line width	59 µm
CPW signal-ground gap	10 µm
Characteristic impedance	50 ohm

4.2. Extracted Parasitic Parameters

As shown in Figure 7, the RF input channel is composed by embedded inductor, via, trace, bond wire and LGA pad. The RF output channel and Source channel are also composed by them. These transition channels can be accurately modeled by a lumped T circuit to achieve a good impedance matching. Table 5 gives the extracted RLC parameters of RF input, RF output, and Source by ANSYS Q3D.

Table 5. Extracted RLC parameters.

Name	R (ohm)	L (nH)	C (pF)
RF input	1.44	2.35	0.15
RF output	0.74	1.12	0.11
Source	0.59	0.80	0.08

4.3. The Pre-Simulation Results of LNA

The chip-package co-design circuit topology is given in Figure 8. This topology includes one touchstone file of s-parameter and three lumped T circuits of RLC parameters: The touchstone file representing the unmatched CMOS LNA generated from Cadence Virtuoso Analog Design Environment (ADS) and three T circuits representing the parasitic effects from the LGA package modeled by using ANSYS Q3D. Each signal port is terminated to 50 ohm.

The simulation results are shown in Figure 9, where the gain S_{21}, reverse-isolation $|S_{12}|$, input reflection coefficient S_{11}, output reflection coefficient S_{22} and Noise figure NF are 3.03 dB, 44.76 dB, −6.03 dB, −22.46 dB and 3.97 dB, respectively. It is obvious that the input reflection coefficient S_{11} and gain S_{21} do not satisfy the design requirements ($S_{11} < -10$ dB, $S_{21} > 10$ dB).

According to the pre-simulation results, an optimized design method is performed to meet the requirements in the following section.

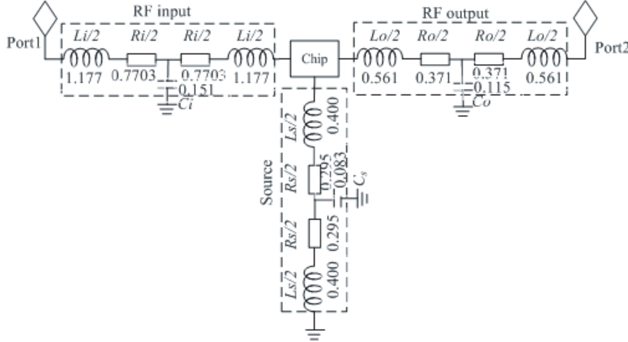

Figure 8. Circuit diagram of the LNA with interfaces.

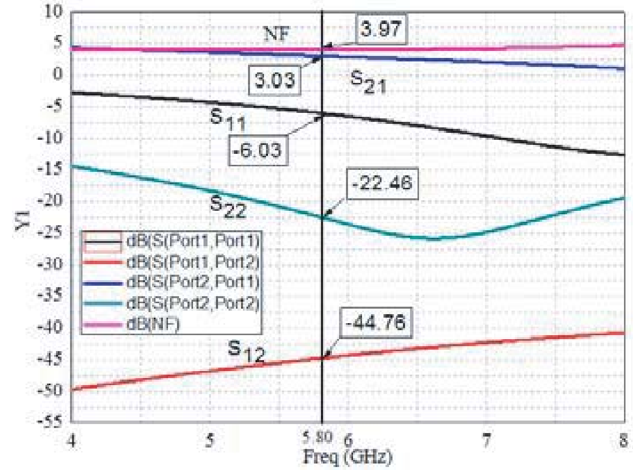

Figure 9. Pre-simulation results of LNA.

5. OPTIMIZATION CO-DESIGN OF LNA

5.1. Frequency Sweep

Impedance matching can be done by a handy calculation through a couple of equations [11]. However, by the assistance of frequency sweep, the impedance matching becomes easier. In Table 6, ten simulation configurations with different Li and Ls are conducted to find a better compromise between performance and robustness. Considering the importance of inductance for impedance matching, Li and Ls are focused on performing inductance parametric analysis while keeping the resistance (Ri, Rs) and capacitance (Ci, Cs) unchanged. Figure 10 gives the results of input reflection coefficient S_{11} and gain S_{21} from 5 GHz to 6 GHz. As we can see, the simulated results of Scenarios 3, 4, 5 and 6 measured for S_{11} and S_{21} satisfy the design criterions. In this paper, Scenario 5 with Li (3 nH) and Ls (0.1 nH) is preferred as the guide to improve the 3D architecture.

Figure 11 gives the simulation results by using the new values of Li (3 nH) and Ls (0.1 nH). The input reflection coefficient S_{11} is -17.09 dB, and the gain S_{21} is 14.26 dB at the frequency of 5.8 GHz, which satisfy the design criterions. Furthermore, the noise figure NF and output reflection coefficient S_{22} are lower than the previous results in Figure 9.

Table 6. Simulation configurations.

	RF input part			Source part		
Configuration	Ri	Ci	Li	Rs	Cs	Ls
Scenario 1	1.44	0.15	**2.2**	0.1	0.02	**0.02**
Scenario 2	1.44	0.15	**2.4**	0.1	0.02	**0.04**
Scenario 3	1.44	0.15	**2.6**	0.1	0.02	**0.06**
Scenario 4	1.44	0.15	**2.8**	0.1	0.02	**0.08**
Scenario 5	1.44	0.15	**3.0**	0.1	0.02	**0.10**
Scenario 6	1.44	0.15	**3.2**	0.1	0.02	**0.12**
Scenario 7	1.44	0.15	**3.4**	0.1	0.02	**0.14**
Scenario 8	1.44	0.15	**3.6**	0.1	0.02	**0.16**
Scenario 9	1.44	0.15	**3.8**	0.1	0.02	**0.18**
Scenario 10	1.44	0.15	**4.0**	0.1	0.02	**0.20**

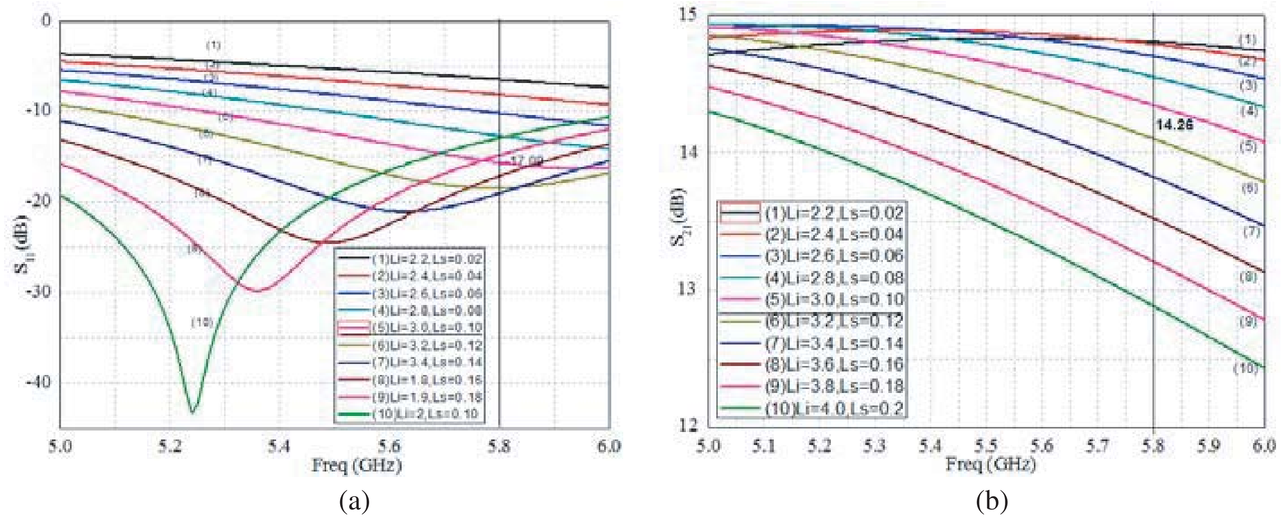

Figure 10. S-parameter sweep results: (a) input reflection coefficient S_{11}, (b) gain S_{21}.

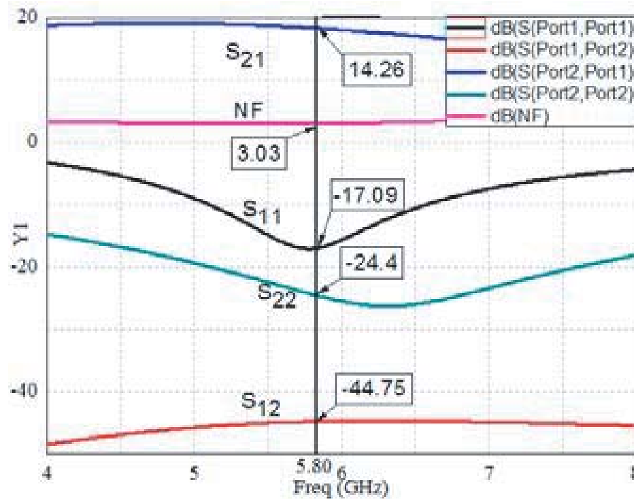

Figure 11. Optimized simulation results of LNA.

5.2. Rebuilding 3D Chip-Package Co-Design Architecture

An improved 3D architecture is rebuilt for LNA, as shown in Figure 12. Compared with Figure 7, N and d_{out} of the embedded inductance in RF input part are increased from 3 to 3.5 and from 0.27 mm to 0.32 mm, respectively. Due to the low inductance in RF output and Source part better for impedance matching, these two embedded inductors are replaced by bond wires and transmission lines, which have inherent parasitic inductors for impedance matching. Table 7 gives the extracted RLC parameters based on the improved 3D chip-package co-design architecture. Compared with Table 5, the full channel inductors of RF input part are increased from 2.35 nH to 3.08 nH, and the RF output and Source inductances are reduced to 0.71 nH and 0.09 nH. By rebuilding the circuit diagram in Figure 8 with the optimized RLC parameters in Table 7, the simulation results are shown in Figure 13. The gain S_{21}, reverse-isolation $|S_{12}|$, input reflection coefficient S_{11}, output reflection coefficient S_{22} and noise figure NF are 14.35 dB, 44.7 dB, -15.63 dB, -24.43 dB and 2.99 dB, respectively. Table 8 also gives the comparison between on-chip results and embedded inductors results. As we can see, all the optimized results satisfy the design criterions. It means that it is feasible to perform the chip-package co-design for 5.8 GHz LNA system.

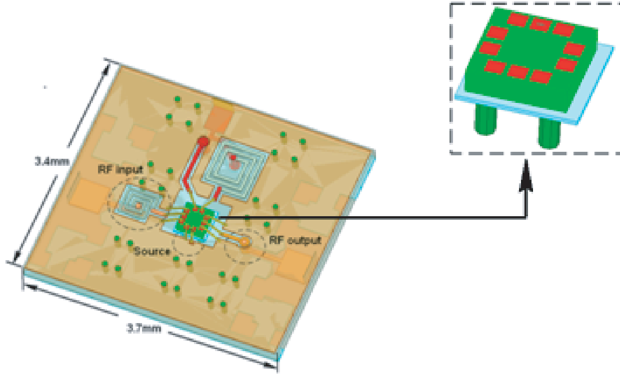

Figure 12. Optimized architecture based on LGA package.

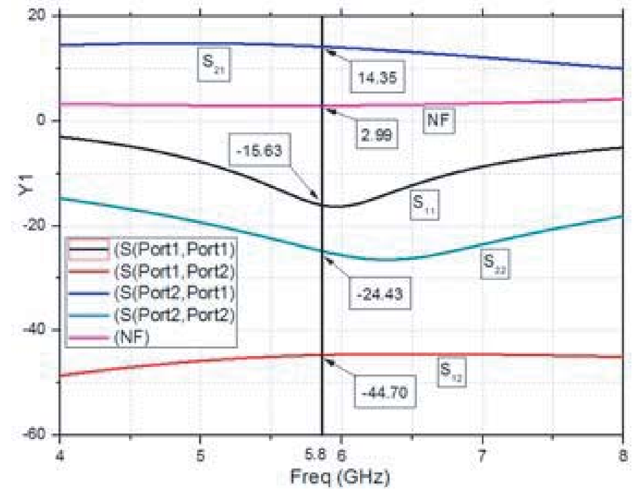

Figure 13. The results based on optimized structure.

Table 7. Optimized RLC parameters.

Name	R (ohm)	L (nH)	C (pF)
RF input	1.44	3.08	0.15
RF output	0.35	0.71	0.10
Source	0.01	0.09	0.02

Table 8. Performance comparison with on-chip results.

Version	On-chip	Embedded inductor
input reflection coefficient S_{11}	−19.76 dB	−15.63 dB
the gain S_{21}	15.29 dB	14.35 dB
reverse-isolation S_{12}	−31.23 dB	−44.70 dB
output reflection coefficient S_{22}	−19.76 dB	−24.43 dB
noise figure NF	3.13 dB	2.99 dB

6. CONCLUSION

The main aim of this paper is to analyze and model the LNAs matching networks with embedded inductors for better circuit assembly density and special matching values. After optimizing the 3D chip-package co-design architecture, the gain S_{21} and input reflection coefficient S_{11} are improved from 3.03 dB to 14.35 dB and from −6.03 dB to −15.63 dB, respectively. It can be concluded that the novel chip-package co-design technique based on embedded inductors is suitable for 5.8 GHz LNA applications.

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