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Design of Miniaturized Wilkinson Power Divider with Higher Order Harmonic Suppression for GSM Application

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Abstract—This paper presents a miniaturized Wilkinson power divider (WPD) with higher order harmonics suppression. The proposed power divider is designed for global system for mobile communication (GSM) application. The quarter wavelength lines of the conventional WPD are replaced by a stub loaded transmission line in order to miniaturize the circuit size. A solution, operating at 1.8 GHz center frequency, has shown that the 2nd and 3rd order harmonics are well suppressed by a level < -15 dB. Further, two differently shaped defected ground structures (DGS) are embedded with the design to suppress the higher order harmonics. Therefore, overall 31% size reduction is achieved, and higher order harmonics are suppressed up to the 9th order (16 GHz) by a level < -15 dB compared to reference WPD. The return loss and isolation performance of the proposed WPD are < -15 dB and < -20 dB, respectively.

1. INTRODUCTION

Federal Communications Commission (FCC) has reserved 1.8 GHz radio band exclusively for GSM application. So, it is necessary to design microwave components (filters, couplers and power dividers) with tight coupling and cost-effective components in that frequency band. Power dividers are used in many microwave subsystems, such as power amplifiers, mixers, frequency multipliers, and antenna array systems. To achieve equal power division in output ports, Wilkinson power divider (WPD) is widely used due to its simple design, impedance matching at all ports and high isolation between output ports [1, 2].

However, the circuit size of the power divider (PD) becomes specifically large at lower frequencies due to the structural dependence on the quarter wave length ($\lambda/4$) line that it incorporates. The nonlinear property of the active circuit in transceiver system caused unwanted harmonics at higher frequencies, which need to be removed to avoid the driving capability of a receiver for down-conversion and interference between other microwave signals. In order to address the above concerns, researchers have proposed several techniques to reduce the circuit area as well as harmonics suppression [3–21]. In [3], two open stubs are loaded at the middle of the quarter-wavelength branches of the power divider for the nth harmonics suppression. Although the harmonics are well suppressed, the cost of circuit becomes high. Researchers are also adopted different techniques such as parallel coupled-lines (PCLs) [4], coupled tapered compact microstrip resonator cell [5], hook-shaped resonators [6], and coupled line with open stub [7, 8] which have been used intentionally to significantly reduce the circuit size, but only a limited number of harmonics are suppressed. The pi (π) shape shunt-stub based artificial transmission lines are used to design a compact power divider comparable to conventional ones without harmonic suppression [9]. In order to achieve good attenuation in out of band performance, a low-pass filter in [10] and quasielliptic filter in [11] are used. The electromagnetic band-gap (EBG) structures and

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composite right-/left-handed (CRLH) transmission lines [12–15] are also used for miniaturization as well as harmonic suppression of power divider. In [13], an EBG cell is used to suppress the nth order harmonics with 30% miniaturization, while in [14], 39% size reduction is achieved with the 2nd and 3rd order harmonics suppression. Defected Ground Structure (DGS) is a popular technique [16] to remove spurious band response due to its electronic band gap property and to reduce overall circuit size due to slow wave effect. So, in the literature, many researchers have used the property of band rejection and slow-wave effect of the DGS to reduce size as well as suppress the harmonics simultaneously [17–20]. In [17], unequal power division is achieved using DGS in WPD and improves stopband characteristics of band-pass filter without increasing the circuit size [18]. In [20], an asymmetric spiral DGS is used to suppress the 2nd and 3rd order harmonics with 10% size reduction in WPD. However, EBG, CRLH transmission line, PCLs with DGS, symmetric DGSs, and asymmetric DGSs techniques are not capable of higher order harmonics suppression and size reduction simultaneously.

In this paper, the design and implementation of a miniaturized WPD with suppressed higher order harmonics up to the 9th order (16 GHz frequency for the presented design) is demonstrated. Firstly, a conventional WPD is designed at 1.8 GHz frequency. The conventional quarter wavelength lines of WPD are replaced by 'T'-shape stub loaded transmission lines to reduce the circuit size while ensuring harmonics suppression. Further, two different shape DGSs are used underneath the feed lines that provide additional band-stop characteristic at 7 GHz and 10 GHz frequencies, which results in higher order harmonics suppression. Finally, the proposed design is simulated using HFSS full wave EM simulator and fabricated on an Arlon substrate with dielectric constant $\varepsilon_r = 2.2$, thickness $h = 0.787$ mm and loss tangent 0.0009.

2. MINIATURIZATION OF WILKINSON POWER DIVIDER AND ITS HIGHER ORDER HARMONICS SUPPRESSION

2.1. Design of Wilkinson Power Divider (WPD)

Conventional WPD is a three-port structure that divides the input power in two equal parts while ensuring matching at each port connected to a specified load Za that is 50 Ω in our case as in the most conventional cases. The two input ports are connected by means of two quarter wavelength lines with a characteristic impedance $Zb = Za \times sqrt(2)$, in this case equal to 70.7 Ω. An isolation resistor with resistance $R = 2 \times Za$ is then connected between the output ports, in our case equal to 100 Ω [1]. The presence of the quarter wavelength line, in addition to impose its operative frequency with consequent bandwidth limitation, makes the size of this traditional structure dependent on the frequency, and the size of power divider becomes significantly large as wavelength increases. Concerning the considered technology, the practical design limitation is reached for frequencies below 2 GHz. Therefore, the selection of a topology that reduces the substrate area is important. In order to address the above concern, hexagonal shaped topology is selected for designing the WPD operating at 1.8 GHz frequency with return loss and isolation better than 20 dB. Fig. 1(a) shows the schematic diagram of WPD (Ref. design). The microstrip width and length corresponding to the characteristic impedances of the design are tabulated in Table 1. The simulated S-parameters responses are shown in Fig. 1(b), respectively. Fig. 1(b) shows equal output at the output ports (ports '2' & '3') which is -3.2 ± 0.1 dB with return loss and isolation performances < -30 dB at operating frequency 1.8 GHz.

Table 1. Design parameters of reference WPD.

Parameters	l_1	l_2	l_3	l_f	W_1	W_f	Area (W × L)
Value (mm)	11.1	13	8.6	8	1.4	2.4	$(39.6 \times 20.8) = 824\,\text{mm}^2$

2.2. Miniaturization of Wilkinson Power Divider Using Stub Loaded Transmission Line

In order to reduce the overall circuit area as well as harmonic suppression, quarter wavelength lines of Ref. power divider are replaced by stub loaded transmission lines. The equivalent transmission line

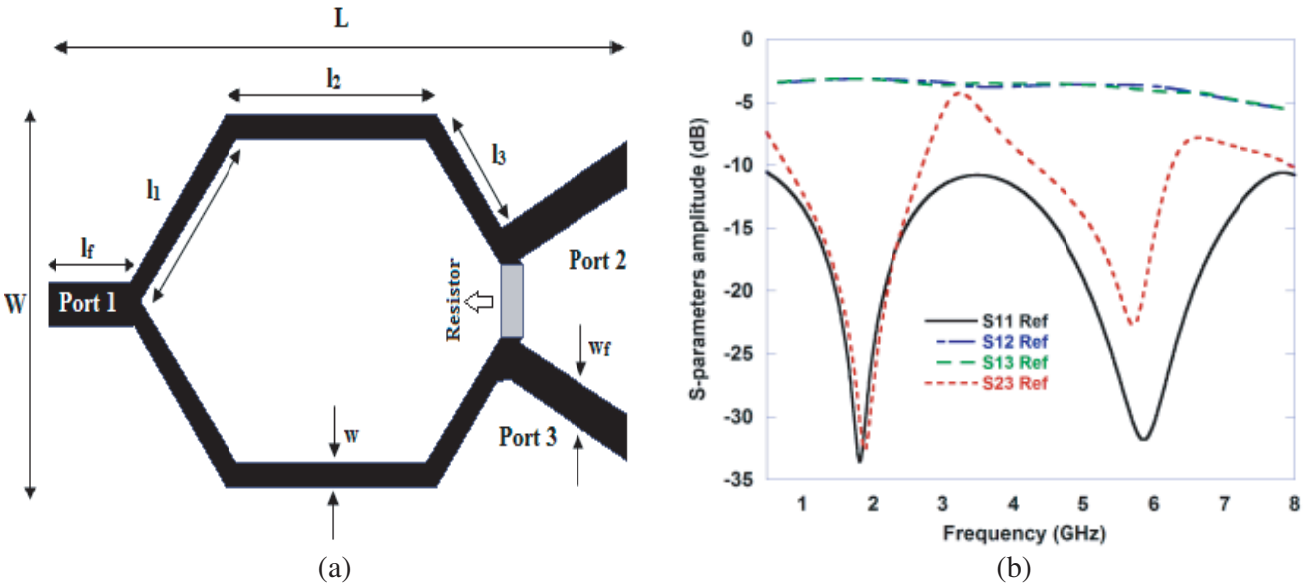


Figure 1. (a) Layout of Ref. WPD. (b) S-parameters of Ref. WPD.

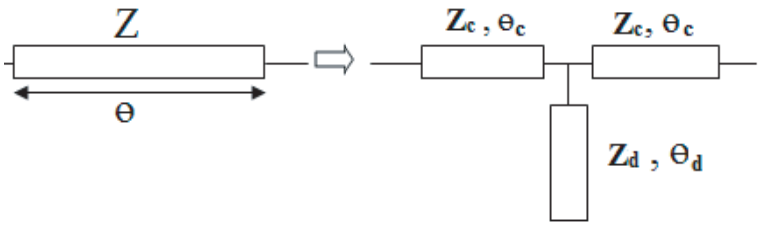


Figure 2. Equivalent model of single TL as stub loaded TL.

model of a single transmission line can be replaced as a equivalent stub loaded transmission line model as shown in Fig. 2 [21].

$$Z_d = \frac{Z_c \tan\theta_d \tan 2\theta_c}{2} \tag{1}$$

$$Z_c = \frac{Z}{\tan\theta_c} \tag{2}$$

where Z, Z_c, and Z_d are the characteristic impedances of the conventional line and stub loaded line, respectively. Similarly, θ, θ_c, and θ_d are electrical lengths of the conventional line and stub loaded line. The overall transmission matrix of a stub loaded TL is equated with transmission matrix of conventional quarter wavelength line in order to obtain the characteristic impedances and electrical lengths of the stub loaded line. The characteristic impedances Z_c and Z_d of the stub loaded TL in terms of electrical lengths θ_c and θ_d are described in Eqs. (1)–(2) [21]. Fig. 3 shows the variation of Z_c and Z_d with θ_c for a fixed value of $\theta_d = 40°$, and $Z = 70.7\,\Omega$ using MATLAB simulation tool. It is evident from the figure that the characteristic impedance of the series line is increased, and the stub line is decreased with θ_c for a fixed value of θ_d.

In order to reduce the circuit area, quarter wavelength lines of Ref. power divider are replaced by stub loaded TLs as shown in Fig. 4(a), namely design '1'. In design '1', electrical lengths of the stub loaded TL, θ_c and θ_d, are chosen as 20° and 40°, respectively for significant size reduction and design simplicity. The characteristic impedances (Z_c & Z_d) are calculated from Eqs. (1)–(2) and found to be $Z_c = 102\,\Omega$ and $Z_d = 35\,\Omega$, where Z is $70.7\,\Omega$. The physical length of the open stub is bended in the form of 'L' and shaped in order to reduce the circuit area. The utilization of a stub loaded line as an

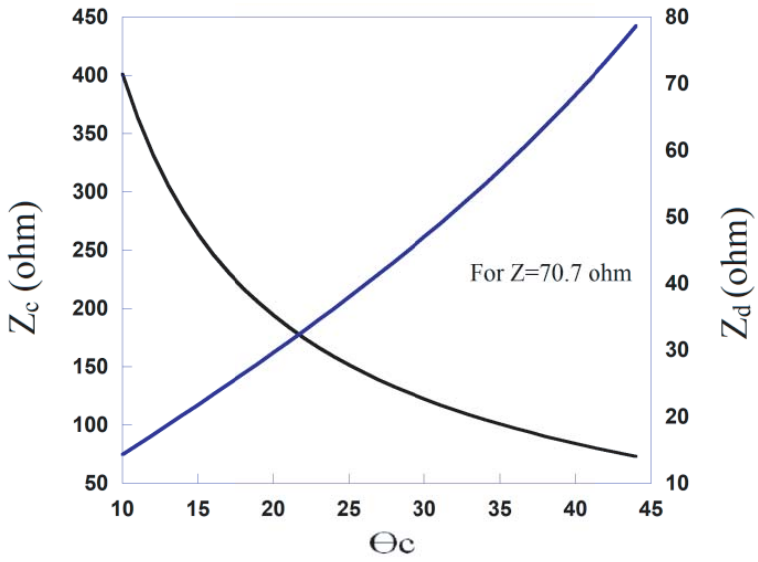
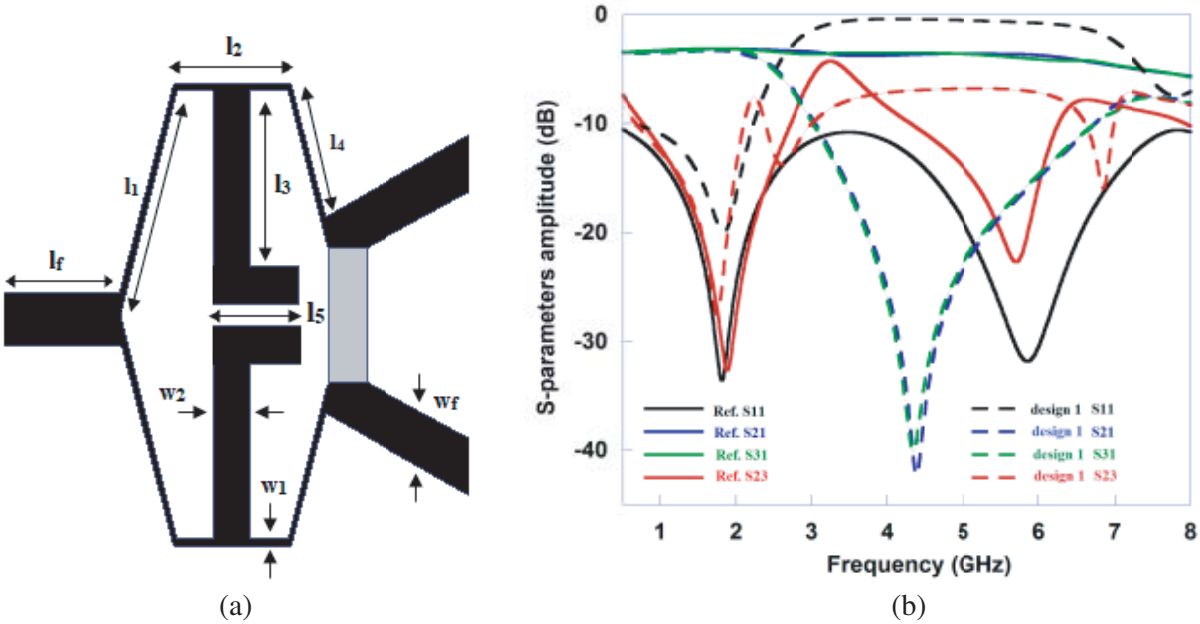


Figure 3. Impedance of series and shunt open stub of a proposed TL with θ_c, for $Z = 70.7$ ohm and $\theta_d = 40°$.

alternative of conventional line not only reduces the circuit size but also produces a transmission zero due to the open stub since it represents a quarter wavelength line at 4.35 GHz frequency. The optimized design parameters of design '1' are tabulated in Table 2. The S-parameter responses of design 1 are compared with the Ref. WPD in Fig. 4(b). From this figure it is clear that at the same frequency band the circuit of design 1 shows return loss and isolation less than −20 dB and −28 dB, respectively, in comparison with the Ref. WPD, whose return loss and isolation are higher than 30 dB. Another attractive feature of design 1 is the band-stop characteristic at 4.35 GHz that shows an attenuation level higher than 40 dB. As a result, unwanted harmonics are suppressed up to 6 GHz by 15 dB as shown in Fig. 4(b).



(a) (b)

Figure 4. (a) Layout. (b) Comparison of simulated S-parameter responses of design '1' with Ref. WPD.

Table 2. Dimension of power divider of design '1'.

Parameters	$\mathbf{l_1}$	$\mathbf{l_2}$	$\mathbf{l_3}$	$\mathbf{l_4}$	$\mathbf{l_5}$	$\mathbf{l_f}$	$\mathbf{w_1}$	$\mathbf{w_2}$	$\mathbf{w_f}$	**Area (W × L)**
Value (mm)	10	5	7.8	6	4	8	0.3	1.7	2.4	$(23.05 \times 20.6) = 474.8\,\text{mm}^2$

2.3. Higher Order Harmonics Suppression Using Defected Ground Structures (DGSs)

Defected ground structure (DGS) is a popular technique to reject frequency band by etching a uniform or nonuniform pattern over the ground metallic plane [16, 17] by implementing a resonant circuit. As a result, the current distribution is disturbed, and electrical path length is increased. Thus effective inductance and capacitance values vary accordingly. Metal incorporated strip ring resonator (MISRR) and dumbbell shaped DGSs are used in order to occupy less circuit area and suppress higher order harmonics. MISRR shaped DGS is considered in order to increase the electrical path length in a minimum space. The layout of the DGSs and their dimensions are shown in Figs. 5(a) & (b). These DGSs are placed underneath the signal line having characteristic impedance equal to $50\,\Omega$ and S-parameter responses shown in Figs. 6(a) & (b). The frequency characteristic of DGS is modeled as a parallel LC network, as shown in Fig. 7(a), and the values of inductance (L) and capacitor (C) evaluated by Eqs. 3(a) & 3(b) respectively [17]. Fig. 7(b) shows the transmission line model to determine the characteristic impedance of the line with DGS, where Z_0, Z_{in}, and Z_{DGS} are the output port impedance, input port impedance, and the impedance of line whose substrate has been implemented by using the DGS, respectively [16]. If the electrical length (θ) of the line with DGS is $\pi/2$ at the resonance frequency, the magnitude of the reflection coefficient (Γ) is maximized, and it can be calculated from S_{11} by (4). Once $|\Gamma|$ is known, Z_{in} is calculated by Eq. (5). Finally, the impedance of DGS embedded microstrip line is calculated from Eq. (6). However, the resonant feature of DGS is more invasive in terms of bandwidth reduction compared to MISRR solution, as can be observed in Fig. 6.

$$L = \frac{1}{4\pi^2 c f_0^2} \tag{3a}$$

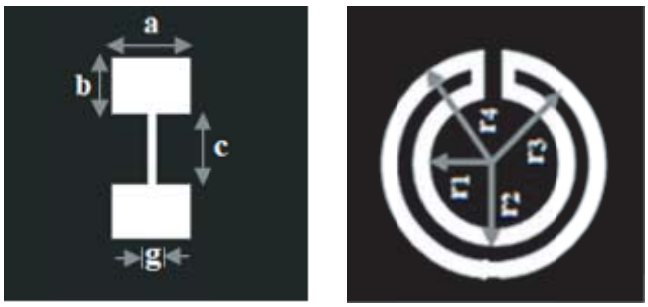
$$C = \frac{f_c}{4\pi Z_0 \left(f_0^2 - f_c^2\right)} \tag{3b}$$

$$S_{11}\,(\text{dB}) = 20\log|\Gamma| \tag{4}$$

$$Z_{in} = Z_0 \frac{1+|\Gamma|}{1-|\Gamma|} \tag{5}$$

$$Z_{DGS} = \sqrt{Z_{in} Z_0} \tag{6}$$

In order to achieve a higher order harmonic suppression, the proposed circuit has been equipped by inserting one dumbbell and two MISRR shaped DGSs, which are etched in the ground plane beneath



(a) (b)

Figure 5. Two DGS's. (a) Dumbbell shape (dimension in mm: $a = 2.5$, $b = 3.5$, $c = 2.4$, $g = 0.4$). (b) MISRR shape (Dimension in mm: $r_1 = 1.5$, $r_2 = 2$, $r_3 = 2.5$, $r_4 = 3$).

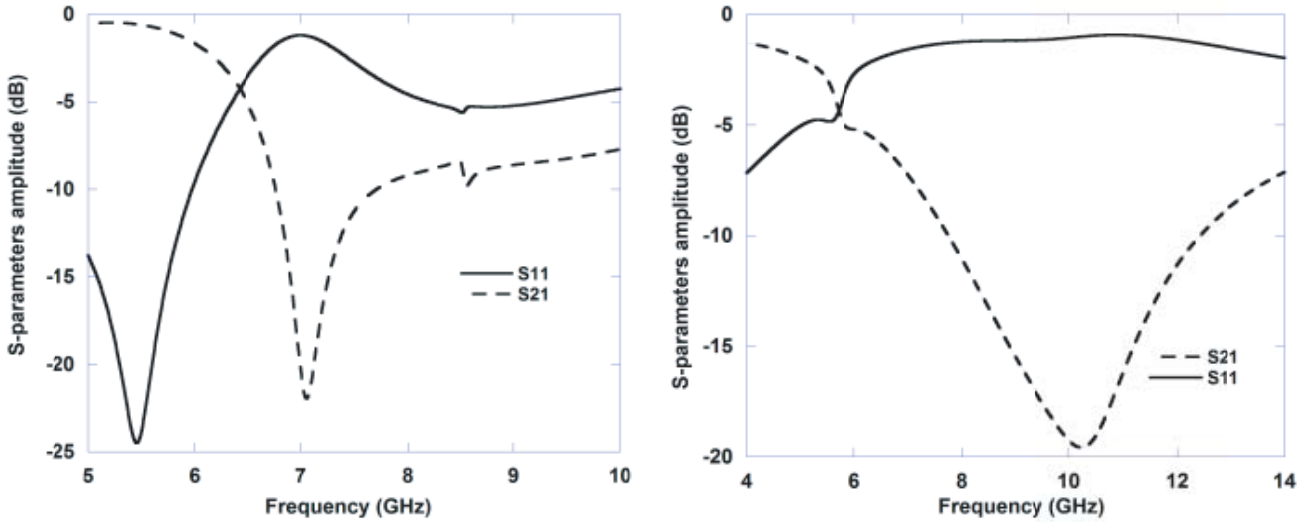


Figure 6. Transmission characteristic of DGS. (a) Dumbbell shaped. (b) MISRR shaped.

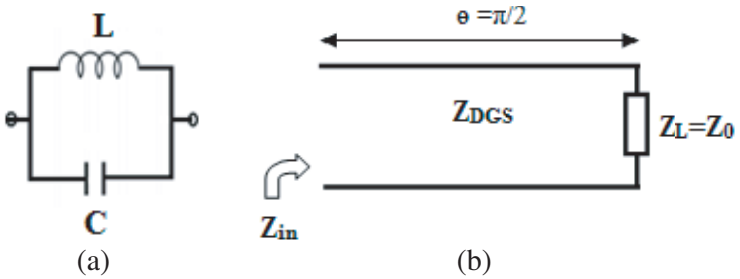


Figure 7. (a) Equivalent circuits of DGS. (b) Transmission line mode of signal line with DGS.

the input and output lines, respectively, and referred as design '2'. By placing the DGS underneath 50 Ω input and output lines, the impedance of the line changes due to the change in effective dielectric constant. In other words, the characteristic of any line with DGS changes the effective capacitance and inductance of the line by adding slot resistance, capacitance, and inductance. In order to improve impedance matching at the input and output ports after incorporating DGS, the widths of the input and output lines are modified to compensate the variation in the characteristic impedance of line with DGS using Eqs. (4)–(6). By adopting this strategy, the layout of the proposed WPD, hereinafter (design '2'), has been obtained as reported in Fig. 8(a). Optimized design parameters are tabulated in Table 3. By incorporating the DGSs into the circuit of design '1', 31% size reduction is achieved compared with the Ref. WPD. The most important feature of the proposed design is the suppression of the undesired higher order harmonics up to the 9th order (16 GHz). The simulated S-parameter responses of the proposed design are compared with the Ref. WPD as shown in Figs. 8(b)–(d). At the center operating frequency of 1.8 GHz, the simulated insertion loss between the output ports (port 2 and port 3) is 3.3 ± 0.2 dB, and the return loss and isolation are higher than 15 dB and 25 dB, respectively. From Fig. 8(c) it is clear that the unwanted harmonics are well suppressed by 15 dB up to the 9th order.

3. EXPERIMENTAL RESULTS

The proposed WPD has been designed, fabricated and measured. An Agilent vector network analyzer is used to test the performance of the fabricated power divider and compared with the simulated results. Photographs of the fabricated structure are shown in Fig. 9. The comparisons between simulated and

Table 3. Optimized designed parameters of proposed power divider.

Parameters	l_1	l_2	l_3	l_4	l_5	l_f	w_1	w_2	w_{fport1}	$w_{fport2,3}$	Area ($W \times L$)
Value (mm)	8.75	5	7.8	5	4	8	0.3	1.7	3.4	2.8	(31.5×18.1) $= 571\,\text{mm}^2$

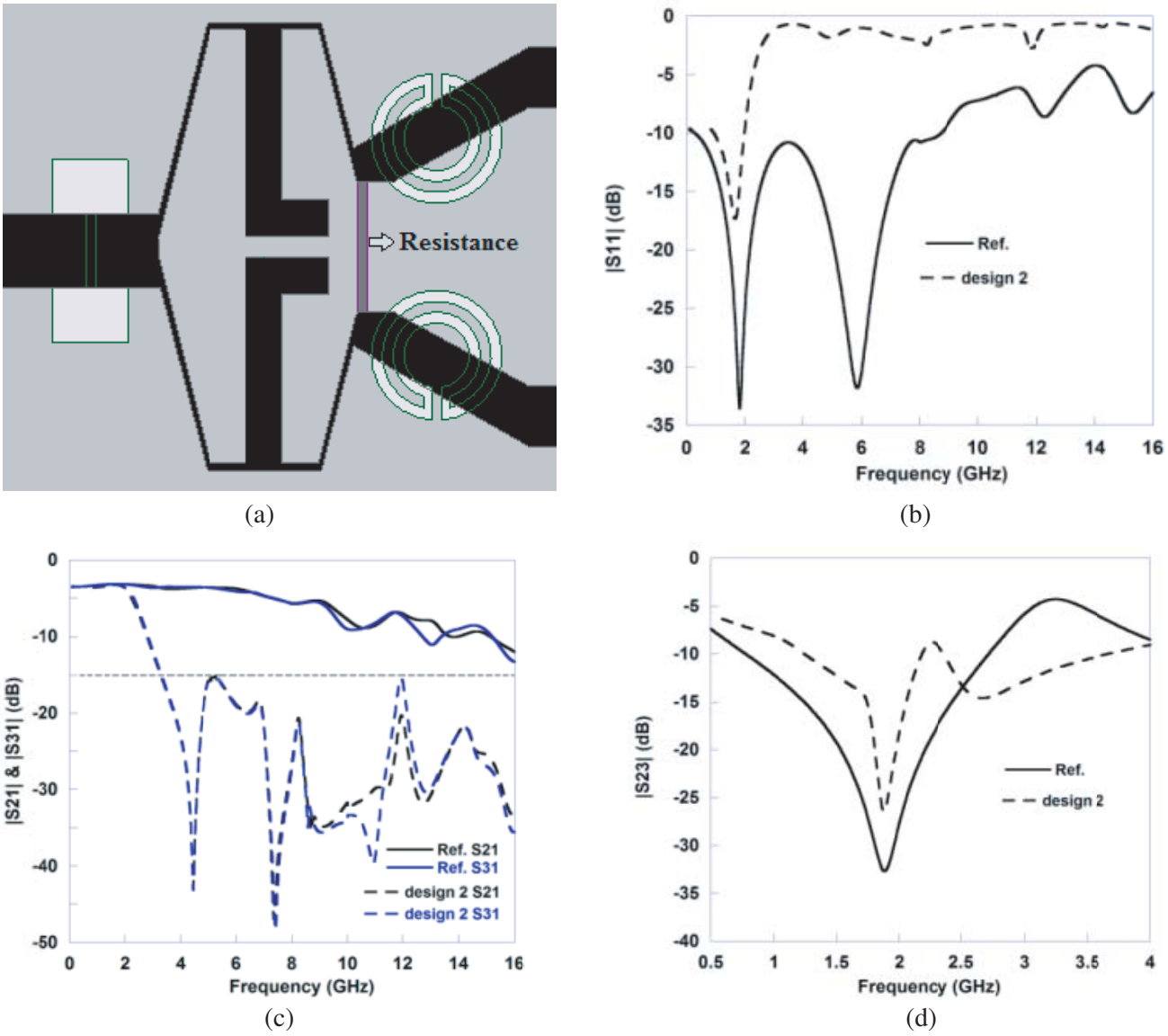
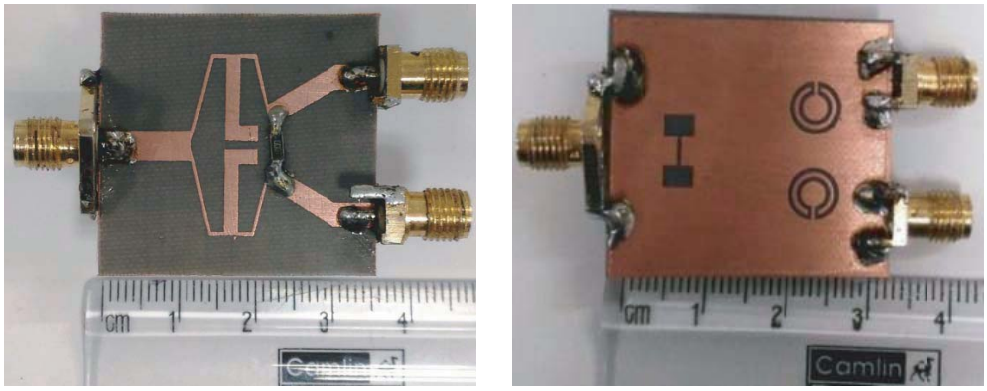


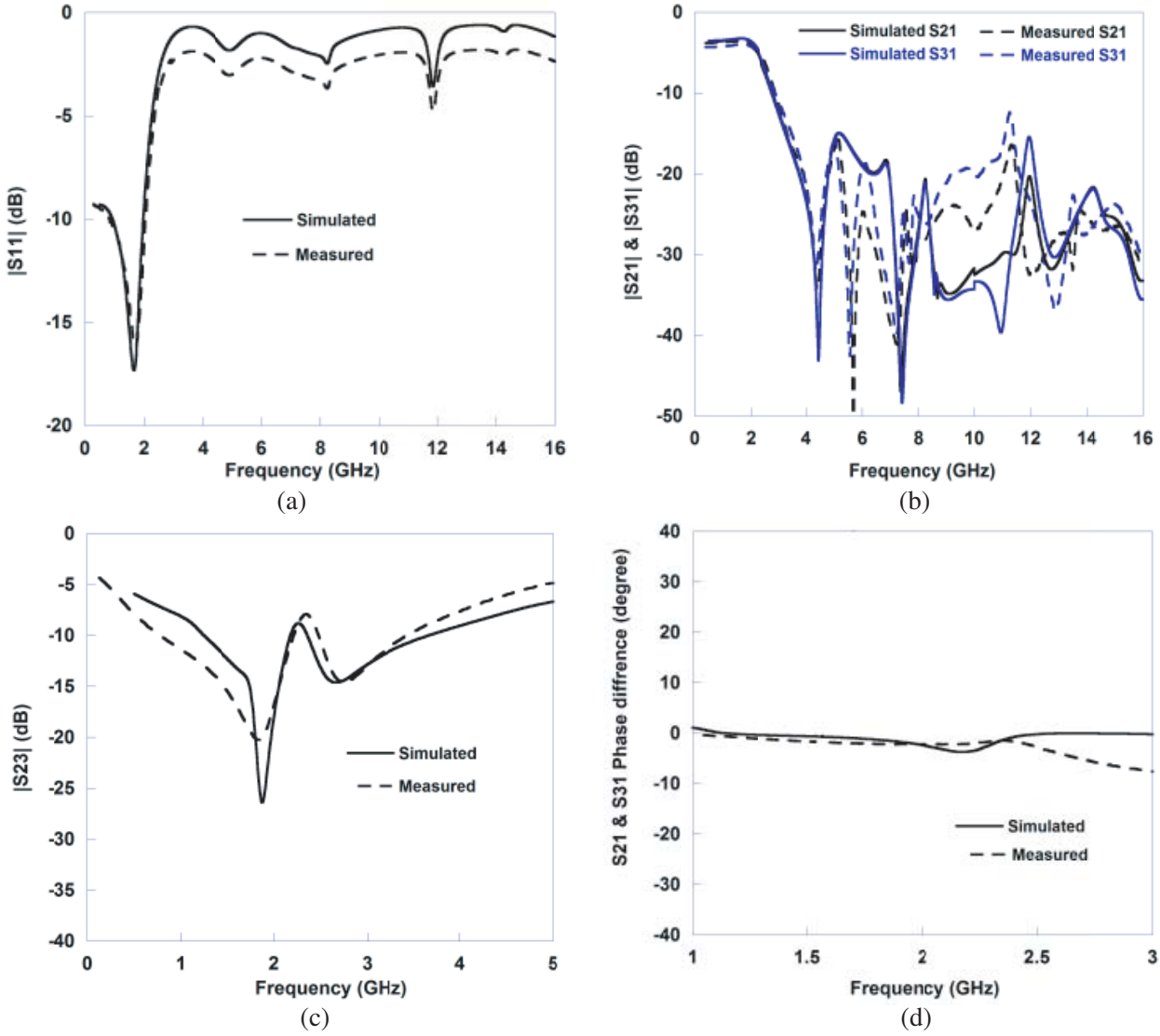
Figure 8. Comparisons of simulated frequency response of Ref. and proposed design 2. (a) Layout of design '2'. (b) $|S_{11}|$. (c) $|S_{21}|$ & $|S_{31}|$. (d) $|S_{23}|$.

measured responses are shown in Figs. 10(a)–(d). The measured circuit has shown an insertion loss at the output ports of 3.2 ± 0.1 dB for around 30% FBW with a return loss and isolation higher than 15 dB at the operating frequency. Table 4 illustrates the simulated and measured S-parameter details, FBW and phase difference (PD) of the proposed WPD. Table 5 shows the performance of the proposed WPD and the comparison with the existing one. The solution in [9] accounts for almost double of area reduction, but it suppresses the 2nd harmonic by almost 6 dB less than the proposed circuit. The



(a) (b)

Figure 9. Fabricated structure unit of proposed WPD. (a) Top. (b) Bottom.



(a) (b) (c) (d)

Figure 10. Comparisons of simulated and measured S-parameters response of proposed WPD. (a) $|S_{11}|$. (b) $|S_{21}|$ & $|S_{31}|$. (c) $|S_{23}|$. (d) Phase difference between output ports.

Table 4. Comparisons of S-parameters performance.

	$\|S_{21}\|$ dB	$\|S_{31}\|$ (dB)	$\|S_{23}\|$ (dB)	$\|S_{11}\|$ (dB)	FBW %	PD (degree)
Simulated	3.29	3.29	25	21.68	35	0.9
Measured	3.4	3.4	20	16	30	1.1

Table 5. Comparison between proposed WPD with existing ones.

[Ref.], Year	Area reduction (%)	Harmonic suppression (dB)							
		2nd	3rd	4th	5th	6th	7th	8th	9th
[20], 2005	10	18	15	-	-	-	-	-	-
[13], 2007	30	32.5	12	-	-	-	-	-	-
[14], 2008	39	26	25	-	-	-	-	-	-
[9], 2010	66	13	35	-	-	-	-	-	-
[11], 2011	-	-	46.2	-	37.35	-	-	-	-
[6], 2012	40	-	24	-	-	-	-	-	-
[5], 2013	29.3	-	53	25	56	20	-	-	-
[7], 2013	35	-	45	-	43	-	-	-	-
[8], 2014	20	43	49	37	-	-	-	-	-
[10], 2018	43	20.6	20.1	23.3	24.4	32.1	-	-	-
Design '1'	**42**	**18**	**19**	**-**	**-**	**-**	**-**	**-**	**-**
This work	**31**	**18.6**	**15.8**	**38**	**38.5**	**37.6**	**23**	**22.5**	**27**

proposed WPD is comparable in size to that in [13, 14], but it suppresses the unwanted harmonics up to the 9th order, while the harmonic suppression in [13, 14] is up to the 3rd order.

4. CONCLUSION

The feasibility of a miniaturized Wilkinson power divider with higher order harmonics suppression is demonstrated by means of an improved structure based on stub loaded transmission lines and a defected ground structure for GSM application. The overall size reduction of 31% is achieved at the operating frequency 1.8 GHz. Another attractive feature of the design includes the suppression of unwanted harmonics by a level < -15 dB up to the 9th order without much affecting the performance of Ref. WPD. The measured return loss and isolation performance is better than 15 dB at the operating frequency, and a comparison with the state of the art devices present in literature shows that the proposed solution gives a great tradeoff between size and performances. The proposed WPD design on planer printed circuit board with reduced circuit size and improved harmonic suppression, which is in great demand in microwave wireless communication systems.

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