

Broadband Vertical Transitions Between Double-Sided Parallel-Strip Line and Coplanar Waveguide

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Abstract—A pair of broadband double-sided parallel-strip line (DSPSL) to coplanar waveguide (CPW) vertical transitions are presented. The transitions are composed of CPW open end with connected grounds forming two strips of the DSPSL with single via connection. The connected grounds of CPW, which forms top strip of the DSPSL are of two different shapes resulting in two transitions (Types 1 & 2). Simulated results for the back-to-back transitions, using the multilayer solver of CST Microwave Studio, show good agreement with the measured ones.

1. INTRODUCTION

Vertical transitions are crucial components in double-layer microwave circuits to avoid the use of crossovers. DSPSL, also known as broadside coupled stripline (BCS), is a balanced transmission line, with wide range of characteristic impedances, differential signalling and simple transition structures [1]. However, no vertical transitions between DSPSL and CPW have been reported yet. Back to back vertical transitions of DSPSL in direct and inverted forms are capable of achieving signal/phase inversion, resulting in microwave applications such as mixers and ring couplers. Traditionally, vertical transitions will use either low-pass natured via connection or band-pass natured slot/cavity coupling.

Due to the wide popularity of CPW probe pads, various wideband transitions between CPW and DSPSL have been proposed in recent years [2–5]. Furthermore, majority of them are built on high dielectric-constant substrates for attaining low characteristic impedances thereby easy matching to $50\ \Omega$ lines. However, they are suitable for circuit design instead, and using such transitions to feed antennas will degrade the antenna performance [4]. The optimizations of planar transitions using different techniques have already been reported [10–13].

In this paper, a vertical broadband $50\ \Omega$ DSPSL to $50\ \Omega$ CPW transition is proposed for the first time. A simplified equivalent circuit revealing the basic low pass nature is introduced. The back-to-back transitions on a 1.524 mm thickness Rogers RO4003C substrate yield return and isolation losses better than 14.5 dB and 2.5 dB respectively, from DC to 11.5 GHz, and for 1.6 mm thickness FR4 substrate, the return and insertion losses better than 15.0 dB and 4.0 dB respectively, from DC to 11.0 GHz. It has an optimized structure with a single via, which can be easily fabricated.

2. DOUBLE-SIDED PARALLEL-STRIP LINE

The DSPSL is two identical metal strips separated by a dielectric slab. It possesses a wide range of characteristic impedance, which validates the feasibility in constructing new high performance

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microwave circuits and integrating with other microwave circuits/components without any impedance transformer. As per image theory, the middle plane of the dielectric slab is a virtual ground plane to form identical microstrip lines with half the substrate thickness ($h/2$) as shown in Fig. 1. The relationship of the characteristic impedances between them is

$$(Z_0)_{dspst} = 2 * (Z_0)_{microstrip}$$

For unbalanced transmission lines such as microstrip line and CPW, very high impedance is not available due to fabrication limitation. On the other hand, for the CPS and slot line, very low impedance is not available due to the small capacitance between the two strips. Like microstrip line, strip width is also a key factor in controlling the characteristic impedance of the DSPSL. However, offset top and bottom lines of the DSPSL result in higher impedances. According to [1, 7–9], it finds applications in filters, rat-race hybrid couplers, power dividers and antenna feeds, etc. for frequencies ranging up to 30 GHz.

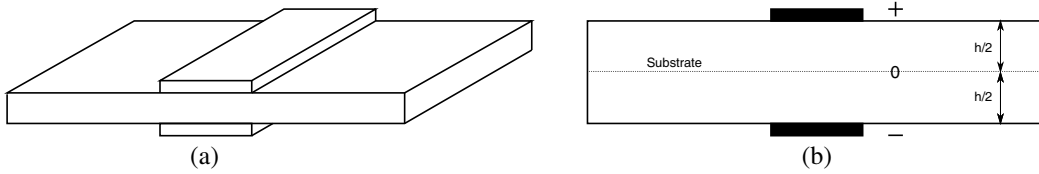


Figure 1. Double-sided parallel-strip line, (a) three dimensional view, (b) cross sectional view.

3. TRANSITION DESIGN

Geometrical layouts of the transitions between $50\ \Omega$ CPW and $50\ \Omega$ DSPSL are shown in Fig. 2. To design a good transition between transmission lines, gradual change in electromagnetic (EM) fields and impedance matching are required. Since realization of different characteristic impedance values of DSPSL is comparatively easy, in these designs only smooth transition of EM field from CPW mode to DSPSL mode is considered to avoid any abrupt discontinuities. However, to obtain field matching, parallel electric field of CPW is to be rotated 90° to become the vertical electric field of DSPSL. The equal magnitude currents flowing in the DSPSL conductors show 180° out of phase nature. On the other hand, due to the presence of two ground lines in CPW, the center strip carries doubled value of their individual current magnitude.

The currents of top strip line of DSPSL and ground lines of CPW have identical directions in the proposed vertical transition structure. The top strip of DSPSL is formed from the connected grounds of CPW which takes a ‘v’-shape in type 1 and semi-ring shape in type 2 transitions, respectively. The center conductor of CPW has to be connected to the bottom strip of DSPSL, and two methods can be used for this. One uses EM coupling between them, and the other is a single via connecting them directly. We choose the latter for our design because of enhanced bandwidth (zero frequency onwards), simple structure and compact size, since EM coupling requires comparatively large structures and low bandwidth.

Multilayer solver (Frequency domain) of CST Microwave Studio (3D planar electromagnetic solver based on MoM) is used for the parametric studies and optimization. The transitions are printed on two similar substrates, Roger’s RO4003C ($\epsilon_r = 3.55$ & $h = 1.524$ mm) and FR4 ($\epsilon_r = 4.3$ & $h = 1.6$ mm). The dimensions of $50\ \Omega$ CPW are determined by CST Microwave Studio utility with the center strip width $W_1 = 4.0$ mm and gap width $G_1 = 0.35$ mm for both cases. Using image theory, the strip width of the $50\ \Omega$ DSPSL can be calculated as $W_2 = 4.4$ mm.

3.1. Type 1

CPW grounds are connected together to form a y junction with the top metal of DSPSL as one arm, just as a power combiner circuit as shown in Fig. 2(b). The thickness of the junction is $L_3 = 4$ mm. The transition length is designed as approximately $\lambda/4$ at the center frequency ($L_1 + L_2 + L_3 = 7.4$ mm).

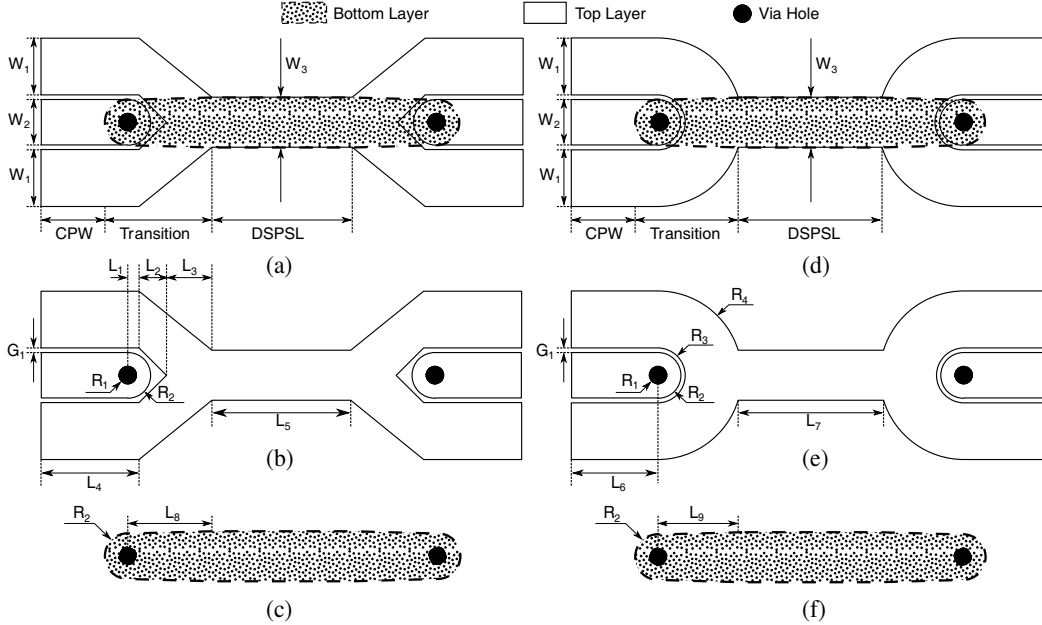


Figure 2. Configuration of the back-to-back transitions (Type 1 & Type 2): (a) schematic layout (Type 1), (b) top view (Type 1), (c) bottom view (Type 1), (d) schematic layout (Type 2), (e) top view (Type 2), and (f) bottom view (Type 2). ($W_1 = 5 \text{ mm}$, $W_2 = 4 \text{ mm}$, $W_3 = 4.4 \text{ mm}$, $G_1 = 0.35 \text{ mm}$, $L_1 = 1 \text{ mm}$, $L_2 = 2.4 \text{ mm}$, $L_3 = 4 \text{ mm}$, $L_4 = 8.6 \text{ mm}$, $L_5 = 6.24 \text{ mm}$, $L_6 = 7.6 \text{ mm}$, $L_7 = 6.24 \text{ mm}$, $L_8 = 7.4 \text{ mm}$, $L_9 = 7.4 \text{ mm}$, $R_1 = 0.75 \text{ mm}$, $R_2 = 2 \text{ mm}$, $R_3 = 2.35 \text{ mm}$, $R_4 = 7.35 \text{ mm}$).

The CPW center strip and DSPSL bottom metal are circularly terminated to form via pads with radius equal to half their width ($R_2 = 2 \text{ mm}$). In Fig. 2(c) after via connection ($R_1 = 0.75 \text{ mm}$), the width of the bottom metal strip is gradually increased for a length ($L_8 = 7.4 \text{ mm}$), to match the width of DSPSL ($W_3 = 4.4 \text{ mm}$).

3.2. Type 2

As shown in Fig. 2(e), ground conductors are circularly tapered with inner radius ($R_3 = 2.35 \text{ mm}$) and outer radius ($R_4 = 7.35 \text{ mm}$) to form the top metal of DSPSL. The rest of the design is exactly the same as Type 1. The total transition length is ($L_9 = 7.4 \text{ mm}$).

4. EQUIVALENT CIRCUIT

The electric field at the open circuit between connected ground conductor and terminated center conductor results in capacitive reactance [6]. A via is used in series with the signal line whenever we wish a signal to change layers in a two-sided or multilayer circuit. The lower frequency response of the via tends to look capacitive. At higher frequencies, the upper and lower pads of the via remain capacitive, but the cylindrical part will become more inductive in nature. An approximate equivalent circuit which excludes coupling effects, for determining the response of the transition, is given in Fig. 3.

The equivalent circuit behaves as a Π network LC low-pass filter which has capacitive components to ground and inductive series components. Transitions involving multiple vias will have the cascading effect of several low-pass filter sections which will provide greater roll off.

5. MEASURED AND SIMULATED RESULTS

The scattering parameters of both back-to-back transitions were simulated and measured using multilayer solver (Frequency domain) of CST Microwave Studio and Keysight Fieldfox N9927A handheld

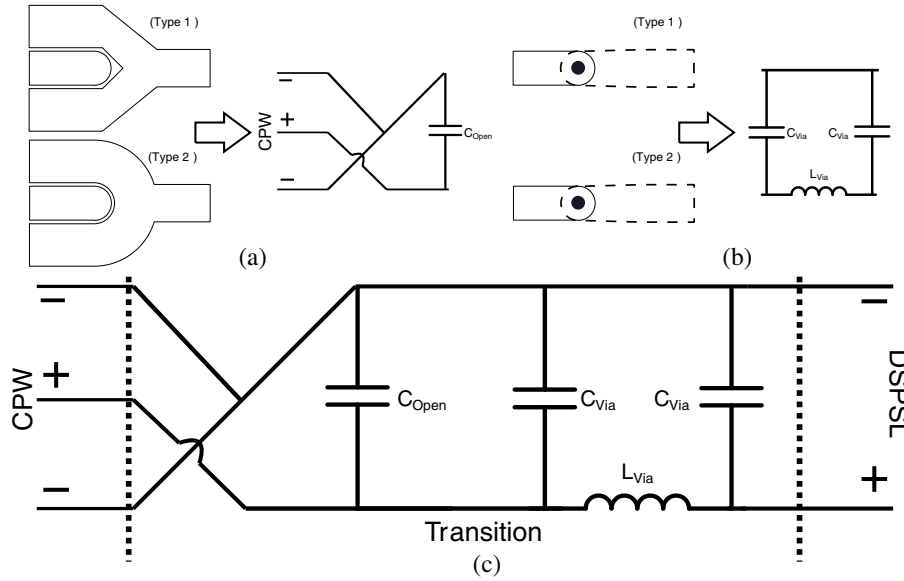


Figure 3. Simplified equivalent circuit: (a) equivalent circuit of CPW with connected grounds, (b) equivalent circuit of via (Lumped), (c) complete equivalent circuit of the transitions (Type 1 & Type 2).

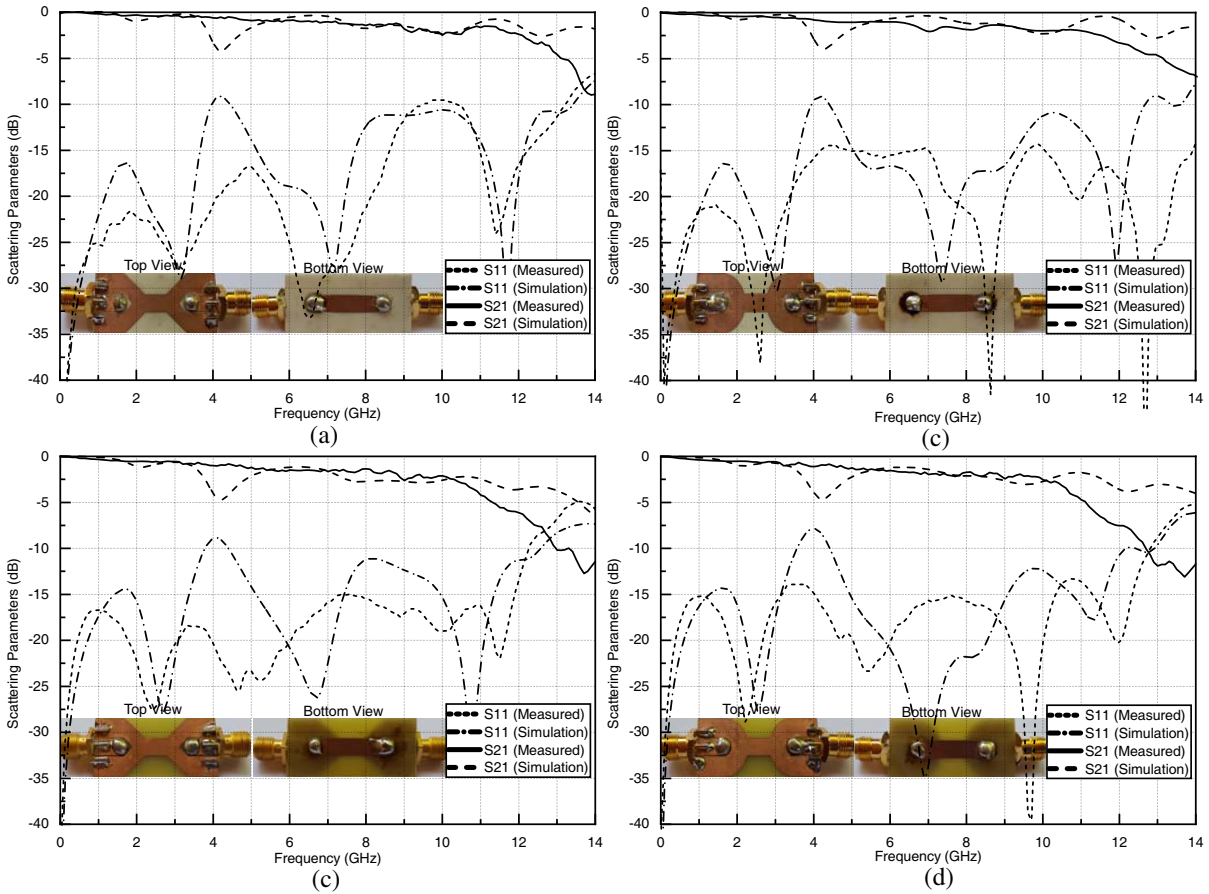


Figure 4. Simulated and measured scattering parameters of the back-to-back transitions, (a) Type 1 (Rogers RO4003C), (b) Type 1 (FR4), (c) Type 2 (Rogers RO4003C), (d) Type 2 (FR4).

Table 1. Measured losses of the back-to-back transitions.

Type	Substrate	Bandwidth (GHz)	Insertion loss (dB)	Return loss (dB)
1	Rogers RO4003C	0.0–12.1	≤ 2.5	≥ 9.0
1	FR4	0.0–11.0	≤ 4.0	≥ 15.0
2	Rogers RO4003C	0.0–11.5	≤ 2.5	≥ 14.5
2	FR4	0.0–10.7	≤ 4.0	≥ 13.4

network analyzer respectively, which are illustrated in Fig. 4 and show good match. The actual photographs of top and bottom views of all transitions are also included in the same figure. Table 1 shows the measured insertion and return losses of the transitions for different substrates.

From the measured group delays, average delay deviation for 30 kHz to 14 GHz is only about 0.021 ns (Type 1 — Rogers RO4003C), 0.014 ns (Type 2 — Rogers RO4003C), 0.016 ns (Type 1 — FR4) and 0.020 ns (Type 2 — FR4) which are relatively small, indicating good transmission phase linearity of the transitions, as shown in Fig. 5.

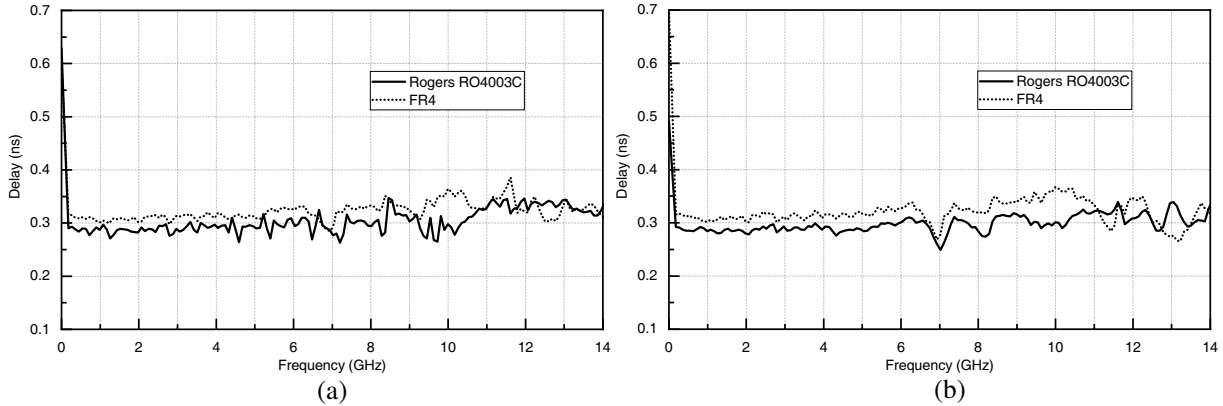


Figure 5. Measured group delays of the back-to-back transitions, (a) Type 1, (b) Type 2.

The insertion loss associated with a single transition, $IL_{Transition}$, can be calculated as

$$IL_{Transition} = (IL_{Total} - L_{CPW} - L_{DSPSL} - L_{SMA})/2$$

where, IL_{Total} is the total measured insertion loss; L_{CPW} and L_{DSPSL} are the insertion losses of the CPW and DSPSL lines respectively; L_{SMA} is the insertion loss of SMA connectors. According to [1, 4], the transmission losses of DSPSL and CPW sections are about 0.03 dB/mm and 0.04 dB/mm, respectively, and insertion loss of a single SMA connector is around 0.09 dB. Therefore, maxima in band insertion loss for a single transition are approximately 0.76 dB and 1.51 dB for the substrates Rogers RO4003C and FR4, respectively.

6. CONCLUSION

Vertical broadband baluns between DSPSL and CPW have been designed, optimized and measured for the first time. The proposed transitions (Types 1 & 2) are based on a single via connection and connected CPW grounds. An approximate equivalent circuit, which is a Π network, LC low-pass filter is discussed. Transitions are fabricated on Rogers RO4003C and FR4 substrates, using a standard photolithography process. These transitions are useful in many applications such as antenna feeds and passive and active microwave components. Besides the vertical transitions of DSPSL in flipped back-to-back form are capable of achieving phase inversion, useful especially in applications like ring couplers, mixers, doublers, etc.

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