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# A Current-Mode-Logic-Based Frequency Divider with Ultra-Wideband and Octet Phases

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**Abstract**—This paper presents a comprehensive analysis of a current-mode-logic frequency divider (CML FD) and the theoretical locking range of CML FD. The locking range of the CML divider is proportional to the injection ratio. By adding a resistive load, the locking range of the CML divider is not limited by the $Q$ value of the LC resonant circuit. The minimum input power to drive the divider is achieved when the output frequency is equal to the self-oscillation frequency. To verify the properties of wideband and multi-phase outputs, the ÷4 octet-phase frequency divider based on a two-stage CML FD was implemented using a 0.18 µm CMOS process. It has a locking range of 1 GHz to 8 GHz with a 12.6 mW dc power consumption, and the phase deviation between the octet output signals is less than 4.7°. With an ultra-wide frequency bandwidth and accurate octet outputs, the proposed divider is suitable for multi-phase generator applications.

## 1. INTRODUCTION

The implement of a subharmonic mixer (SHM) in the direct-conversion receiver was proposed to solve dc-offset problem [1]. The frequency of local oscillator (LO) is one-half or quarter of the RF frequency so that the self-mixing phenomenon can be effectively regenerated [2]. A common approach to generate the multi-phase LO signal is using a multi-phase generator connected with the phase-locked-loop-based (PLL) frequency synthesizer. To generate multi-phase local-oscillator (LO) signals, a multi-phase generator is usually connected with a phase-locked loop (PLL). A common way to develop a multi-phase generator is connecting a quadrature frequency divider (QFD) with a differential voltage-controlled oscillator (VCO). The QFD can offer accurate quadrature signals and also isolate the mixer's input impedance to reduce the VCO's tuning range [3]. With these advantages, the QFD is suitable for multi-phase generation.

The QFD usually requires wide operating bandwidth to ensure robust tracking with the VCO, so the current-mode-logic (CML) FD [4] with wider bandwidth and quadrature outputs is preferred. The operation principle of the ÷2 CML FD has been investigated in previous studies [5, 6]. However, the locking range of the CML FD with resistive load has not been developed thoroughly. In this paper, the locking range of the CML FD in a mathematical form is analyzed. A ÷4 octet FD based on a two-stage CML dividers is also designed to verify the properties of wideband and multi-phase outputs. This ÷4 FD has been shown to achieve a wide locking range of 1 GHz to 8 GHz at −6 dBm injection power, and the phase deviation between octet output signals is less than 4.7°.

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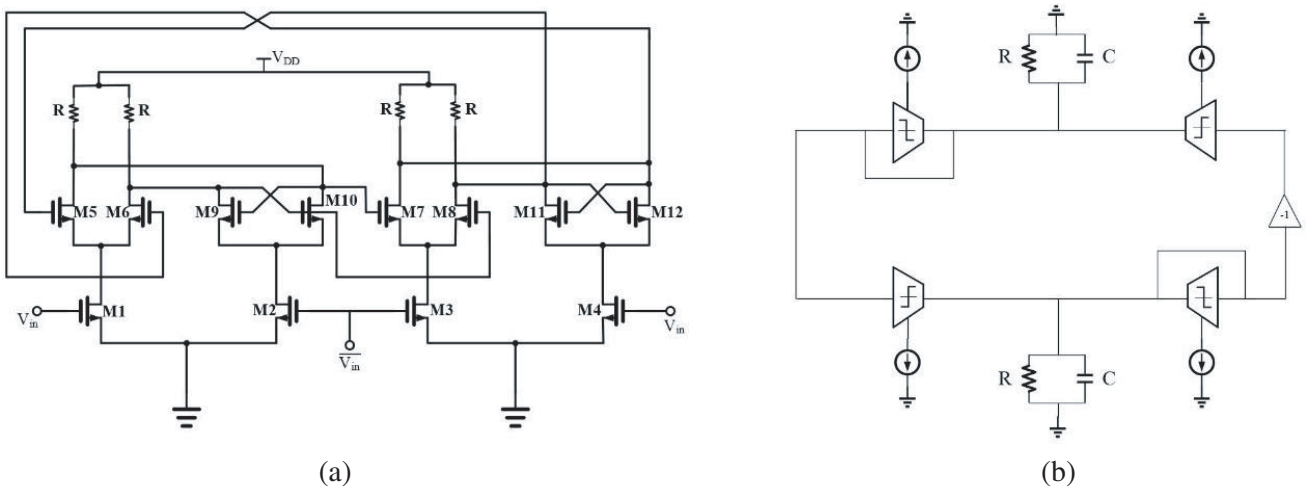
## 2. DESIGN OF A DIVIDE-BY-4 OCTET FREQUENCY DIVIDER

When a CML ring oscillator is injected by sufficient signals with differential phases, the output frequency of the ring oscillator is precisely locked at half of the injection frequency. Using the generalized Adler's equations for large differential injections, a necessary phase condition can be obtained to operate properly for the CML FD. The derived theoretical locking range of the divider is found to be wider than those of other injection-locked frequency dividers (ILFDs).

Figure 1(a) presents the circuit schematic of the ÷2 CML FD, and Fig. 1(b) illustrates the equivalent behavioral model of the CML FD. Including the circuit's nonlinearity, the output differential pairs ($M_5$–$M_8$) and cross-coupled pairs ($M_9$–$M_{12}$) of the CML FD are modeled as the hard-limiter transconductors.




(a) (b)

**Figure 1.** Divide-by-2 CML FD: (a) Circuit schematic and (b) behavior model.

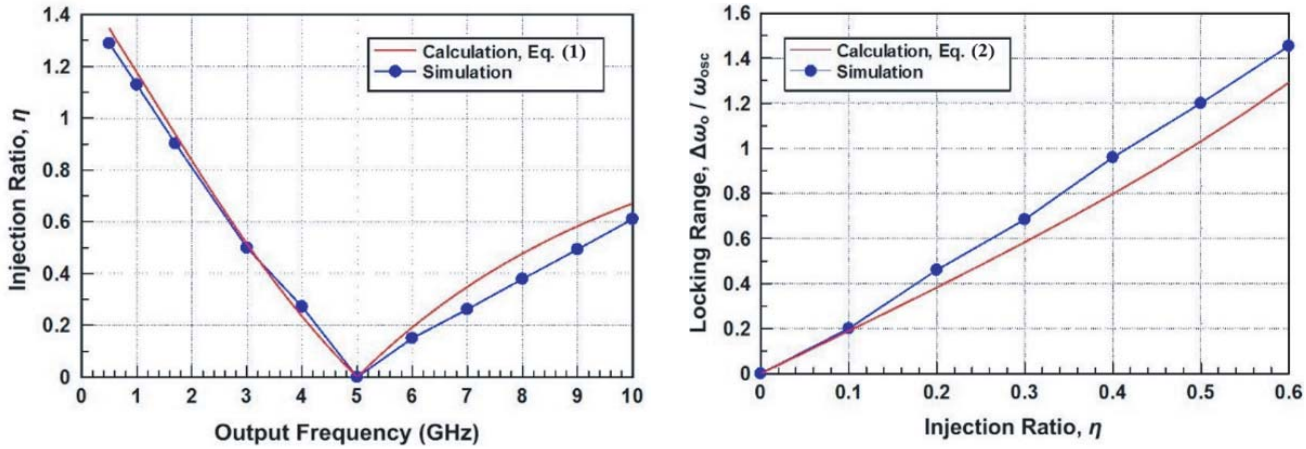
The injection ratio $\eta$ is defined as $I_{inj}/I_D$. By calculating, the minimum required injection current and locking range of the CML FD can be obtained as

$$\eta \geq \frac{3}{2}\frac{\left|\dfrac{\omega_{\text{out}}}{\omega_{\text{osc}}} - 1\right|}{\sqrt{1 + \left(\dfrac{\omega_{\text{out}}}{\omega_{\text{osc}}}\right)^2}}. \tag{1}$$

$$\frac{\Delta\omega_{\text{out}}}{\omega_{\text{osc}}} \leq 2\frac{\sqrt{1 - \left[1 - \left(\dfrac{2}{3}\eta\right)^2\right]^2}}{1 - \left(\dfrac{2}{3}\eta\right)^2}. \tag{2}$$

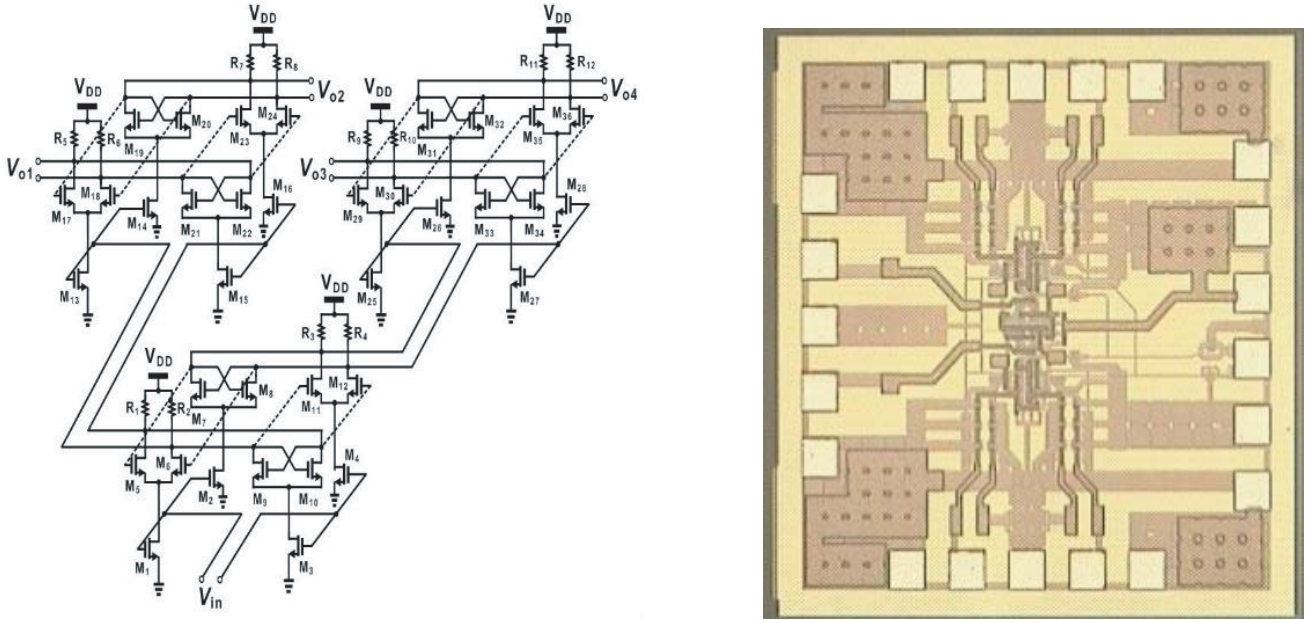
$\omega_{\text{osc}}$ is the self-oscillation frequency, and $\omega_{\text{out}}$ is the output frequency.

Comparison of the calculated locking range of the CML FD using Eq. (1) with circuit simulation from ADS is shown in Fig. 2(a). The proposed CML FD in ADS simulation is under the selected bias and load conditions. The bias dc current $I_{\text{D}}$ is fixed at 1.4 mA, and the resistive load $R$ is 460 Ω. The self-oscillation frequency (SOF) of the CML FD is simulated at 5 GHz, and the simulated output frequency range is from 0.4 GHz to 10 GHz with the corresponding injection ratio 1.3 and 0.6, respectively. By substituting SOF of 5 GHz and different values of the injection ratio into Eq. (1), the calculated output frequency range of the CML FD can be obtained. As shown in Fig. 2(a), the calculated locking range matches well with the simulated one. The deviation is mostly at the last half of the graph, and the error at 10 GHz is approximately 15% due to additional parasitic components which are not included in the model of the CML FD.




(a) (b)

**Figure 2.** Comparison of the (a) calculated minimum injection ratio using the derived equations and simulation results from ADS and (b) locking range versus injection ratio $\eta$ between theory and simulation from ADS.




(a) (b)

**Figure 3.** (a) Schematic of the ÷4 octet FD and (b) chip micrograph of the ÷4 octet FD.

Figure 2(b) shows the comparison of the calculated locking range versus the injection ratio using Eq. (2) and the simulated one from ADS. The simulated locking range agrees with the calculated one. According to the calculated results, $\Delta\omega_{\text{out}}/\omega_{\text{osc}}$ approaches 1 when the injection ration is 0.5, which means that the CML FD can provide a quite large locking range while applying a sufficient input signal. Moreover, the locking range is proportional to the injection ratio and can be enhanced by increasing the injection current under a fixed bias current. The discrepancy between the simulation and calculation becomes obvious at large injection ratio because the divider's nonlinearity is not considered in the behavioral model. Moreover, due to its wide locking range and the quadrature outputs by using the derived model, the CML FD can be used for the ÷4 octet FD.

The schematic of the ÷4 octet FD is shown in Fig. 3(a). It includes two stages of ÷2 CML FDs. The quadrature outputs of the first-stage CML FD are applied to the next stage of two CML FDs with the injection phases of 0°, 180° and 90°, 270°, respectively. Therefore, a division ratio of 4 is obtained because of the two divide-by-2 stages. The 90° phase difference associated with the second-stage FD input frequency is divided by two, so the output phases of the two dividers differ by 45°, which includes 0°, 90°, 180°, and 270° generated by one divider, as well as 45°, 135°, 225°, and 315° generated by the other one. The complete parameters of the proposed ÷4 FD are listed in Table 1.

**Table 1.** Circuit parameters of the proposed ÷4 octet FD.

| Devices | Values | Devices | Values | Devices | Values |
|---|---|---|---|---|---|
| $M_1$–$M_4$ | 70/0.18 | $M_{13}$–$M_{16}$ | 2/0.18 | $M_{25}$–$M_{28}$ | 2/0.18 |
| $M_5$–$M_{12}$ | 12/0.18 | $M_{17}$–$M_{24}$ | 8/0.18 | $M_{29}$–$M_{36}$ | 8/0.18 |
| $R_1$–$R_4$ | 350 Ω | $R_5$–$R_8$ | 1 kΩ | $R_9$–$R_{12}$ | 1 kΩ |

## 3. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The proposed ÷4 Octave FD was fabricated with 0.18 µm 1P6M CMOS technology. The chip micrograph is shown in Fig. 3(b), and the size is $0.78 \times 0.79\,\text{mm}^2$. With a 1.8 V dc supply voltage, the ÷4 Octave FD consumes 12.6 mW dc power, including 10.1 and 2.5 mW for the first- and the second-stage CML FDs. Process voltage temperature (PVT) influence is tiny.

As shown in Fig. 4(a), the measured locking range of the ÷4 octet FD is 1 GHz to 8 GHz at an input power of −6 dBm, and the minimum input power of −35 dBm is at 7 GHz. When the input power is decreased to −10 dBm, the locking range still covers 4.3 GHz from 3.6–7.9 GHz. Fig. 4(b) illustrates the measured output power of $V_{01}$, $V_{02}$, $V_{03}$ and $V_{04}$ as a function of input frequency. The output powers are all greater than −16 dBm over the entire input frequency range, and the peak value of the output power is at 4 GHz. The maximum power difference of $V_{o1}$ to $V_{o2}$ and $V_{o3}$ to $V_{o4}$ is 1.1 dB and 2.8 dB, respectively.

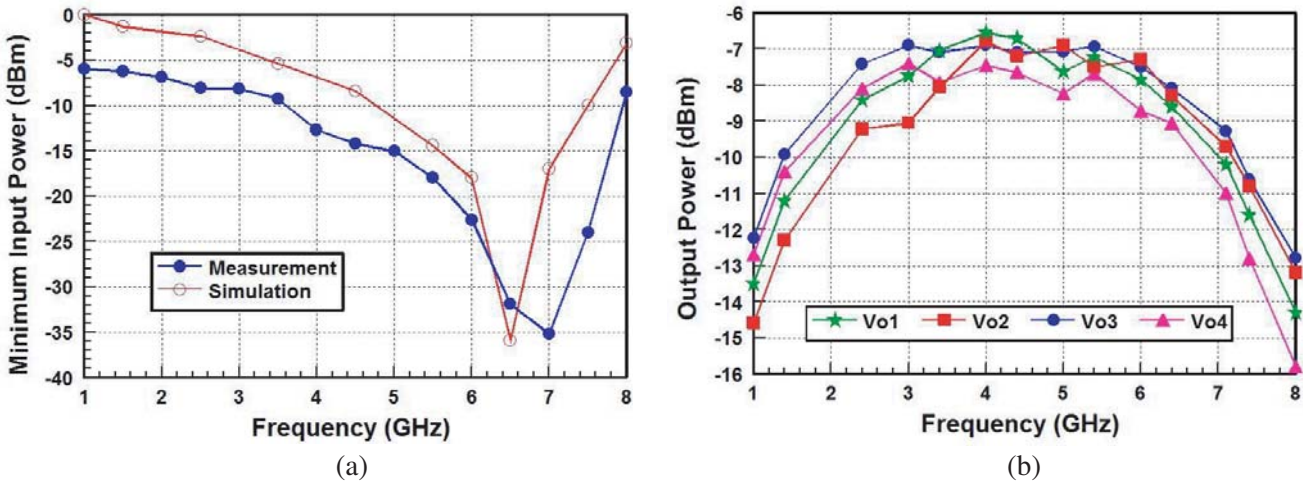
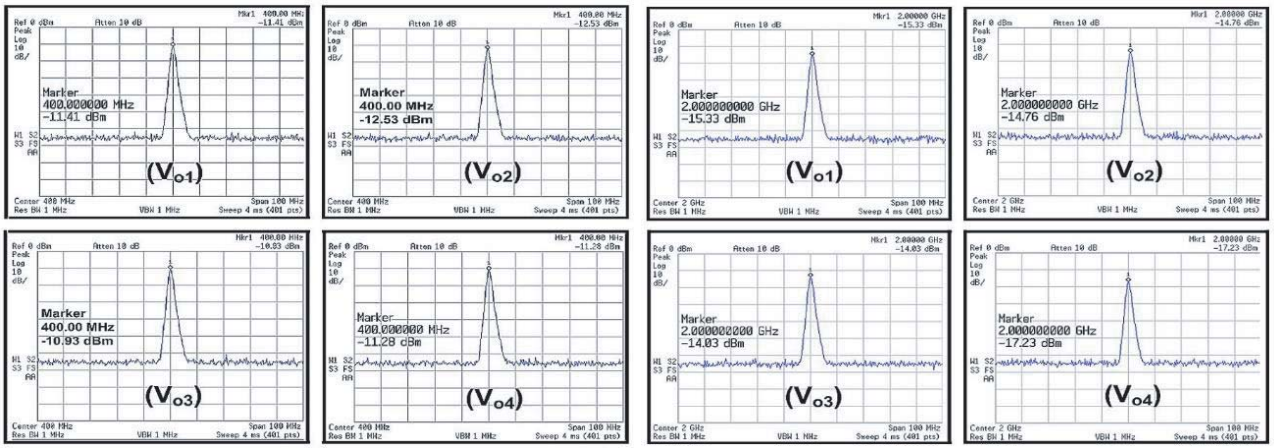


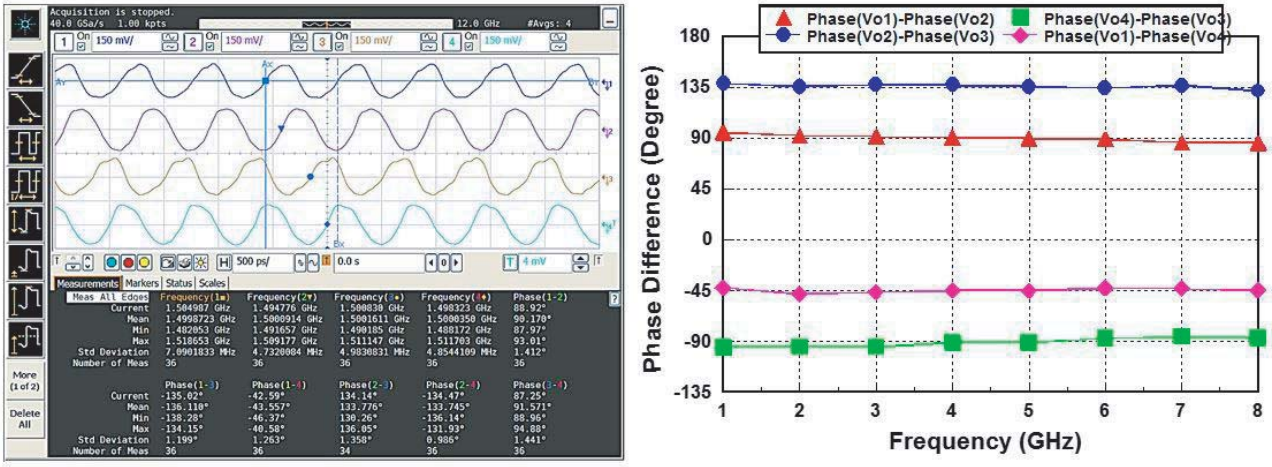

**Figure 4.** (a) Measured input sensitivities versus simulation results and (b) measured output power of the ÷4 FD.

According to Fig. 5(a), the output signals $V_{o1}$ to $V_{o4}$ are locked at 0.4 GHz when the input frequency is 1.6 GHz, and the output powers are all larger than −12.53 dBm. Fig. 5(b) presents that the output signal is 2 GHz when the divider is locked at the input frequency of 8 GHz. In this state, the output powers are larger than −17.23 dBm.




(a) (b)

**Figure 5.** Measured output spectra of the locked signals at (a) $f_{in} = 1.6\,\text{GHz}$ and (b) $f_{in} = 8\,\text{GHz}$.




(a) (b)

**Figure 6.** (a) The measured waveform of the locked output signals at $f_{in} = 6\,\text{GHz}$ and (b) phase difference between the output signals as a function of the input frequency.

Figure 6(a) illustrates measured time-domain output waveforms when the input signals are locked at 1.5 GHz. The phase differences between $V_{o1}$–$V_{o2}$ and $V_{o3}$–$V_{o4}$ are 88.92° and 87.25°, respectively. The phase differences between $V_{o1}$–$V_{o3}$, $V_{o1}$–$V_{o4}$, $V_{o2}$–$V_{o3}$ and $V_{o2}$–$V_{o4}$ are −135.02°, −42.59°, 134.14°, and −134.47°, respectively. Fig. 6(b) presents that over the whole locking range, the phases deviate from −90°, −45°, 90° and 135°, and are less than 4.5°, 2.9°, 4.7° and 3.3°, respectively. The phase error is primarily caused by connectors, cables and mismatch of the on-chip devices, and the output waveforms are asymmetric. However, the main reason is that the buffer circuits suffer from the process variation and device mismatch.

$$\text{FOM} = \frac{\text{Locking Range}\,(\%) \times \text{Division Ratio}}{\text{P}_{\text{in}}\,(\text{mW}) \times \text{P}_{\text{DC}}\,(\text{mW})} \tag{3}$$

The comparisons of the proposed ÷4 octet FD with state-of-art published FDs are summarized in Table 2. The figure-of-merit (FOM) to evaluate an FD is defined in Eq. (3). Compared with other CMOS FDs, the proposed FD has a high division ratio, low input power, and an excellent locking range. The octet-phase outputs are also achieved. Therefore, the proposed divider obtains an outstanding FOM value.

**Table 2.** Comparisons with state-of-art FDs.

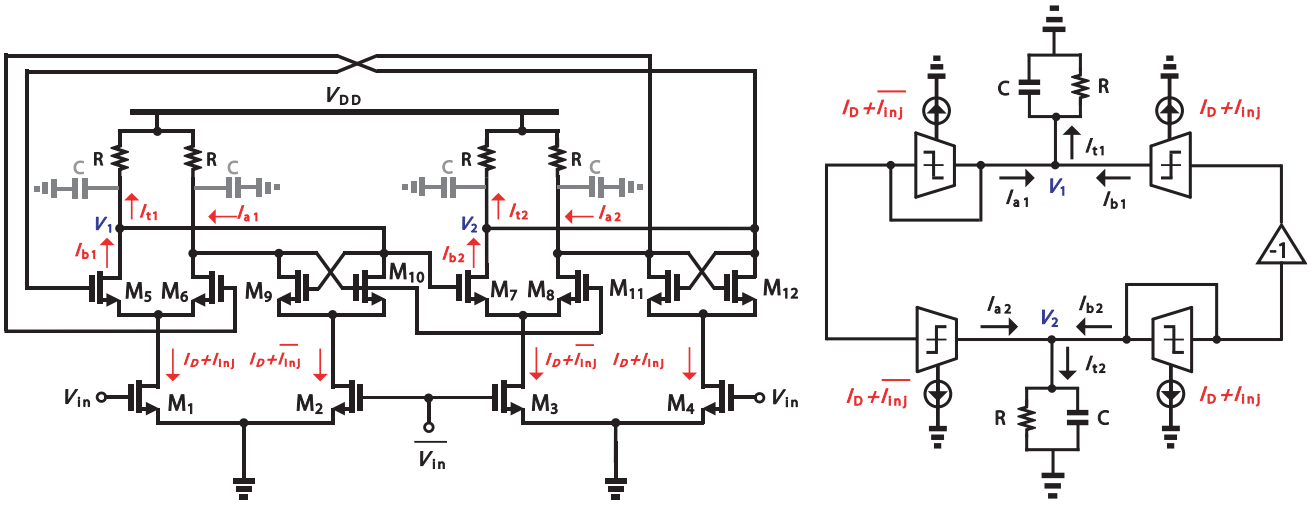
| References | This Work | [6] | [7] | [8] | [9] | [10] | [11] |
|---|---|---|---|---|---|---|---|
| Technology (μm) | 0.18 | 0.18 | 0.18 | 0.18 | 0.13 | 0.09 | 0.18 |
| Division Ratio | 4 | 2 | 4 | 4 | 2 | 2 | 4 |
| Input/Output | Diff./Octet. | Diff/Quad. | Single/Diff. | Single/Quad. | Diff/Quad. | Diff/Quad. | Single/Diff. |
| Locking Range (GHz) | 1–8 (155.5%) | 7.5–20 (90.9%) | 8.8–12.7 (36.28%) | 6.86–8.02 (15.6%) | 12–18 (40%) | 2–35.5 (178.6%) | 9.9–12.1 (20%) |
| $P_{in}$ (dBm) | −6 | 0 | 0 | 0 | 0 | 0 | 0 |
| $P_{DC*}$ (mW) | 12.6 | 4.3 | 3.61 | 3.12 | 12 | 28.8 | 25.44 |
| FOM | 1.97 | 0.43 | 0.41 | 0.2 | 0.07 | 0.12 | 0.031 |
| Size ($mm^2$) | 0.61 | 0.014# | 0.78 | 1.05 | 1 | 0.63 | 0.4 |

* DC power is normalized to quadrature outputs. # Core area only.

## 4. CONCLUSION

In this paper, a ÷4 octet FD based on a two-stage CML FDs with a 0.18 μm CMOS technology is implemented. The locking range is not limited by the $Q$ value of the LC resonant circuit. The calculations of the designed CML FD agree well with the circuit's simulation results. With the advantages of ultra-wide locking range and accurate octet output phases, the proposed ÷4 FD is suitable for application to SIMO and MIMO microwave systems.

## APPENDIX A.




Two sinusoidal input signals with inversed phases are applied, $V_{in}(t) = A_i(t)\exp(j\theta_{inj}(t))$ and $\overline{V_{in}}(t) = A_i(t)\exp(j(\theta_{inj}(t)+\pi))$.

The divider creates two output voltages, $V_1(t) = A_1(t)\exp(j\theta_1(t))$ and $V_2(t) = A_2(t)\exp(j\theta_2(t))$.

Superposing the injection currents and bias currents, the tail currents can be expressed as, $I_{inj}\exp(j\theta_{inj}(t)) + I_D$ and $I_{inj}\exp(j(\theta_{inj}(t)+\pi)) + I_D$. $\theta_{inj}$, $\theta_1$, and $\theta_2$ represent the angular frequency of the corresponding signals.

The currents $I_{a1}$ and $I_{b1}$ at the output of the first-stage circuit of the CML FD can be denoted as,

$$\begin{aligned} I_{a1} &= \frac{4}{\pi}\left(\cos\theta_1 - \frac{1}{3}\cos 3\theta_1 + \frac{1}{5}\cos 5\theta_1 + \ldots\right) \times [I_D + I_{inj}\cos(\theta_{inj}+\pi)] \\ &= \frac{4}{\pi}\left(I_D\cos\theta_1 - I_{inj}\cos\theta_{inj}\cos\theta_1 + \frac{1}{3}I_{inj}\cos 3\theta_1\cos\theta_{inj} + \ldots\right) \end{aligned} \quad \text{(A1)}$$

$$I_{\mathrm{b1}} = \frac{4}{\pi}\left[\cos(\theta_2+\pi) - \frac{1}{3}\cos 3(\theta_2+\pi) + \frac{1}{5}\cos 5(\theta_2+\pi) + \ldots\right] \times (I_{\mathrm{D}} + I_{\mathrm{inj}}\cos\theta_{\mathrm{inj}})$$
$$= -\frac{4}{\pi}\left(I_{\mathrm{D}}\cos\theta_2 + I_{\mathrm{inj}}\cos\theta_{\mathrm{inj}}\cos\theta_2 - \frac{1}{3}I_{\mathrm{inj}}\cos 3\theta_2\cos\theta_{\mathrm{inj}} + \ldots\right). \quad \text{(A2)}$$

All higher harmonics in $I_{\mathrm{a1}}$ and $I_{\mathrm{b1}}$ will be significantly attenuated because of filtering in the RC circuit, so Eqs. (A1) and (A2) can be approximated as,

$$I_{a1} = \frac{4}{\pi}\left[I_{\mathrm{D}}e^{j\theta_1} - \frac{1}{2}I_{\mathrm{inj}}e^{j\left(\theta_{\mathrm{inj}}-\theta_1\right)} + \frac{1}{6}I_{\mathrm{inj}}e^{j\left(3\theta_1-\theta_{\mathrm{inj}}\right)}\right] \quad \text{(A3)}$$

$$I_{\mathrm{b1}} = \frac{4}{\pi}\left[-I_{\mathrm{D}}e^{j\theta_2} - \frac{1}{2}I_{\mathrm{inj}}e^{j\left(\theta_{\mathrm{inj}}-\theta_2\right)} + \frac{1}{6}I_{\mathrm{inj}}e^{j\left(3\theta_2-\theta_{\mathrm{inj}}\right)}\right]. \quad \text{(A4)}$$

Combining Eqs. (A3) and (A4), the total current renter RC circuit at node 1 can be derived as,

$$I_{\mathrm{t1}} = \frac{4}{\pi}\left[I_{\mathrm{D}} - I_{\mathrm{D}}e^{j(\theta_2-\theta_1)} - \frac{I_{\mathrm{inj}}}{2}e^{j\left(\theta_{\mathrm{inj}}-2\theta_1\right)} + \frac{I_{\mathrm{inj}}}{6}e^{j\left(2\theta_1-\theta_{\mathrm{inj}}\right)}\right]. \quad \text{(A5)}$$

The output current of the second-stage circuit of the CML FD is,

$$I_{\mathrm{a2}} = \frac{4}{\pi}\left[I_{\mathrm{D}}e^{j\theta_1} - \frac{1}{2}I_{\mathrm{inj}}e^{j\left(\theta_{\mathrm{inj}}-\theta_1\right)} + \frac{1}{6}I_{\mathrm{inj}}e^{j\left(3\theta_1-\theta_{\mathrm{inj}}\right)}\right] \quad \text{(A6)}$$

$$I_{\mathrm{b2}} = \frac{4}{\pi}\left[I_{\mathrm{D}}e^{j\theta_2} + \frac{1}{2}I_{\mathrm{inj}}e^{j\left(\theta_{\mathrm{inj}}-\theta_2\right)} - \frac{1}{6}I_{\mathrm{inj}}e^{j\left(3\theta_2-\theta_{\mathrm{inj}}\right)}\right]. \quad \text{(A7)}$$

The total current entering RC circuit at node 2 is,

$$I_{\mathrm{t2}} = \frac{4}{\pi}\left[I_{\mathrm{D}} + I_{\mathrm{D}}e^{j(\theta_1-\theta_2)} + \frac{I_{\mathrm{inj}}}{2}e^{j\left(\theta_{\mathrm{inj}}-2\theta_2\right)} - \frac{I_{\mathrm{inj}}}{6}e^{j\left(2\theta_2-\theta_{\mathrm{inj}}\right)}\right]. \quad \text{(A8)}$$

Using Kirchhoff's current law (KCL) at output nodes of $V_1$ and $V_2$ can be expressed as,

$$\frac{A_1e^{j\theta_1}}{R} + C\frac{dA_1}{dt}e^{j\theta_1} + jCA_1e^{j\theta_1}\frac{d\theta_1}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}} - I_{\mathrm{D}}e^{j(\theta_2-\theta_1)} - \frac{I_{\mathrm{inj}}}{2}e^{j\left(\theta_{\mathrm{inj}}-2\theta_1\right)} + \frac{I_{\mathrm{inj}}}{6}e^{j\left(2\theta_1-\theta_{\mathrm{inj}}\right)}\right] \quad \text{(A9)}$$

$$\frac{A_2}{R} + C\frac{dA_2}{dt} + jCA_2\frac{d\theta_2}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}} + I_{\mathrm{D}}e^{j(\theta_1-\theta_2)} + \frac{I_{\mathrm{inj}}}{2}e^{j\left(\theta_{\mathrm{inj}}-2\theta_2\right)} - \frac{I_{\mathrm{inj}}}{6}e^{j\left(2\theta_2-\theta_{\mathrm{inj}}\right)}\right]. \quad \text{(A10)}$$

The real parts derived from Eqs. (9) and (10) related the amplitudes of the output voltage to the amplitudes of the injection signals,

$$\frac{A_1}{R} + C\frac{dA_1}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}} - I_{\mathrm{D}}\cos(\Delta\theta) - \frac{I_{\mathrm{inj}}}{2}\cos(\varphi_1) + \frac{I_{\mathrm{inj}}}{6}\cos(-\varphi_1)\right] \quad \text{(A11)}$$

$$\frac{A_2}{R} + C\frac{dA_2}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}} + I_{\mathrm{D}}\cos(\Delta\theta) + \frac{I_{\mathrm{inj}}}{2}\cos(\varphi_2) - \frac{I_{\mathrm{inj}}}{6}\cos(-\varphi_2)\right]. \quad \text{(A12)}$$

$$\Delta\theta = \theta_1 - \theta_2 \quad \text{(A13)}$$

$$\varphi_1 = \theta_{\mathrm{inj}} - 2\theta_1 \quad \text{(A14)}$$

$$\varphi_2 = \theta_{\mathrm{inj}} - 2\theta_2. \quad \text{(A15)}$$

Given that the output amplitudes $A_1$ and $A_2$ in a steady state vary slowly with time ($dA_1/dt$, $dA_2/dt \approx 0$), the real parts of Eqs. (A11) and (A12) can be expressed as,

$$A_1 = \frac{4R}{\pi}\left[I_{\mathrm{D}} - I_{\mathrm{D}}\cos(\Delta\theta) - \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_1)\right] \quad \text{(A16)}$$

$$A_2 = \frac{4R}{\pi}\left[I_{\mathrm{D}} + I_{\mathrm{D}}\cos(\Delta\theta) + \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_2)\right]. \quad \text{(A17)}$$

The image parts of Eqs. (11) and (12) are,

$$CA_1\frac{d\theta_1}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}}\sin(\Delta\theta) - \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_1)\right] \tag{A18}$$

$$CA_2\frac{d\theta_2}{dt} = \frac{4}{\pi}\left[I_{\mathrm{D}}\sin(\Delta\theta) + \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_2)\right]. \tag{A19}$$

Substituting Eqs. (A16) and (A17) into Eqs. (A18) and (A19), two differential equations representing the instantaneous output phases of the first- and second-stage circuit of the CML FD can be derived as,

$$\frac{d\theta_1}{dt} = \frac{1}{RC}\frac{I_{\mathrm{D}}\sin(\Delta\theta) - \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_1)}{I_{\mathrm{D}} - I_{\mathrm{D}}\cos(\Delta\theta) - \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_1)} \tag{A20}$$

$$\frac{d\theta_2}{dt} = \frac{1}{RC}\frac{I_{\mathrm{D}}\sin(\Delta\theta) + \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_2)}{I_{\mathrm{D}} + I_{\mathrm{D}}\cos(\Delta\theta) + \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_2)}. \tag{A21}$$

Because the CML FD works at the free-running state or injection-locked state, the phase difference of the output signals maintains 90° (i.e., $\Delta\theta = \pi/2$), and Eqs. (A20) and (A21) can be rewritten as,

$$\frac{d\theta_1}{dt} = \frac{1}{RC}\frac{I_{\mathrm{D}} - \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_1)}{I_{\mathrm{D}} - \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_1)} \tag{A22}$$

$$\frac{d\theta_2}{dt} = \frac{1}{RC}\frac{I_{\mathrm{D}} + \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_2)}{I_{\mathrm{D}} + \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_2)}. \tag{A23}$$

Considering the free-running state when the CML FD is in the absence of the injection signal ($I_{\mathrm{inj}} = 0$), the SOF ($\omega_{\mathrm{osc}}$) can be obtained from Eqs. (A22) and (A23) as,

$$\frac{d\theta_1}{dt} = \frac{d\theta_2}{dt} = \frac{1}{RC} = \omega_{\mathrm{osc}}. \tag{A24}$$

The instantaneous angular frequency of the output signal is equal to half of the injection ones, where $d\theta_1/dt = d\theta_2/dt = \omega_{\mathrm{out}} = \omega_{\mathrm{inj}}/2$. Therefore, Eqs. (A22) and (A23) are satisfied by using the following equation,

$$\frac{I_{\mathrm{D}} - \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_1)}{I_{\mathrm{D}} - \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_1)} = \frac{I_{\mathrm{D}} + \frac{2}{3}I_{\mathrm{inj}}\sin(\varphi_2)}{I_{\mathrm{D}} + \frac{1}{3}I_{\mathrm{inj}}\cos(\varphi_2)}. \tag{A25}$$

A solution can be found to satisfy Eq. (A21),

$$\varphi_2 = \varphi_1 + \pi. \tag{A26}$$

Assume $\varphi_1 = \varphi$ and $\varphi_2 = \varphi + \pi$. The injection ratio $\eta$ is defined as $I_{\mathrm{inj}}/I_{\mathrm{D}}$ by applying Eqs. (A24) and (A26) into Eq. (A23), and the output frequency is,

$$\omega_{\mathrm{out}} = \frac{d\theta_2}{dt} = \omega_{\mathrm{osc}}\frac{1 + \frac{2}{3}\eta\sin(\varphi)}{1 + \frac{1}{3}\eta\cos(\varphi)}. \tag{A27}$$

$\varphi$ can be determined by,

$$\varphi = \sin^{-1}\left[\frac{\frac{\omega_{\text{out}}}{\omega_{\text{osc}}} - 1}{\frac{2}{3}\eta\sqrt{1+\left(\frac{\omega_{\text{out}}}{\omega_{\text{osc}}}\right)^2}}\right] - \tan^{-1}\left(\frac{\omega_{\text{out}}}{\omega_{\text{osc}}}\right). \tag{A28}$$

From Eq. (A28), the minimum injection ratio is,

$$\eta \geq \frac{3}{2}\frac{\left|\frac{\omega_{\text{out}}}{\omega_{\text{osc}}} - 1\right|}{\sqrt{1+\left(\frac{\omega_{\text{out}}}{\omega_{\text{osc}}}\right)^2}}. \tag{A29}$$

According to Eq. (A29), we get,

$$\frac{\left(\frac{\omega_{\text{out}}}{\omega_{\text{osc}}} - 1\right)^2}{1+\left(\frac{\omega_{\text{out}}}{\omega_{\text{osc}}}\right)^2} \leq \left(\frac{2}{3}\eta\right)^2. \tag{A30}$$

$$\frac{\Delta\omega_{\text{out}}}{\omega_{\text{osc}}} \leq 2\frac{\sqrt{1-\left[1-\left(\frac{2}{3}\eta\right)^2\right]^2}}{1-\left(\frac{2}{3}\eta\right)^2}. \tag{A31}$$

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