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A Compact Ka-Band TDD Transceiver System Module with Attractive Temperature Characteristic

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Abstract—This paper presents a Ka-band TDD transceiver system module for the secondary surveillance radar application with attractive temperature characteristic. Four multifunction chips and a MEMS filter are designed and fabricated in GaAs pseudomorphic high electron mobility transistor (pHEMT) process and MEMS technology in this work, respectively. These multifunction chips and MEMS filter with some other commercial chips are assembled in a compact cavity to form the transceiver system. The temperature characteristics of the designed chips and the whole transceiver module are measured respectively in this work. Benefiting from the designed temperature compensation circuits on the chips, the transceiver is able to work from -55°C to $+75^{\circ}$C with little performance fluctuation. The noise figure of the receiver is less than 3.7 dB in the 400 MHz working bandwidth. Its dynamic range is more than 59 dB with more than 23.9 dB power gain. The maximum output power of the transmitter is larger than 30.3 dBm. The system only has two input/output ports and one control bus, which is suitable for the large-scale system integration.

1. INTRODUCTION

Spectrum has been very crowded in the sub-6 GHz band. It is difficult to find a wide spectrum for the high-speed communication or radar application. Microwave and millimeter-wave bands are attractive because of the large absolute bandwidth [1, 2]. Ka-band is suitable for many applications, such as satellite communications and phased array radar, and is a promising band for the upcoming 5G communication [3]. This paper presents a compact Ka-band transceiver system module for the secondary surveillance radar application with attractive temperature characteristic. The transceiver operates in time division duplexing (TDD) mode and consists of four designed multifunction chips, a designed filter and some commercial chips. The designed chips in the module are fabricated in GaAs pHEMT, and the filter is fabricated in MEMS technology. All of the chips are assembled in a compact cavity using the bonding wire process. The cavity is sealed with the parallel seam welding technology. As a result, the module has high airtightness and reliability. The module only has two input/output ports and one control bus, which is suitable for the large scales integration, such as phased array radar and MIMO base station. The maximum output power of the transmitter is 30.3 dBm, and the out-of-band spur suppression is larger than 46 dBc. The noise figure of the receiver is lower than 3.7 dB at room temperature. The dynamic range of the receiver is larger than 59 dB with more than 23.9 dB power gain. An off-chip temperature compensated attenuator and on-chip temperature compensated biasing networks are adopted to enable the transceiver to work from -55°C to $+75^{\circ}$C with little performance fluctuation. The output power variation is less than ± 1.2 dB in all temperature ranges within the

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400 MHz working bandwidth, and the noise figure variation is less than ±0.84 dB. At the same time, the power gain of the receiver variation is less than ±1.4 dB.

2. SYSTEM ARCHITECTURE

The architecture of the system is shown in Fig. 1. The chip 1 ∼ 4 are the multifunction chips designed in this work, while the other chips are the commercial chips. IF signal and local oscillator (LO) signal use the same port to minimize the number of ports. A diplexer is designed in the cavity to separate the IF signal and LO signal. The input LO signal is located at X-band and multiplied by 4 times by chip 2. Then the signal is amplified and passes an on-chip filter to reduce the spurs of LO signal. The system works in the TDD mode for the secondary surveillance radar application. The Σ and Δ channels are implemented using the TR switches. Then they are connected with the antenna using the beam direction synthesis network. The receiver and transmitter use the same mixer and filter to minimize the size of the whole system. The MEMS filter with high quality factor is used to suppress the image frequency and spurious signals. A temperature compensated attenuator is inserted into the receive link to enhance the dynamic range and compensate the gain of the link at the different temperature. Furthermore, on-chip temperature compensate biasing networks, which give proper biasing ports to the amplifiers, are adopted to stabilize the performance of the designed chips at the different temperature. The parameters allocation of the system is shown in Fig. 1. The power management chips and control circuits are integrated in the module, which enable the circuit to work in the pulse mode.

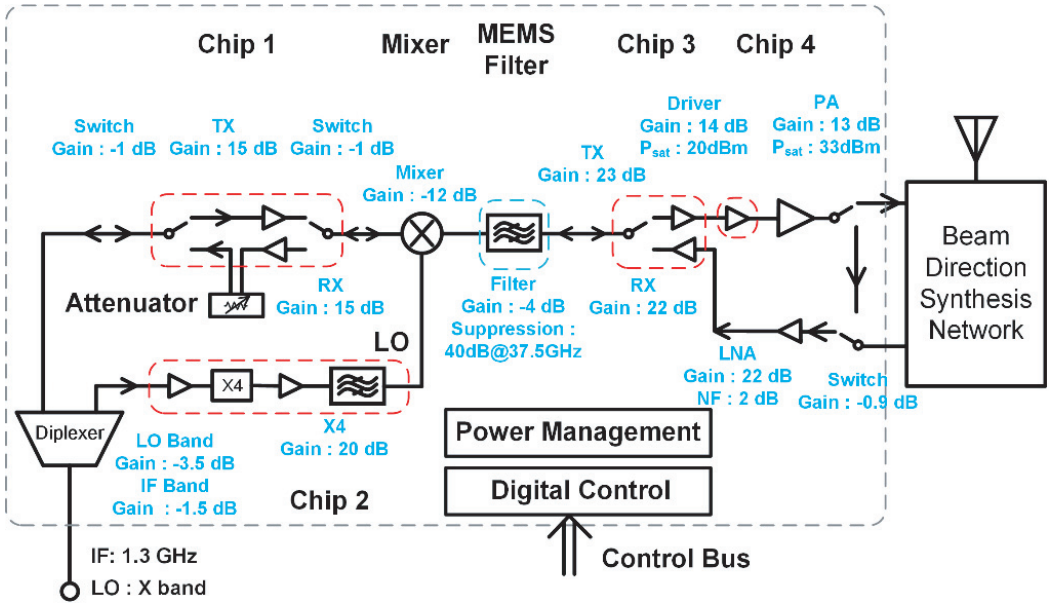

Figure 1. The architecture of the proposed transceiver module.

3. CIRCUIT DESIGN

3.1. Chip 1

Chip 1 contains two switches and two amplifiers, which are used to amplify the IF signals in the receiver and transmitter, respectively. The schematic of the switches is shown in Fig. 2(a). In the switches, both of the receiver link and transmitter link contain a series transistor and a parallel one [4]. The transistors are controlled by changing the gate bias voltage. The schematic of amplifiers is shown in Fig. 2(b). The size of transistors is 140 μm. Parallel negative feedback is used to enhance the stability factor. The source resistor Rs generates a positive voltage at the transistor's source terminal and then forms a negative V_{gs} biasing voltage. The C_s provides an AC ground for the RF signal.

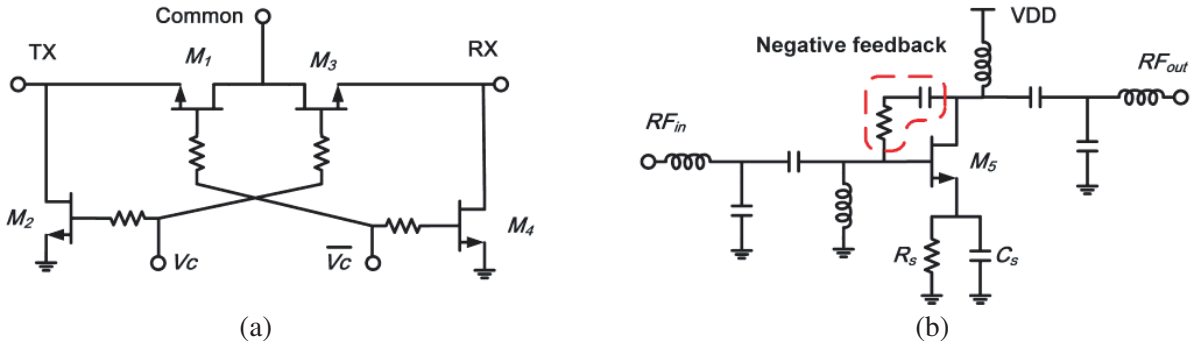

Figure 2. The schematic of (a) switches (b) amplifiers in chip 1.

3.2. Chip 2

The function of chip 2 is to multiply the signal four times and amplify it. The schematic of the quadrupler is shown in Fig. 3. The transistor works as a nonlinear device to generate harmonic waves [5]. The transmission line T3 at the output port is an open-circuited $\lambda/4$ transmission line at f, which is used to reduce the fundamental wave and odd harmonic waves at the output port. T4 is an open-circuited $\lambda/4$ transmission line at $2f$, which is used to reduce the second and sixth harmonic waves. The output matching network is tuned at $4f$. T1 and T2 at the input port is an open-circuited $\lambda/4$ transmission line at $2f$ and $4f$, which is used to reduce the reflection of second and fourth harmonic wave. The output fourth harmonic wave is amplified and passes an on-chip filter to reduce the spurs spurs.

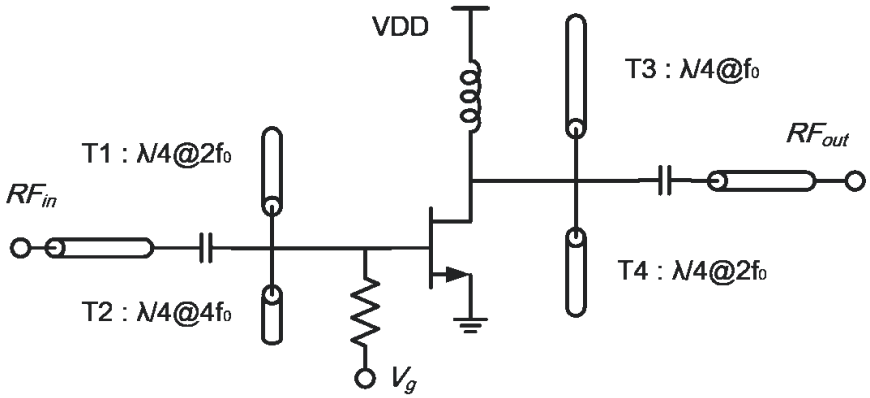

Figure 3. The schematic of the quadrupler in chip 2.

3.3. Chip 3

Chip 3 contains one switch and two amplifiers. The switch works at Ka-band. Therefore, the series and parallel structure in chip 1 is not adopted because of the high loss in the millimeter-wave band [6]. Traveling wave switch is used in chip 3 and the schematic is shown in Fig. 4 [7]. When it works in RX mode, the transistor at TX port is turned on to low impedance and transformed to high impedance by the $\lambda/4$ transmission line. Then the light arm is open and the signal passes to RX port. When it works in the TX mode, all controls are symmetrical. There are no series transistors in the signal link, which reduces the loss of the switch. Moreover, compared with the transistors, the transmission lines made up by the passive metal are independent of temperature, which reduces the performance variation of the system.

The schematic of the amplifier in receiver link is shown in Fig. 5(a). Four stages are adapted. Current-reused structure [8] is used in stage 1 and stage 2 to minimize the power consumption, which is

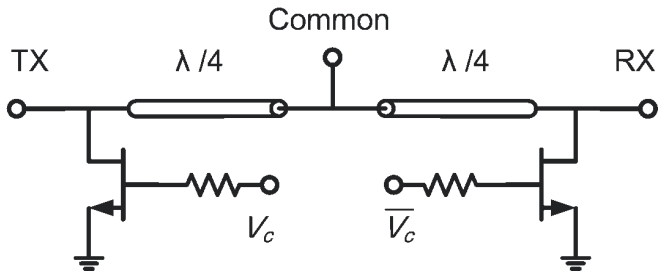

Figure 4. The schematic of switch in chip 3.

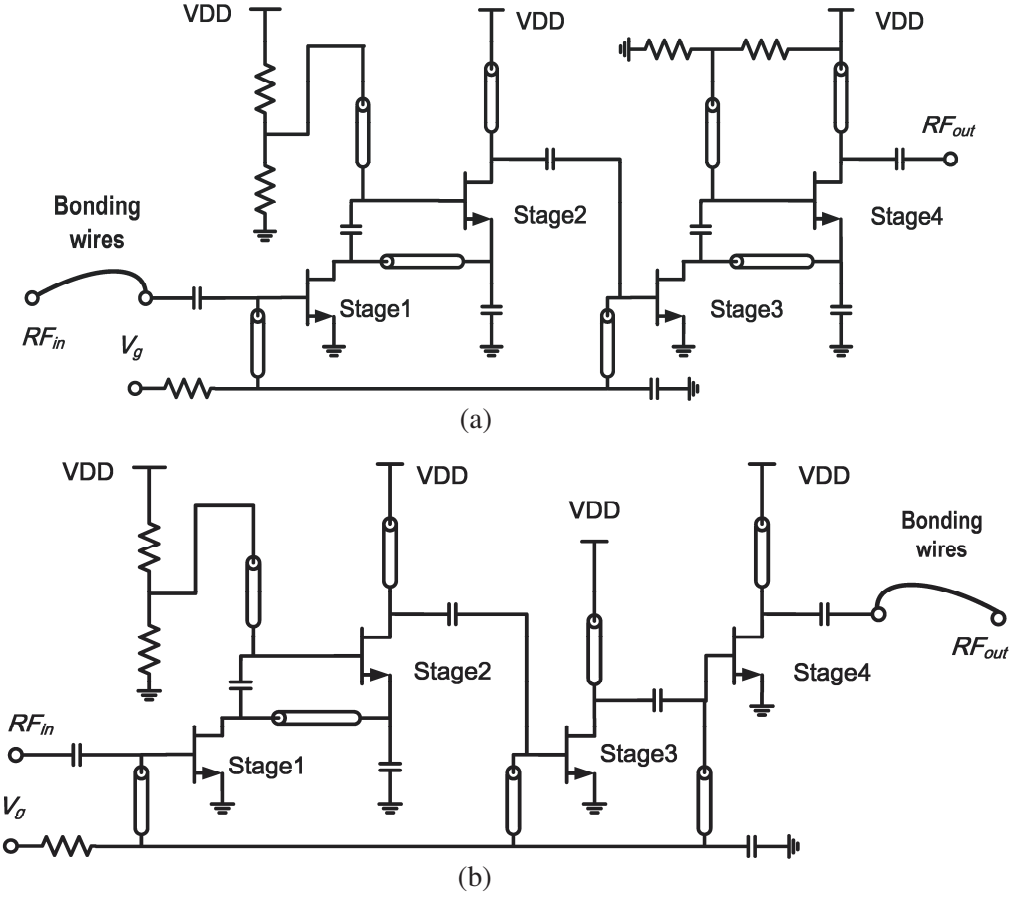

Figure 5. The schematic of amplifier in (a) receiver link and (b) transmission link.

the same as stage 3 and stage 4. The amplifier in transmission link is shown in Fig. 5(b). Stage 1 and stage 2 as the driver stages also share the same current. Stage 3 and stage 4 use the common source structure to get a high output power. The bias voltages are obtained from biasing network.

3.4. Chip 4

Chip 4 is a driver amplifier, which is used to generate enough power to drive the 30 dBm power amplifier. The schematic is shown in Fig. 6. It contains three stage common source amplifiers, and the final stage contains two transistors connected in parallel, which is able to output more than 20 dBm with 13 dB power gain. The transistor size of stages 1 and 2 is 4×50 μm, and each transistor in stage 3 is 6×50 μm.

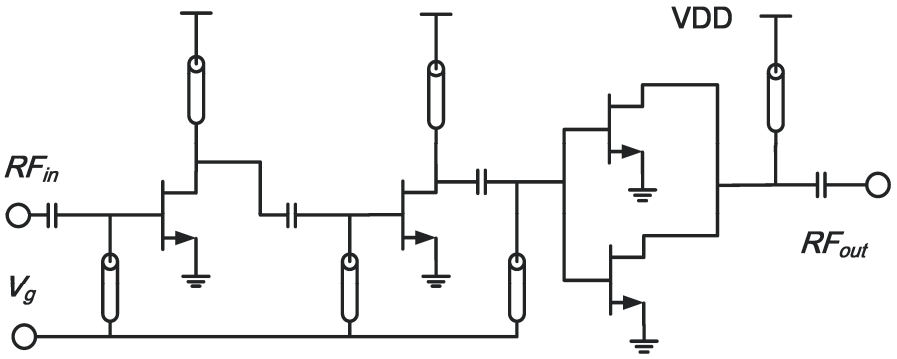

Figure 6. The schematic of driver amplifier in chip 4.

3.5. MEMS Filter

To suppress the image and spur signals, a millimeter-wave 5-order Chebyshev filter is designed. The filter is based on the gap coupling substrate integrated waveguide (SIW) units [9] as shown in Fig. 7. The size of the filter is 9.46 mm × 2 mm. The diameter of each hole is 0.1 mm with the pitch is 0.19 mm. Both ports of the filter are converted to CPW structure to connect with other chips. The SIW units use the metal through holes to form the equivalent metal waveguide, which has a better performance than the conventional microstrip line structure. The SIW units also have a stable performance versus temperature variation [10]. There are several alternative techniques to fabricate the filter, which are printed circuit board (PCB), Low Temperature Co-fired Ceramic (LTCC) and Micro-Electro-Mechanical System (MEMS). The machining precision of the PCB technology is not enough for the Microwave or Millimeter-wave filter. There is uncontrollable shrinkage in the LTCC process, especially in the z-direction, which will generates deviation and influence the filter's performance [11]. The MEMS technique is based on the silicon-substrate etching technique. The three-dimensional device can be realized on the silicon-substrate, which is able to achieve micrometer-accuracy and ensures the consistency. The high-resistivity silicon substrate is used, which has lower power loss than the low-resistivity silicon. The thickness of the substrate is 0.4 mm, while the metal thickness is 3 µm. The filter is a 5-order Chebyshev filter, which is based on the gap coupling unit. Both ports of the filter are converted to CPW structure to connect with other chips. The structure is shown in Fig. 7.

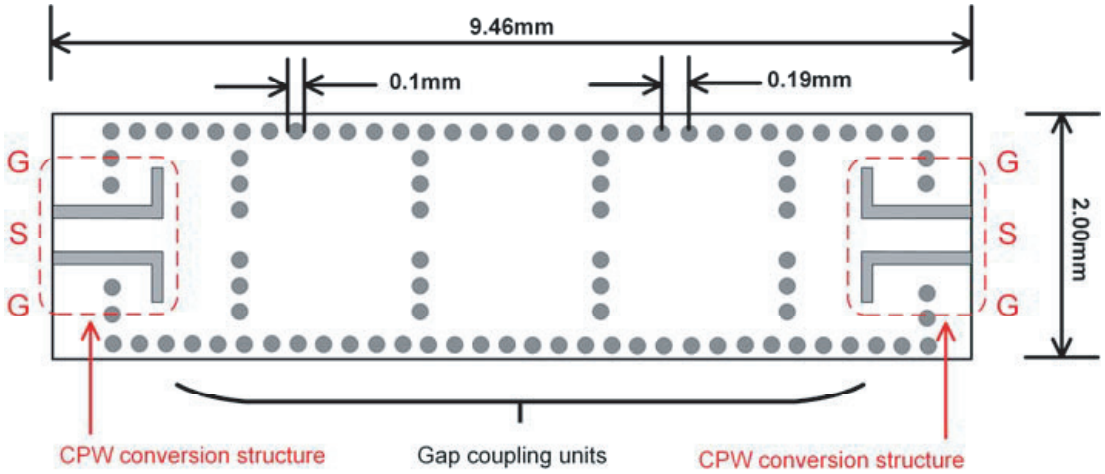

Figure 7. The structure of the MEMS filter.

3.6. Temperature Compensated Biasing Network

The biasing network generates the transistors' gate biasing voltage in each chip, which varies versus temperature to compensate the performance changing [1]. The biasing network consists a R_{Mesa} and a R_{TFR} as shown in Fig. 8. The R_{Mesa} has a positive temperature coefficient, while the R_{TFR} is opposite. With the negative supply voltage V_{SS}, the biasing voltage (V_g) increases with the temperature as shown in Fig. 9. The V_g is adaptive with the temperature, which compensates the performance variation of the transistors. By selecting proper ratio of the resistor, the variation of the circuit can be minimum. The resistor RG and Capacitor C_{decouple} form a low-pass filter to isolate the RF signal so as not to affect the biasing network.

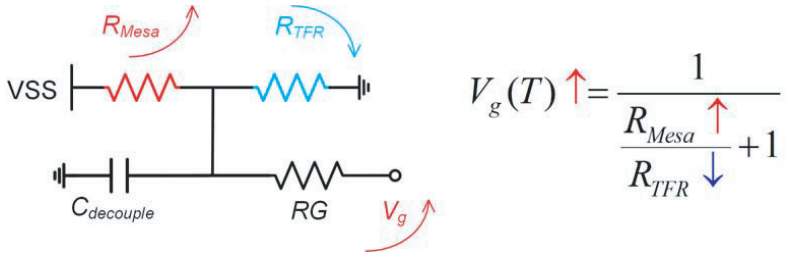

Figure 8. The schematic of the temperature compensated biasing network.

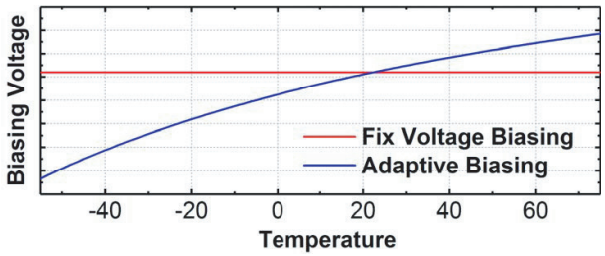

Figure 9. The biasing voltage versus temperature.

As mentioned above, all of the chips are interconnected using the bonding wire process as shown in the Fig. 10(a). The bonding wires have a great impact on the performance of circuits. Therefore, the interconnection bonding wires should be taken into consideration in the design. The characteristic of the bonding wires are usually simulated in the 3-D EM simulation software [12, 13]. However, it consumes a long time and large computer resources, which is more serious when multi-chips and dozens of bonding wires are assembled together. To reduce the simulation time and improve the convergence in the circuit simulator, the bonding wires are modeled by a lumped network as shown in Fig. 10(b). Typically, the diameter of the bonding wires is 25 μm and the length is around 500 μm. Therefore, a

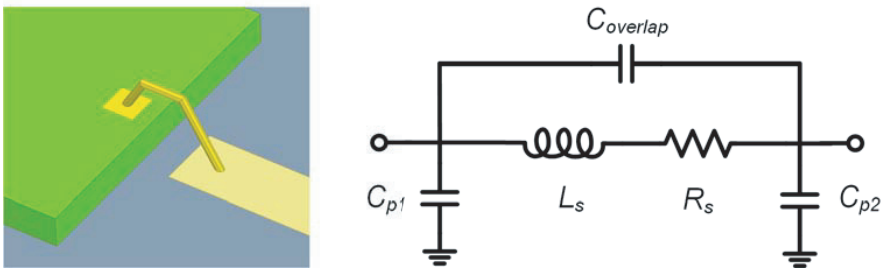

Figure 10. The schematic of the biasing network.

model containing a series inductor, a series resistor and parasitic capacitors is built [14]. It should be mentioned that the inductor in this lump model is used as an off-chip part of the matching networks of the designed chips, which has a better quality factor than the on-chip inductors [15].

4. PACKAGE

All chips are assembled in a compact cavity as shown in Fig. 11. All the high-frequency chips are pasted on the top of the module. The bottom of the module consists of the digital control circuit and the

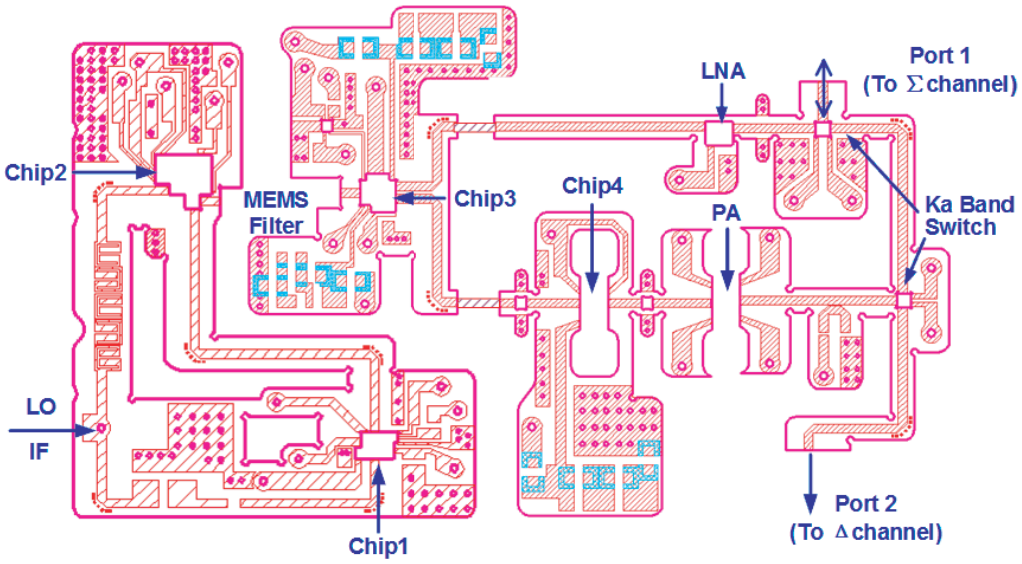

Figure 11. The top view of the layout of the system module.

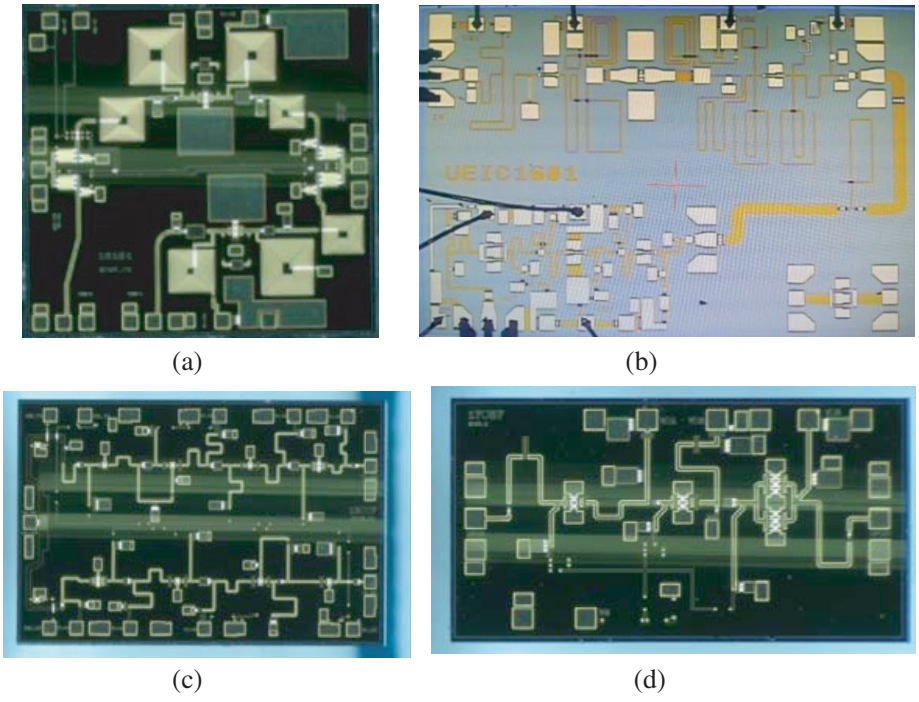

Figure 12. The top view of the layout of the system module.

power management chips. The power management chips convert the 28 V DC input voltage to several different levels, such as −5 V, 3.3 V and 5 V. High-frequency glass insulators are used to connect both of the sides. Port 1 and Port 2 are connected to the Ka-band waveguide terminals. Port 1 and Port 2 are connected to the $\sum$ channel and Δ channel, respectively, using the Ka-band waveguide terminals.

5. MEASUREMENT RESULT

Photos of chip 1 ∼ 4 are shown in Fig. 12. The size of the dies is 2.2 mm × 2.3 mm, 3.0 mm × 2.2 mm, 2.6 mm × 2.7 mm and 1.2 mm × 2.2 mm, respectively. Benefiting from the temperature compensated biasing network, the power gains of chip 1 at different temperatures are shown in Fig. 13. The variation is less than ±0.5 dB. Fig. 14 shows the output power of chip 2 at different temperatures, which is larger than 17.5 dBm in the working band. The power gain of chip 3 is shown in Fig. 15. Its harmonic waves suppression is more than 59 dBc, and the variation is less than ±1.75 dB. The performances of each chip versus temperature within the 400 MHz working bandwidth at 35.x GHz are measured and summarized in Tables 1 ∼ 4.

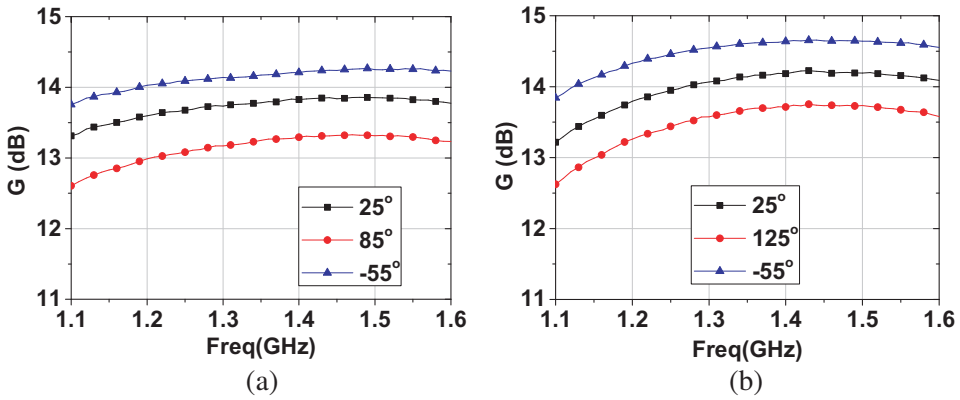

Figure 13. The power gain of the (a) RX link and the (b) TX link of the chip 1 versus temperature.

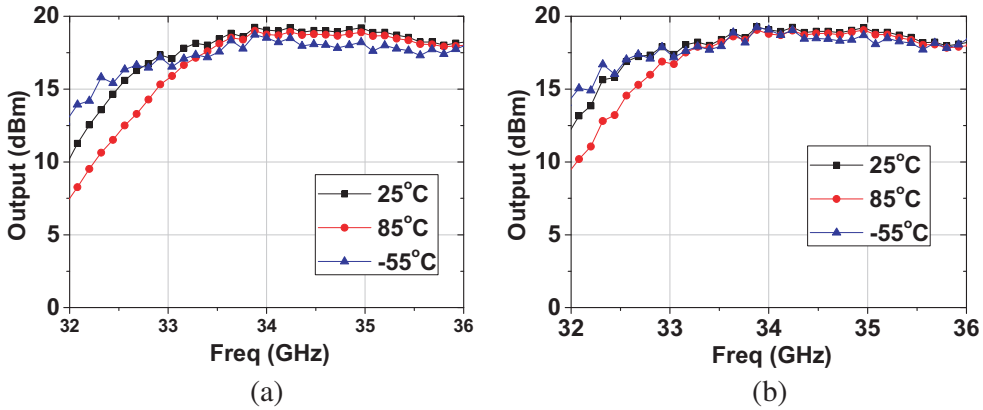

Figure 14. The output power of chip 2 at different temperature when (a) −5 dBm and (b) −2 dBm input power.

A photo of MEMS filter is shown in Fig. 16. The size of the filter is 9.7 mm × 2 mm. Its insertion loss is less than 4.2 dB, and the loss variation is less than ±0.4 dB. The out of band rejection is larger than 52 dBc. The measured and simulated S-parameters are shown in Fig. 17.

A photo of the system module is shown in Fig. 18. The output power of the transmitter system is larger than 30 dBm with fluctuation in band less than 1 dB. The measurement setup for the transmitter's output power is shown in Fig. 19(a). Since each chip's performance is stabilized by temperature

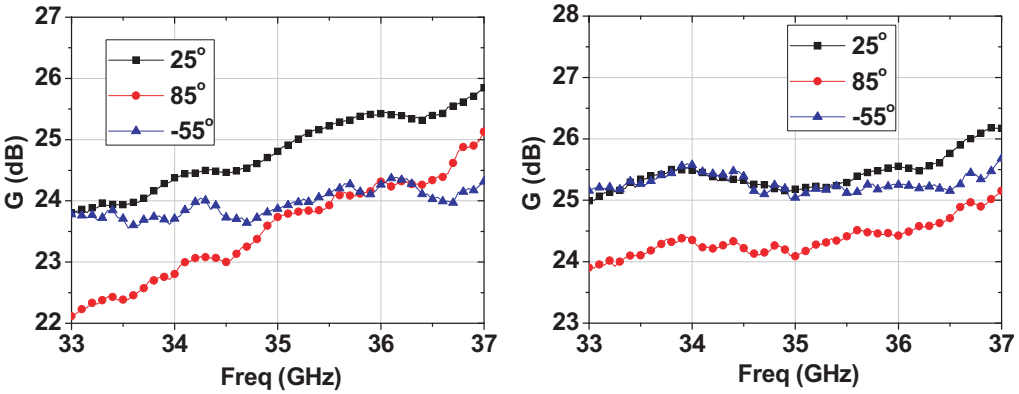

Figure 15. The power gain of the (a) RX link and the (b) TX link of the chip 3 versus temperature.

Table 1. Measurement result of Chip 1.

	−55°C	25°C	75°C	Variation
RX Gain (dB)	14.5	14.1	13.5	±0.50
RX OP1 dB (dBm)	14.0	14.0	13.5	±0.25
RX VSWR	1.43	1.45	1.44	±0.01
TX Gain (dB)	14.1	13.7	13.1	±0.5
TX OP1 dB (dBm)	14.5	15.0	15.0	±0.25
TX VSWR	1.32	1.34	1.36	±0.2
TR Isolation (dB)	32	32	31.5	±0.25

Table 2. Measurement result of Chip 2.

	−55°C	25°C	75°C	Variation
Output Power (dBm)	18	18.5	19	±0.50
f suppression (dBc)	67.5	69.0	71.0	±1.75
$2f$ suppression (dBc)	69.5	70.5	72.5	±1.50
$3f$ suppression (dBc)	60.0	59.0	59.0	±0.5

Table 3. Measurement result of Chip 3.

	−55°C	25°C	75°C	Variation
RX Gain (dB)	23.9	24.8	23.8	±0.5
RX OP1 dB (dBm)	12.1	12.0	12.5	±0.25
RX VSWR	1.51	1.55	1.53	±0.02
TX Gain (dB)	25.3	24.4	24.1	±0.6
TX OP1 dB (dBm)	15.5	16.0	15.2	±0.40
TX VSWR	1.47	1.41	1.45	±0.3

Table 4. Measurement result of Chip 4.

	−55°C	25°C	75°C	Variation
TX Gain (dB)	14.2	14.5	14.0	±0.25
TX P_{sat} (dBm)	20.8	20.6	20.5	±0.13
TX VSWR	1.4	1.5	1.6	±0.10

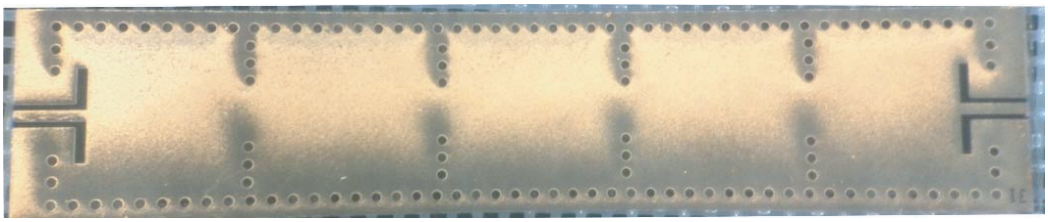

Figure 16. The photo of the MEMS filter.

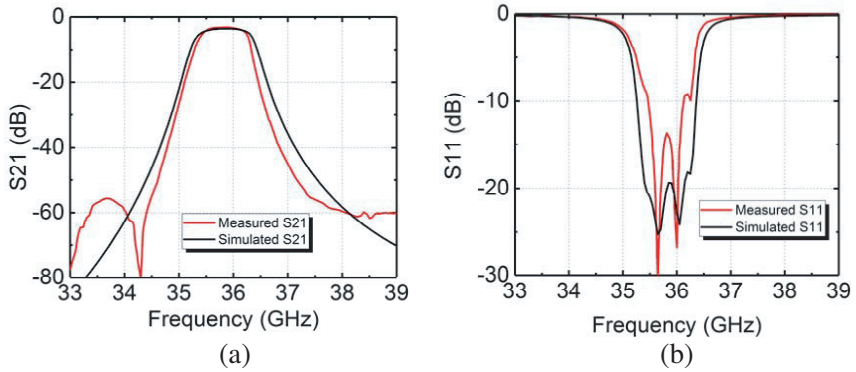

Figure 17. The measured and simulated (a) S_{21} and (b) S_{11}.

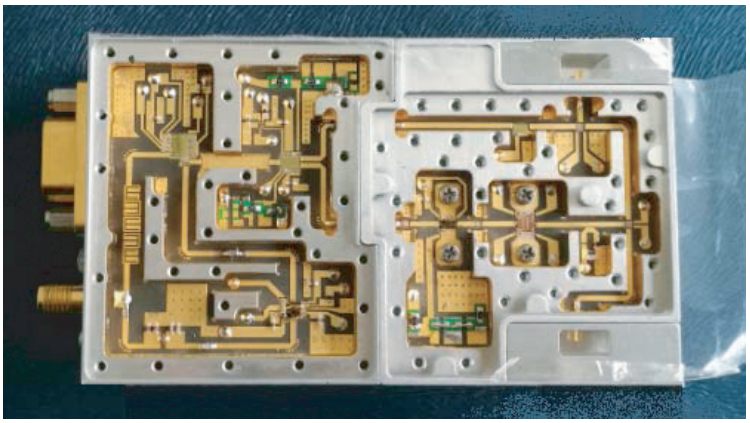

Figure 18. The photo of the system module.

compensated biasing network, the output power varies less than ±0.7 dB versus temperature in the working band as shown in Fig. 20(a). The output spur suppression is more than 42 dBc in all temperature ranges as shown in Fig. 20(a). The noise figure of the receiver is less than 3.7 dB at room temperature and less than 4.7 dB in all temperature ranges as shown in Fig. 20(b). The measurement setup for the

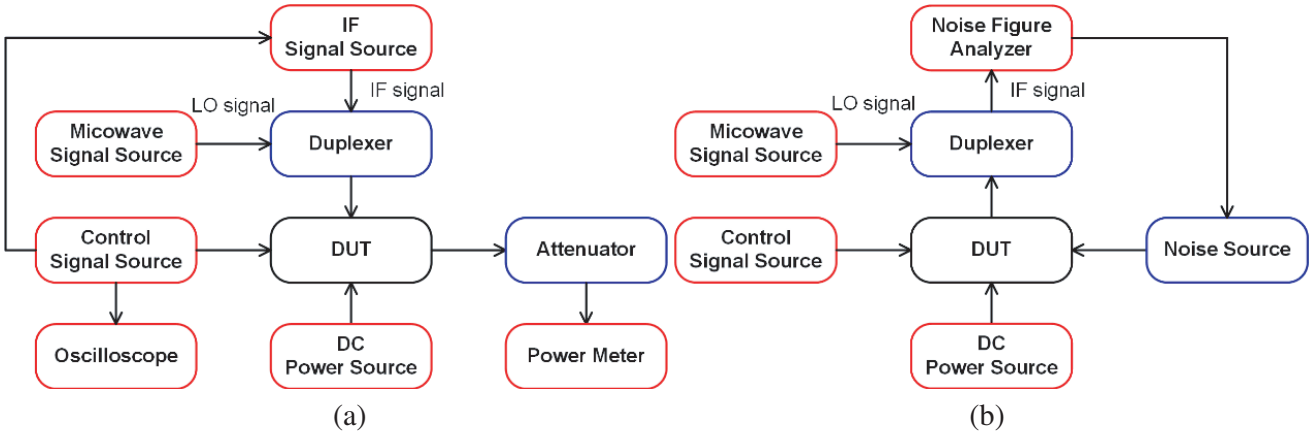

Figure 19. (a) The output power and output spur versus temperature in the transmitter. (b) The noise figure and power gain versus temperature in the receiver.

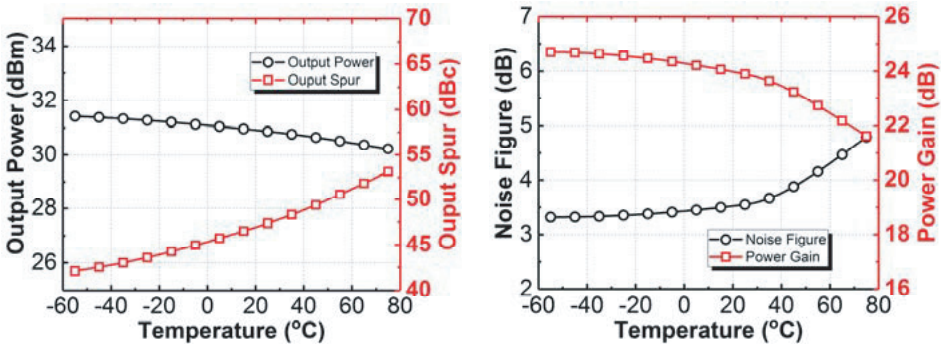

Figure 20. (a) The output power and output spur versus temperature in the transmitter. (b) The noise figure and power gain versus temperature in the receiver.

receiver's noise figure is shown in Fig. 19(b). The image rejection is larger than 43 dB. Its dynamic range is more than 60 dB with more than 21.9 dB power gain. The attenuator in the receiver link has temperature variation characteristic, which further stabilizes the power gain of the receiver. The attenuator can be controlled to adjust the power gain and output power of the receiver. The temperature compensated biasing network enables the amplifiers to work from $-55°$C to $+75°$C.

6. CONCLUSION

This paper presents a Ka-band compact transceiver module. Temperature compensated technique is adopted to stabilize the transceiver's performance versus temperature variation. Compact design with minimum ports is used to make the system suitable for the large-scale system application.

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