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# Power Performance and Spurious Frequencies Analysis of Composite Right-/Left-Handed (CRLH) Distributed Oscillators

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**Abstract**—This paper concerns the analysis of the performance of a Composite Right-/Left-Handed (CRLH) distributed oscillator. In order to increase its output power, a modification of the standard configuration is proposed. The basic idea is to combine the signals from the two output ports of the structure by means of a Wilkinson combiner, so obtaining a single output generator. The power performance of the conventional two output oscillator and the power performance of the new configuration are numerically compared by changing the number of employed transistors. The same procedure is adopted to analyze the amplitude of the higher order harmonics in the generated signals as a function of the number of active elements. On the basis of simulated data an increase of the output power, together with a second harmonic reduction, is expected for the single output oscillator with respect to the standard CRLH topology. Experimental results fully confirm these numerical predictions.

## 1. INTRODUCTION

Sinusoidal signal generation at microwave frequencies is a fundamental issue for communication systems working in this range. For this reason, in literature, both theoretical and design aspects of high frequency oscillators have been investigated. For these devices, in addition to the well-known topologies, a novel configuration has been presented in [1], obtained by inserting, in a distributed amplifier, a feedback element from the idle drain line port to the input gate line port. It is worth noting that the basic concept of travelling wave circuit has been used in the past not only for the signal amplification [2–4], but also for other kinds of processing, as for example the signal phase control [5]. Starting from [1], a number of papers have been published on distributed oscillators [6–11]. In a recent letter [12], a significant innovation has been proposed, replacing the low-pass network of the unit cell, with a CRLH (Composite Right-/Left-Handed) topology, as shown in Fig. 1(a). The output ports of the gate and drain lines are loaded by the impedance $Z_0$, and FTL is a positive feedback element consisting of a transmission line. In this circuit, each transistor supplies nearly the same amount of power, as demonstrated in [12]. This advantage cannot be obtained by using the conventional low-pass unit cells reported in [6, 10, 11]. Thus the oscillator provides two sinusoidal signals, $V_{outg}$ and $V_{outd}$, having a comparable power level. In microwave communication systems, high power signal sources are often needed [13]. The aim of this paper is to describe techniques for improving the output power of the CRLH oscillator. The first method consists of increasing the number of the active elements. In order to check the validity of this approach, the behavior of the output power from the gate and drain lines is studied as a function of the number of transistors. To this end, a commercial software package is used for the simulation of the oscillators. An interesting obtained result is the decrease of the output power for a number of active devices exceeding a certain value. Another method for realizing a high power oscillator is based on the use of a Wilkinson combiner, which adds the signals supplied by the

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gate and drain lines, thus creating a device with a single output (Fig. 1(b)). This solution can be adopted because of the strict phase control on the two output signals, inherently allowed by the CRLH topology. The numerical simulator is also used to investigate the higher order harmonic contributions in the output signal. A considerable reduction of the second harmonic has been found for the Wilkinson combiner oscillator. The organization of this paper is as follows. In Section 2, the design of the CRLH double output distributed oscillator, briefly discussed in [12], is presented more in detail. Section 3 concerns the transformation of this circuit in a single output signal generator. Section 4 is focused on the discussion of numerical and experimental results. In particular, simulations performed by means of a nonlinear software package are used to investigate the power performance of the oscillators as a function of the number of transistors. Furthermore, the experimental characterization of the fabricated circuits is presented. Finally, Section 5 is dedicated to summarize some conclusions.

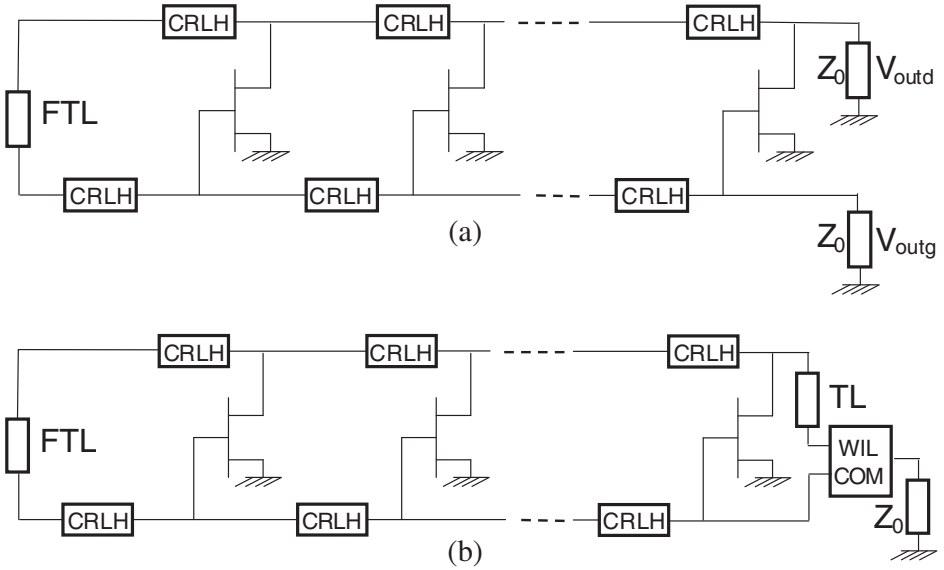


**Figure 1.** (a) The CRLH double output distributed oscillator. (b) The CRLH single output distributed oscillator.

## 2. DESIGN OF THE CRLH DOUBLE OUTPUT DISTRIBUTED OSCILLATOR

For the active elements in the oscillator, the MGF 4941AL InGaAs HEMT has been chosen. The model used for this transistor is the well-known lossless unilateral equivalent circuit typically adopted for the design of distributed amplifiers [2, 4], characterized by the gate and drain capacitances, $C_{gs}$ and $C_{ds}$, respectively. The topology of the CRLH unit cell is depicted in Fig. 2. Capacitances $C_{gs}$ and $C_{ds}$ are included in the series and parallel capacitors $C_s$ and $C_p$, respectively. In the following, we assume that the series and parallel resonators have the same resonance frequency (balancing condition), which is also the oscillation frequency $f_0$. Thus we have:

$$\frac{1}{\sqrt{L_s C_s}} = \frac{1}{\sqrt{L_p C_p}} = 2\pi f_0 \tag{1}$$

where $L_s$ and $L_p$ are the series and parallel inductors, respectively. Moreover, for such a basic cell, the characteristic impedance is usually defined in terms of $L_s$ and $C_p$. For this impedance, the value $Z_0$ is imposed, so obtaining:

$$\sqrt{\frac{L_s}{C_p}} = Z_0 \tag{2}$$

A key role, to turn the distributed amplifier into an oscillator, is played by the feedback element FTL. A uniform transmission line with characteristic impedance $Z_0$ and electrical length $\varphi$ is used to realize the

FTL component. In [12], it has been demonstrated that for having oscillations, the following condition must be fulfilled:

$$\varphi|_{f=f_0} = \pi \tag{3}$$

A very simple analysis of the structure can be developed considering that, at the resonance frequency $f_0$, each unit cell behaves as a short circuit. Therefore, the gate voltages of the transistors are all equal to each other. Hence the transistors provide the same value for the drain current, half of which is addressed to the drain output and half to the gate output, obtaining two sinusoidal signals having almost the same power level. The oscillator is designed in microstrip technology, on an RT/duroid 5870 substrate with thickness 1.575 mm, assuming: $f_0 = 2.8$ GHz, $C_{gs} = 0.43$ pF, $C_{ds} = 0.16$ pF. An essential step of the design procedure is the replacement of the lumped elements in the CRLH basic cell (Fig. 2) by means of transmission lines. To this end, the configuration depicted in Fig. 3 is adopted, where the parameters of the transmission lines (characteristic impedances $Z_1$ and $Z_2$, as well as the electrical lengths $\theta_g$, $\theta_d$, $\theta_1$, and $\theta_2$) are given numerically in the following. For the gate unit cell, the values for $C_{gs}$ and $\theta_g$ must be utilized, while $C_{ds}$ and $\theta_d$ must be utilized for the drain unit cell. Also, the significance of the capacitance $C_{pic}$ is clarified below. This solution for the gate and drain unit cell topology exhibits the following important features:

- inductors and chip capacitors are not needed;
- coupling effects between the gate circuit and the drain circuit are avoided;
- an interdigitated capacitor is used for the realization of the series resonator, and in its equivalent circuit there is also shunt capacitor $C_{pic}$;
- capacitor $C_p$ must include the effect of capacitors $C_{gs}$ and $C_{pic}$ for the gate circuit unit cell, and the effect of capacitors $C_{ds}$ and $C_{pic}$ for the drain circuit unit cell.

The electromagnetic IE3D-Zeland software package is used for the simulation of the interdigital capacitor. For such a component, with 10 fingers of 0.17 mm width and 8 mm length, spaced at 0.18 mm from each other, we find $C_s = 0.9$ pF, $L_s = 3.5$ nH, $C_{pic} = 0.64$ pF. These values of $C_s$ and $L_s$ fulfill Equation (1). By imposing Eqs. (2) and (1), we obtain: $C_p = 1.372$ pF, $L_p = 2.05$ nH. According to Fig. 3, the part of the circuit composed by capacitors $C_{gs/ds}$, $C_{pic}$ and by the transmission lines should replace the shunt connected admittance in Fig. 2. This result can be achieved by using, for the characteristic impedances and for the electric lengths of the transmission lines in Fig. 3, the values listed as follows: $Z_1 = 107\,\Omega$, $Z_2 = 70\,\Omega$, and at $f = f_0\theta_1 = 28°$, $\theta_2 = 84°$, $\theta_g = 6.2°$, $\theta_d = 18.6°$. To evaluate the validity of this proposed solution, the behaviors of the scattering parameters for the lumped CRLH cell, and for the unit cells with transmission lines of the gate circuit (Gate TL CRLH) and of the drain circuit (Drain TL CRLH), are plotted in Figs. 4(a) and 4(b). The agreement is remarkable in the range 2–4 GHz. Furthermore, it can be noted that at $f = f_0$ the phase of $S_{21}$ is zero for all the three analyzed configurations, as theoretically expected.

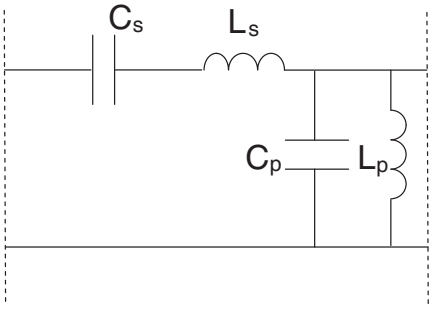


**Figure 2.** The CRLH unit cell for the gate and drain circuit.

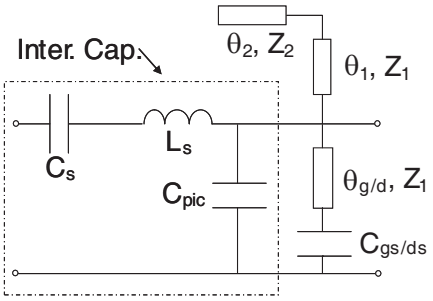


**Figure 3.** The configuration of the CRLH unit cell, proposed for the microstrip realization of both the gate circuit and the drain circuit.

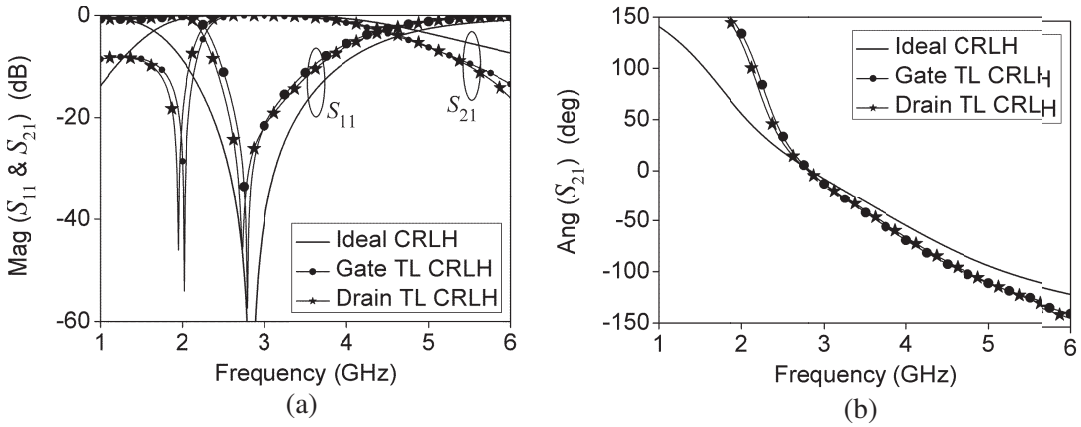


**Figure 4.** Scattering parameters versus frequency for the CRLH unit cells depicted in Fig. 3.

## 3. DESIGN OF THE CRLH SINGLE OUTPUT OSCILLATOR

The above presented oscillator generates two sinusoidal signals with the same power level. The aim of this section is to describe how it can be converted in a device providing a single signal with a higher power value. The basic idea is to connect the output ports of the oscillator to a 3 dB Wilkinson combiner. It is well known that this three-port component, if used as a divider, provides two signals with the same phase. To make it work as a combiner, a constructive interference is required, resulting in reciprocal reinforcement of the input signals. Thus the latter should have the same value for the phase. However, a simple analysis of the CRLH oscillator shows that this effect does not occur to its output signals. In fact, the drain current contribution produced by each transistor, addressed to the gate circuit, has to pass through the feedback element FTL. Furthermore, each unit cell cannot introduce a phase change, as demonstrated above. Therefore, according to Eq. (3), there is a difference of 180° between the phases of the outputs of the gate circuit and of the drain circuit. In order to have two signals with the same phase, at the input ports of the Wilkinson combiner, a transmission line section with characteristic impedance $Z_0$ and electric length 180° at $f = f_0$ is inserted between the drain circuit output port and the input port of the combiner (TL element in Fig. 1(b)).

## 4. RESULTS AND DISCUSSION

### 4.1. Numerical Simulation and Considerations on the Output Power

Both the distributed oscillators have been analyzed by the nonlinear simulator included in the Advanced Design System (ADS) — Keysight software package. In particular, the linear passive components present in each oscillator have been characterized by the momentum electromagnetic simulator, implemented in ADS. For the transistors the nonlinear model provided by the Mitsubishi company has been used. As discussed in the introduction, a key parameter controlling the power performance is the number of active devices ($N$) present in the circuit. Therefore, oscillators with different values of $N$ have been simulated. The power of the first harmonic from the output ports of the gate and drain lines, $P_{outg1}$ and $P_{outd1}$, respectively, are shown in Fig. 5 as a function of $N$. For the sake of completeness, output powers of the second harmonic at the output gate and drain ports, $P_{outg2}$ and $P_{outd2}$, respectively, are depicted in Fig. 6, for different values of $N$. The values of the power for the first and second harmonics at the output of the Wilkinson combiner, $P_{outc1}$ and $P_{outc2}$, respectively, are also plotted in the same figures for the single output oscillator topology. The main considerations suggested by the presented results can be summarized as follows:

a) The $P_{outg1}$ curve exhibits a maximum value. This behavior can be explained by the fact that the amplitude of the signal propagating on the gate line decreases because of losses. This effect is exceeded, for low values of $N$, by the power provided by the added active elements. However, for large values of $N$, the transistors close to the end of the oscillator receive a very low input signal,

and thus cannot compensate the losses. The same effect should be present in the $P_{outd1}$ curve, but for a higher value of $N$. In fact, in this case the signals from the added transistors have to pass through a quite short transmission line section for arriving at the drain output port.

b) The difference between $P_{outg1}$ and $P_{outd1}$, negligible for low value of $N$, becomes quite big by increasing this parameter.

c) For a fixed value of the required output power, the use of the Wilkinson combiner allows to reduce the number of active devices. In fact, we have $P_{outd1} = 11.2$ dBm with $N = 3$, but a slightly higher value can be obtained for $P_{outc1}$ with $N = 2$. Even more, $P_{outd1} = 13.6$ dBm for $N = 5$, and the same value is provided by $P_{outc1}$ with $N = 3$.

d) Since $P_{outc2}$ values are at least 5 dB lower than $P_{outd2}$, the single output oscillator exhibits a remarkable reduction of the second harmonic contribution in the output signal.

To assess the validity of the simulations, a comparison with experimental results for oscillators with $N = 3$ will be presented in the next section. The expected oscillation frequency is 2.833 GHz.

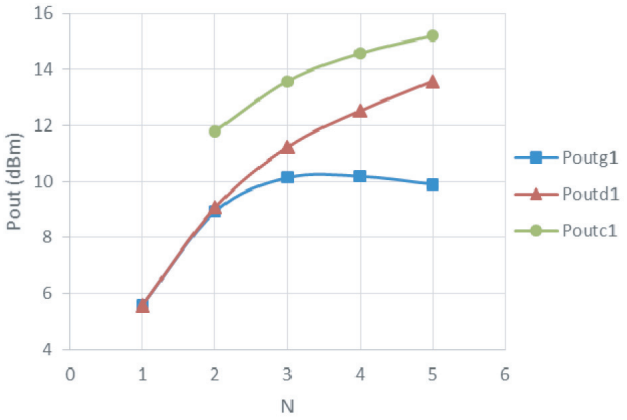


**Figure 5.** First harmonic output powers versus number of transistors for the two configurations of CRLH distributed oscillators.

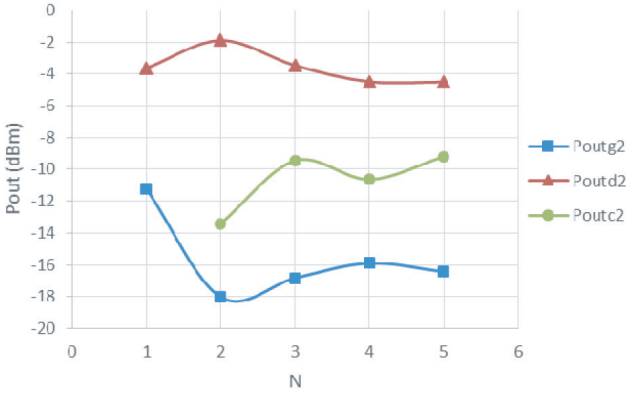


**Figure 6.** Second harmonic output powers versus number of transistors for the two configurations of CRLH distributed oscillators.

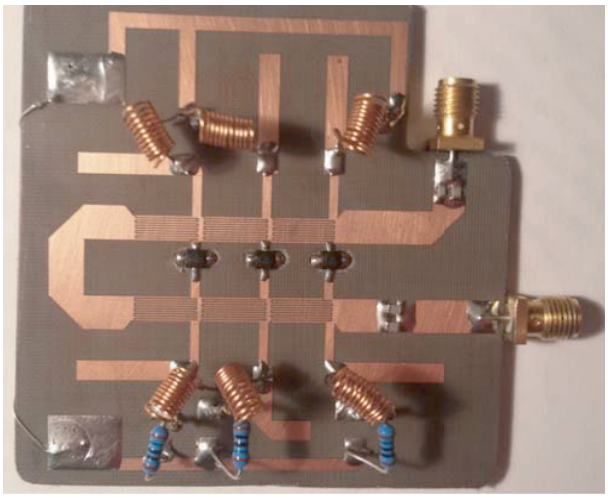

**Figure 7.** Photograph of the realized CRLH double output distributed oscillator.

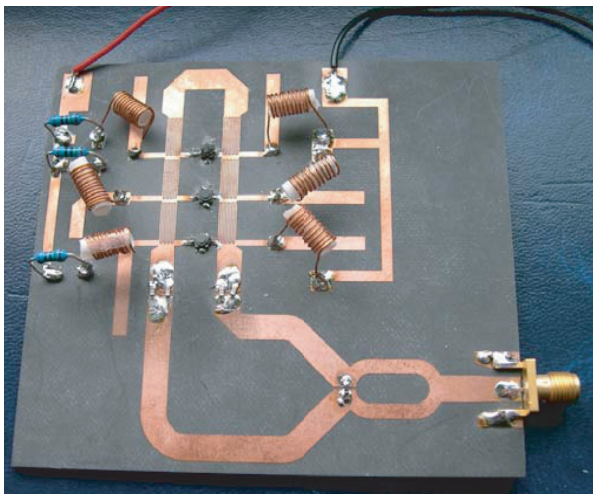

**Figure 8.** Photograph of the realized CRLH single output distributed oscillator.

### 4.2. Experimental Characterization of the Realized Distributed Oscillators

The manufactured distributed oscillators are shown in Figs. 7 and 8. The characterization of the realized circuits has been achieved by means of the Agilent E4448A spectrum analyzer. In Figs. 9 and 10, the frequency spectra of the output signals for the oscillator in Fig. 7 are plotted. For the configuration in Fig. 8, the frequency spectrum of the generated signal is depicted in Fig. 11. For convenience of the reader, the measured data in terms of power values for the harmonics of both the oscillators are summarized in Table 1. The increase in power (i.e., the difference $P_{outc,1} - P_{outd,1}$) is 1.97 dBm, with a good agreement with the simulated result. Furthermore, we can note that the power of the second harmonic is lowered from $-2.13$ dBm ($P_{outd,2}$) to $-14.14$ dBm ($P_{outc,2}$). It is worth noting that a distributed oscillator composed by four transistors has been presented in [6], with an output power of 2.63 dBm and working frequency of 3 GHz.

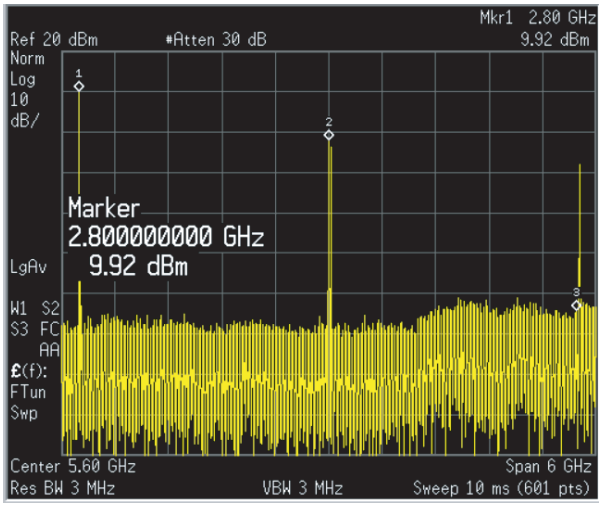


**Figure 9.** Measured frequency spectrum of the drain line output signal for the double output oscillator.

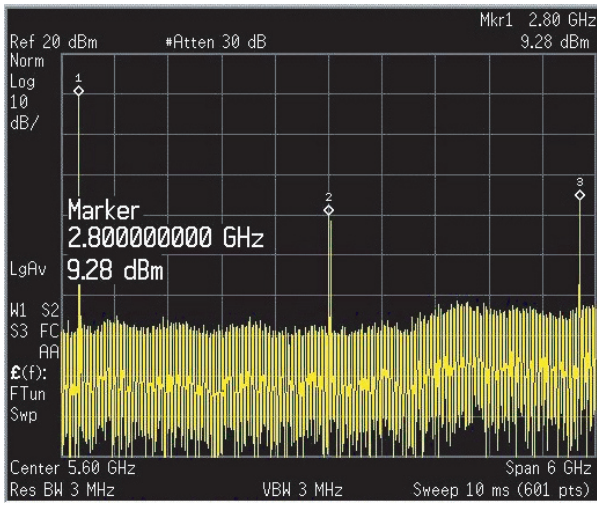


**Figure 10.** Measured frequency spectrum of the gate line output signal for the double output oscillator.

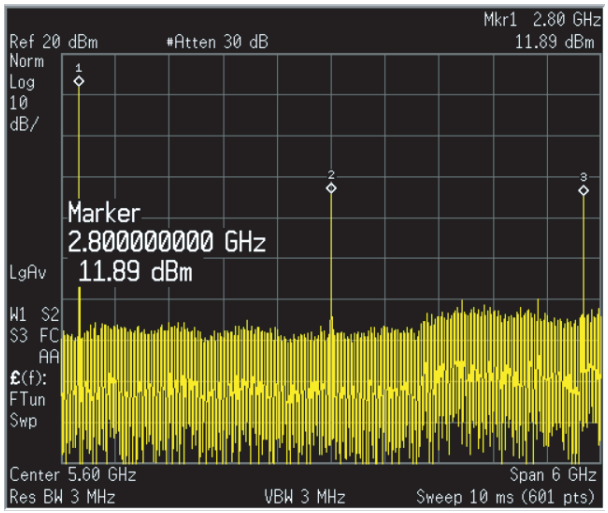


**Figure 11.** Measured frequency spectrum of the output signal for the single output oscillator.

**Table 1.** Comparison of the measured output powers for the fabricated oscillators.

| Output Power (dBm) | first harmonic $i = 1$ | second harmonic $i = 2$ | third harmonic $i = 3$ |
|---|---|---|---|
| $P_{outg,i}$ | 9.28 | −19.97 | −16.65 |
| $P_{outd,i}$ | 9.92 | −2.13 | −8.07 |
| $P_{outc,i}$ | 11.89 | −14.14 | −14.62 |

## 5. CONCLUSION

The power performance of two configurations of CRLH distributed oscillators have been analyzed as a function of the number of employed active devices. Numerical data for simulated structures feature an output power improvement at fundamental frequency and a substantial lowering of the second harmonic in the signal generated by the single output topology. Two distributed oscillators were realized (i.e., double and single output configurations) composed by three transistors. For the single output topology, an increase of 1.97 dBm for the first harmonic output power has been measured, together with a decrease about 12 dBm for the second harmonic, with respect to the conventional double output oscillator.

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