Progress In Electromagnetics Research C, Vol. 82, 67–76, 2018

A Novel Compact Size Wilkinson Power Divider with Two Transmission Zeros for Enhanced Harmonics Suppression

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Abstract—This paper presents a novel compact Wilkinson Power Divider (WPD) that improves harmonics suppression. The proposed WPD consists of a shunt open stub between two series similar inductors, and a microstrip line between an isolation resistor and each output port. This configuration acts as a low-pass filter with two transmission zeros. In addition, it facilitates manufacturability by using lower transmission line impedance values than conventional structures. Through even and odd mode analysis, the general design equations have been derived in closed form. A 2 GHz microstrip WPD is designed, fabricated and measured based on the proposed technique. A great agreement has been obtained between the measured performance of fabricated WPD circuit and the simulation results. The measured results show that the second and third harmonic levels are about −46 dB and −36 dB, respectively. The proposed design has about 40% reduction in size better than conventional WPD. It achieves competing results compared to other published work.

1. INTRODUCTION

Power dividers/combiners are very important parts representing fundamental components for microwave systems that facilitate the input for composing feeding networks for an array of antennas and high power amplifier sections. The major advantage of a conventional WPD is its good isolation between output ports and good matching at all ports. However, its major drawback is the presence of spurious responses due to quarter-wavelength transmission lines that increase the overall system nonlinearity [1]. Power dividers opportune solutions, present in literature, have been conceived to reach particular requirements such as low passive intermodulation distortion (PIM), compact size, wide bandwidth, and multi-band operations.

Recently, many researches are focused on minimizing the size and improving the harmonics suppression of power dividers using different techniques. Electromagnetic Band Gap (EBG) cells that exhibit band-stop and slow-wave characteristics are used in [2], but this technique faces some difficulties in modelling and fabrication since it relies on high resolution.

The technique of Defected Ground Structure (DGS), in [3, 4], depends on band stop characteristics, and it is easier than electromagnetic band gap in fabrication and equivalent circuit modelling, but its structure dimensions need design formulae, and their proper values are obtained iteratively. In addition, it needs backside etching. In [5], Defected Microstrip Structure (DMS) is used to prevent the leakage current through ground plane such as DGS, but it needs high resolution in fabrication. Planar artificial transmission line is presented in [6], High-low impedance resonator cells in [7], and Slow-wave structure in [8] which depends on reducing the group velocity of the propagated waves. All of the above techniques are based on intensive 3D EM simulations, while this paper adopts circuit analysis techniques having an advantage of providing helpful design equations and more precise results with reduced computational efforts.

Received 26 November 2017, Accepted 26 February 2018, Scheduled 13 March 2018
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On the other hand, some circuit-based designs utilizing stepped impedance transmission lines are introduced in [9, 10], but they depend on circuit optimization process and on shifting the spurious passband to other higher frequencies. In addition, other circuit-based designs rely on extra stubs and transmission lines as in [11, 12]. Since these designs depend only on microstrip lines, the post fabrication tuning is not possible to overcome the deviation between measured and required response if any. Therefore, lumped elements are presented, which play extra important roles in miniaturization and harmonic suppression such as capacitive loaded [13] and inductive loaded-based designs [14, 15].

In this paper, the inductor loaded design is adopted with the addition of two transmission zeros to improve the harmonic suppression performance by utilizing extra stub and a transmission line. Through even and odd mode analysis, the general design equations have been derived in closed form with the advantage of choosing the harmonic order which are required to be suppressed to suppressed [13] as in Section 2. Based on the derived equations, a design flows as well as design curves are proposed to facilitate the calculation-to-fabrication procedure, in Section 3. A 2 GHz microstrip WPD is designed, fabricated and measured to verify the proposed technique and show its advantages over other recent work as in Sections 4 and 5.

2. EVEN- AND ODD-MODE ANALYSIS

The quarter wave length 70.7 Ω microstrip line in the conventional WPD is replaced by two inductors (L) and a shunt open stub (Z_{st}, θ_{st}) in the proposed design. Furthermore, the 100-Ω isolation resistor is replaced by a microstrip line (Z_2, θ_2) and lumped resistor (R) as shown in Fig. 1. Thus, the proposed open stub and the transmission line can be utilized to add two transmission zeros in order to suppress the higher harmonics. Therefore, the electrical lengths (θ_{st} and θ_2) of both elements can be determined by means of the chosen frequency to be suppressed f_z as follows:

$$\theta_2 = \frac{\pi}{2n} \;\&\; \theta_{st} = \frac{\pi}{2n} \tag{1}$$

where

$$n = \frac{f_z}{f_0} = 1, 2, 3, \ldots \tag{2}$$

$$\theta_{st} = \frac{2\pi L_{st}}{\lambda} \;\&\; \theta_2 = \frac{2\pi L_2}{\lambda} \tag{3}$$

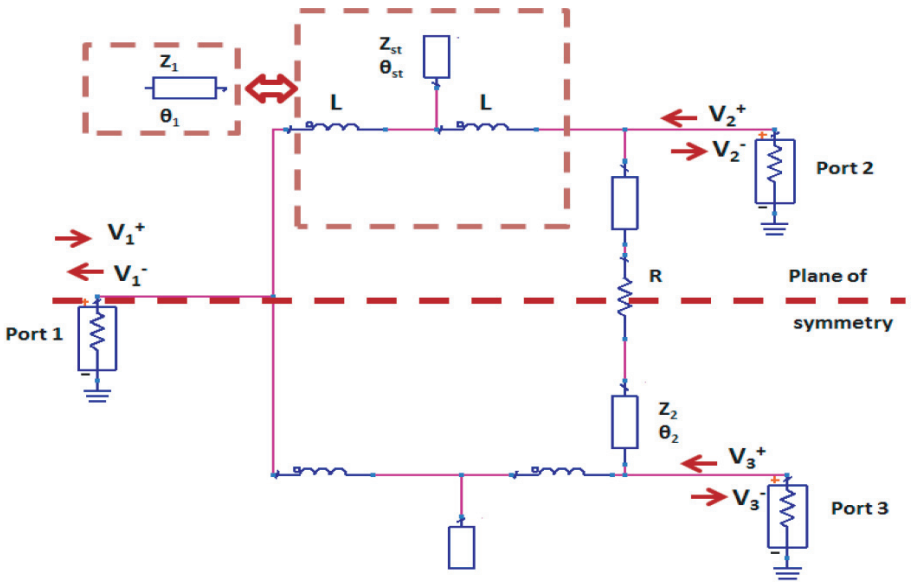


Figure 1. The proposed miniaturized WPD with two transmission zeros.

where L_{st} and L_2 are the physical lengths of open stub and microstrip line Z_2, respectively.

Firstly, for simplicity, one assumes that the two series inductors and shunt open stub are equivalent to transmission line Z_1 and θ_1 in two square dashed as shown in Fig. 1. The modeling starts with even analysis as shown in Fig. 2 to obtain Z_1 and θ_1.

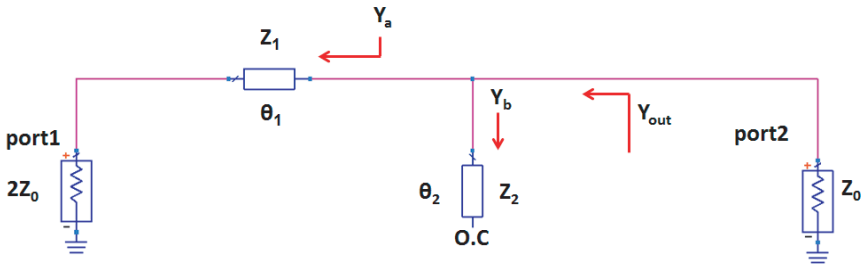


Figure 2. Equivalent circuit for even mode analysis of the proposed design.

The output ports matched to characteristic impedance admittance Y_{out} equal y_0;

$$Y_{out} = Y_a + Y_b \tag{4}$$

$$Y_a = \frac{y_0 y_1 + j y_1^2 \tan\theta_1}{2y_1 + j y_0 \tan\theta_1} \tag{5}$$

$$Y_b = j y_2 \tan\theta_2 \tag{6}$$

where

$$\theta_1 = \frac{2\pi L_1}{\lambda} \tag{7}$$

$$Y_{out} = y_0 = \frac{y_0 y_1 + j y_1^2 \tan\theta_1}{2y_1 + j y_0 \tan\theta_1} + j y_2 \tan\theta_2 \tag{8}$$

Equating real and imaginary parts in Equation (8) deduces that:

$$-\frac{Z_2}{Z_1} = \tan\theta_2 \tan\theta_1 \tag{9}$$

$$1 - \frac{y_0 Z_1^2}{2} = \frac{y_0^2}{\tan^2\theta_1} \tag{10}$$

Substituting Equation (9) in Equation (10) obtains:

$$Z_1 = Z_0 \bar{Z}_2 \sqrt{\frac{2}{\bar{Z}_2^2 + 2\tan^2\theta_2}} \tag{11}$$

$$\theta_1 = \pi - \tan^{-1}\left(\frac{Z_2}{Z_1 \tan\theta_2}\right) \tag{12}$$

In odd-mode analysis, the equivalent circuit can be redrawn as shown in Fig. 3 to obtain isolation resistor R and microstrip line impedance Z_2 which is responsible for the second transmission zero. The total output admittance must equal y_0, and it can be expressed as:

$$Y_{out} = Y_c + Y_d \tag{13}$$

where:

$$Y_c = -j y_1 \cot\theta_1 \tag{14}$$

$$Y_d = \frac{G y_2 + j y_2^2 \tan\theta_2}{y_2 + jG \tan\theta_2} \tag{15}$$

$$Y_{out} = y_0 = \frac{G y_2 + j y_2^2 \tan\theta_2}{y_2 + jG \tan\theta_2} - j y_1 \cot\theta_1 \tag{16}$$

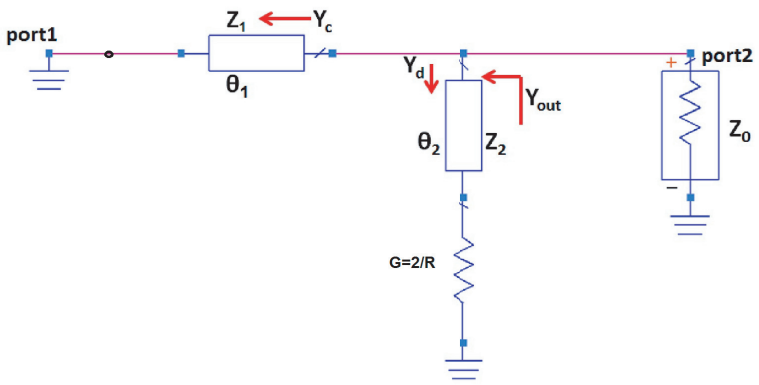


Figure 3. Equivalent circuit for odd mode analysis.

By equating the real and imaginary parts of Equation (16) we get

$$G = \frac{y_0}{1 - \tan^2 \theta_2} \tag{17}$$

From Equations (16) and (17) R and Z_2 can be calculated as:

$$R = 2Z_0 \left(1 - \tan^2 \theta_2\right) \tag{18}$$

$$Z_2 = Z_0 \sqrt{2\left(1 - \tan^2 \theta_2\right)} \tag{19}$$

Equations (18) and (19) indicate that the lumped resistance and impedance value of the extra-transmission line depend only on its electrical length.

Finally, $ABCD$ matrix is used to equate the inductor and stub T network with its equivalent circuit Z_1 and θ_1 of Fig. 1, obtaining design equation for the inductor and stub impedance.

The $ABCD$ matrix of series inductor "L":

$$M_1 = \begin{pmatrix} 1 & -j\omega L \\ 0 & 1 \end{pmatrix} \tag{20}$$

The $ABCD$ matrix of the microstrip line z_1 is:

$$M_{\text{total}} = \begin{pmatrix} \cos\theta_1 & jz_1 \sin\theta_1 \\ jy_1 \sin\theta_1 & \cos\theta_1 \end{pmatrix} \tag{21}$$

The $ABCD$ matrix of shunt stub z_{st} is:

$$M_{st} = \begin{pmatrix} 1 & 0 \\ jy_{st} \tan\theta_{st} & 1 \end{pmatrix} \tag{22}$$

$$M_{\text{total}} = M_1 M_{st} M_1 = \begin{pmatrix} 1 + \omega L y_{st} \tan\theta_{st} & -2j\omega L - j\omega^2 L^2 y_{st} \tan\theta_{st} \\ jy_{st} \tan\theta_{st} & 1 + \omega L y_{st} \tan\theta_{st} \end{pmatrix} \tag{23}$$

By equating elements of the two matrices in Equations (21) and (23) we deduce that:

$$\cos\theta_1 = 1 + \omega L y_{st} \tan\theta_{st} \tag{24}$$

$$z_1 \sin\theta_1 = -2\omega L - \omega^2 L^2 y_{st} \tan\theta_{st} \tag{25}$$

$$y_1 \sin\theta_1 = y_{st} \tan\theta_{st} \tag{26}$$

From Equations (24) and (26), we get:

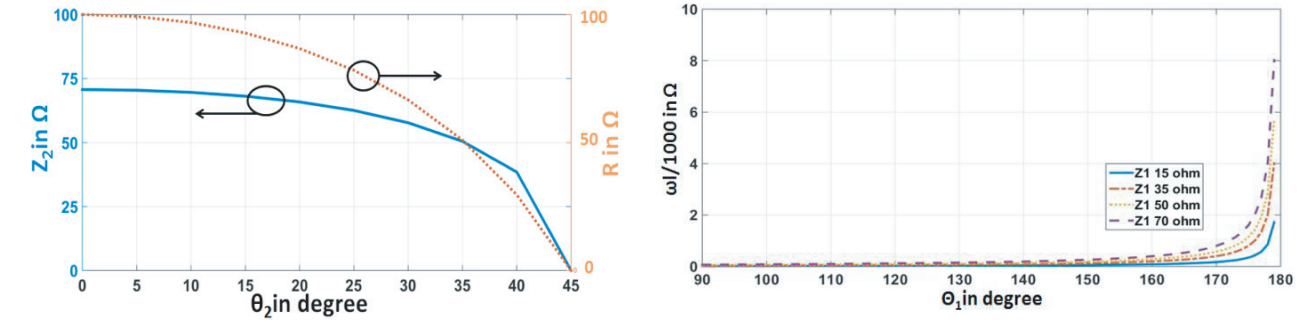
$$z_{st} = \frac{z_1 \tan\theta_{st}}{\sin\theta_1} \tag{27}$$

$$\omega L = \frac{z_{st} \left|\cos\theta_1 - 1\right|}{\tan\theta_{st}} \tag{28}$$

Therefore, the inductor as well as the stub line can be designed based on Equations (27) and (28). The next section describes the utilization of these equations in a proposed design algorithm. These are the closed form equations used to achieve the proposed design based on direct calculations rather than circuit optimization or 3D EM simulation.

3. PROPOSED DESIGN FLOW

Based on the derived equations in the previous section, Fig. 5 helps designers to calculate circuit parameters. The design curves of Fig. 4(a) can be used to determine the impedance of Z_2 and isolation resistor R depending on the chosen electrical length θ_2. The available lumped inductors are always restricted to certain values in the standard kits. Thus, the design curve of Fig. 4(b) can be used to choose appropriate reactance value based on certain inductor kit to obtain impedance Z_1 and its electrical length θ_1.



(a) (b)

Figure 4. Design curves (a) Z_2 and isolation resistor versus θ_2, (b) reactance versus θ_1.

Starting from the circuit specification such as fundamental frequency, harmonics order required to be suppressed and available substrate parameters, the design flowchart illustrated in Fig. 5 gives the designer main guidelines to reach a complete design achieving certain desired response. The flowchart gives the designer some degree of freedom to choose different circuit parameters suitable for manufacturing facilities and inductors values in the available standard kits. A small code could be written easily based on this proposed algorithm for automating the circuit design by some initial guess for the inductor values from the available design kits. The termination from this loop is obtained by the easily fabricated stubs based on the available substrates.

4. A 2 GHZ MODIFIED WPD BASED ON THE PROPOSED DESIGN

4.1. Initial Design and Calculations

To demonstrate the proposed design technique, a WPD has been designed at centre frequency of 2 GHz by applying the algorithm discussed above. The shunt open stub and the extra-transmission line are dedicated for the 2nd and 3rd harmonics suppression, respectively. The designed circuit has been

Table 1. Calculated design parameters using the proposed technique.

Parameter	Impedance (Ω)	Electrical length (deg.)	Physical width (mm)	Physical length (mm)
Z_2	57.7	30	1.8	9.1
Z_{st}	52.3	45	2.1	13.7
Z_0	50	10	2.3	3
R	66.7	—	—	—

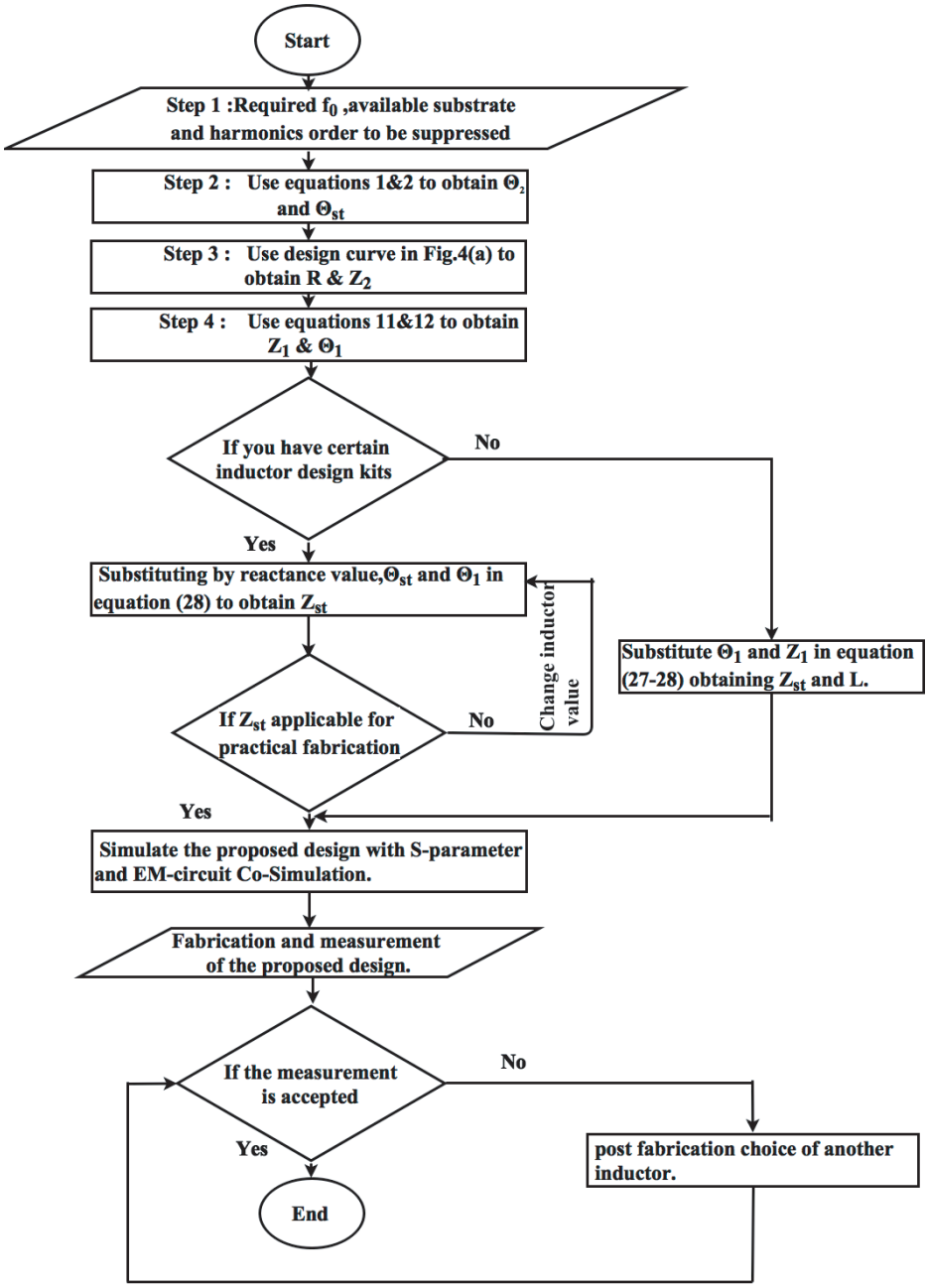


Figure 5. Flow chart of the proposed design methodology.

fabricated on a Rogers' RT/Duroid 5880 substrate with a dielectric constant of 2.2, thickness of 0.787 mm and loss tangent of 0.0009.

Using Equations (1) and (2), the electrical lengths are calculated ($\theta_2 = 30°$, $\theta_{st} = 45°$). From Fig. 4(a), R and Z_2 can be obtained as 66.7 Ω and 57.7 Ω, respectively. The details of obtained circuit parameters are illustrated in Table 1, while the used lumped inductor ($L = 5.6$ nH) is selected from one of the available standard design kits such as EPCOS (TDK). Z_{st} can be determined from Eq. (28) as 52.3 Ω. Z_{st} and Z_2 are found to be applicable as shown in Table 1. It is worth to note that some guess values of L should be chosen in order to obtain realizable stubs. For example, if $L \geq 20$ nH is chosen, an impedance of $Z_{st} \geq 160\,\Omega$ ($W \leq 140\,\mu$m) will be obtained which is not realizable based on the available facility or needs high resolution to be implemented using this substrate. Therefore, the proposed algorithm is used, and the circuit is ready to be simulated as follows.

4.2. Circuit Simulation

In order to verify the proposed design technique, the Advanced Design System (ADS) from Keysight Tech. is used. An S-parameter simulation has been applied to the schematic circuit of the modified WPD developed in Fig. 6(a), based on the calculated parameters of Table 1. The simulation results are shown in Fig. 6(b) where it can be noticed that the designed circuit satisfies all of the desired specifications with excellent suppression for the 2nd harmonic (at 4 GHz) and 3rd harmonic (at 6 GHz) with 52 dB and 58 dB, respectively.

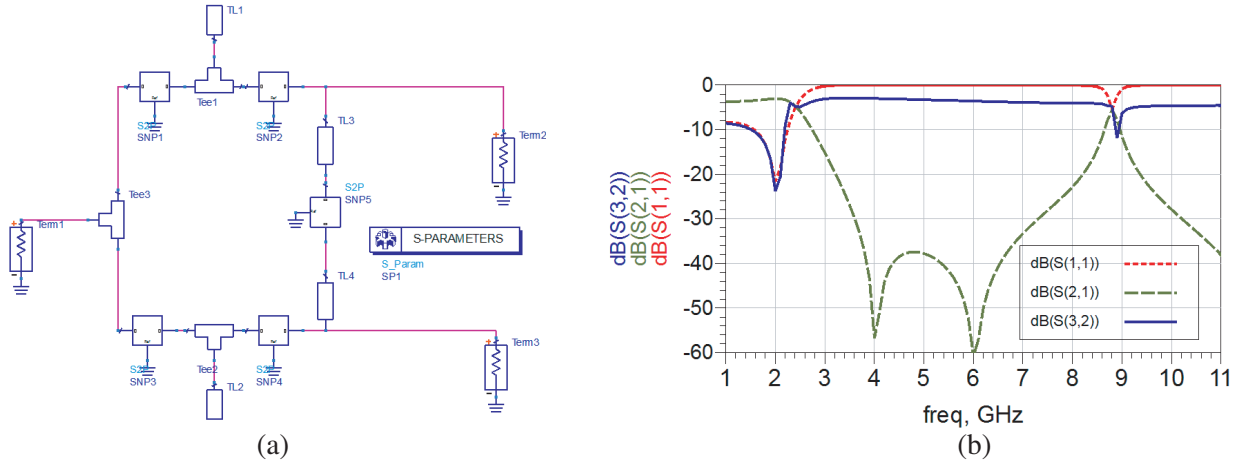


Figure 6. (a) Schematic circuit of the designed WPD, (b) S-parameters simulation results.

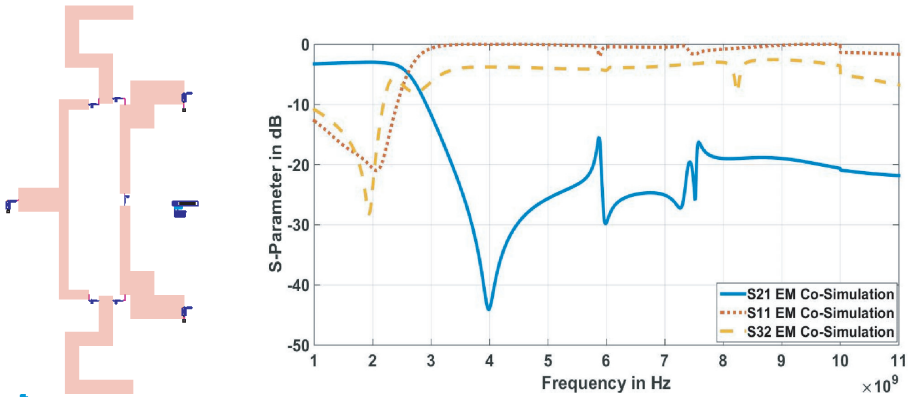
Indeed, lumped and distributed components suffer from manufacturing tolerances. Therefore, it is necessary to study manufacturing tolerances affecting the circuit performance. Monte Carlo simulation is applied with ±5% tolerance in inductor and resistor values, and about ±5% photolithographic tolerance in length and width of microstrip lines. Monte Carlo yield analyses are obtained by adjusting certain yield specification for S-parameter within bandwidth from 1.9 GHz to 2.1 GHz. Variation of S_{21} is adjusted from −3 to −3.5 dB, S_{32} better than −10 dB, and S_{11} better than −10 dB. Moreover, the second and third harmonics can be accepted lower than −30 dB with 100 MHz bandwidth. The number of samples to be simulated is 2000. Numbers of passed and failed samples are as shown in Fig. 7. The passed samples represent 95.05% which can achieve S-parameters and Harmonic Isolation specifications within the acceptable range as specified above. This verifies that the proposed design is insensitive to fabrication and component tolerances.

Yield	NumFail	NumPass
95.050	99.000	1901.000

Figure 7. Yield simulation results showing numbers of pass and fail samples.

4.3. Layout and EM-Circuit Co-Simulation

The layout of the designed circuit has been generated by the ADS software package, and an EM circuit Co-Simulation has been applied to the generated layout as shown in Fig. 8(a). The EM circuit Co-Simulation results are shown in Fig. 8(b) from which it can be seen that an accurate power division is achieved over the frequency band of interest (up to 2.2 GHz), $S_{21} = S_{31} = -3.1$ dB. In addition, a very good reflection coefficient, better than −10 dB, is obtained at the input port, and pretty good isolation, reaching −20 dB, is achieved between the output ports with minimal frequency shift. Moreover, a very good suppression of −47 dB for the 2nd harmonic and −32 dB for the 3rd harmonic are obtained.



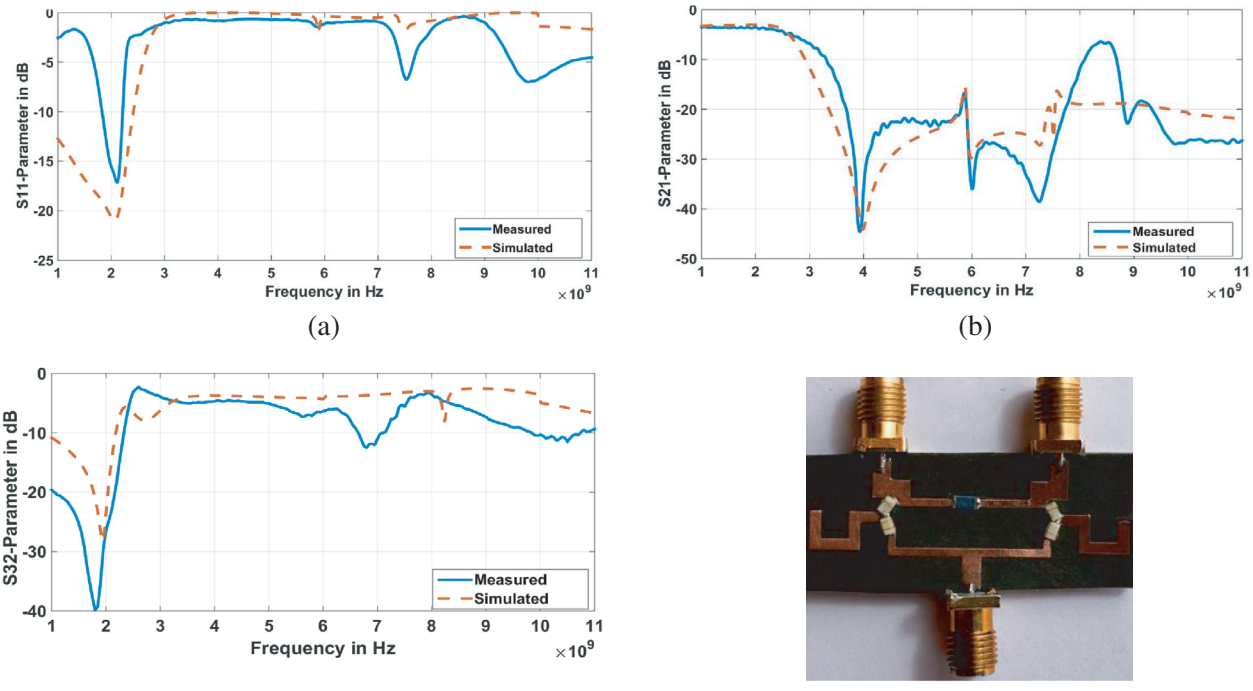
(a) (b)

Figure 8. (a) Layout of the designed WPD, (b) EM circuit co-simulation results.

Therefore, the proposed modified WPD is not that sensitive to microstrip discontinuities as well as coupling between close lines.

5. FABRICATION AND MEASUREMENTS

The designed and simulated circuit of the modified WPD has been fabricated on a specified substrate using photolithography technique, and a photograph of the fabricated circuit is illustrated in Fig. 9. The overall dimensions of the circuit are 5.1 mm ($0.051\lambda g$) in width and (33.048) mm ($0.326\lambda g$) in length with total area about 168.5 mm^2, which has 40% reduction compared to that of a conventional WPD. The measured S-parameters of the fabricated circuit compared to the EM co-simulation results are shown in Fig. 9. From the figure it can be noticed that a good agreement is obtained between them, and the fabricated circuit satisfies the desired specifications. The fabricated power divider has return loss better than 10 dB from 1.83 GHz to 2.21 GHz, insertion loss about 0.5 dB and output ports isolation better



(a) (b)

(c) (d)

Figure 9. Measured versus simulated (a) S_{11}, (b) S_{21}, (c) S_{32} and (d) photograph of the fabricated circuit.

than 25 dB in band. The measured isolation is a bit shifted from the simulated one, but fortunately it is wider in band and better in value. Therefore, this small shift does not affect the isolation performance. In addition, the maximum achievable harmonic suppressions are 46 dB and 36 dB for the 2nd and 3rd harmonics, respectively, assuming 0 bandwidth. They are still better than what is reported in [17] by at least 3 dB for both 2nd and 3rd harmonics with bandwidths of 143 MHz and 100 MHz, respectively.

A comparison between the proposed modified design of the WPD and other similar recently published work is given in Table 2. Up to the authors' knowledge, this proposed divider achieves enhanced performance better than the best reported one [17] by 7% in miniaturization, at least 6 dB in harmonics isolation and 0.3 dB in insertion loss while providing easy fabrication and closed form design equations with clear algorithm. These promising results prove that the proposed design equations are fairly accurate and help the designer to avoid going through intensive circuit optimization or 3D EM simulation, while offering design degree of freedom regarding the inductor choice.

Table 2. Comparison between the proposed modified WPD and recent publications.

Parameter	Ref. [16]	Ref. [17]	Ref. [15]	This work	Enhancement Vs. [17]
Frequency (GHz)	1.5	2.4	2	2	– – – –
Used Technique	T-shape Capacitor & stubs	$\lambda/4$ resonator & stub loaded resonator	Inductive loaded	lumped inductor with two TZ	– – – –
Fabricated TL (Ω)	≥ 70.7	Depends on iteration	≤ 70.7	≤ 70.7	easy fabrication
Miniaturization	16% for caps. & 26% for TL stub	33%	48.8%	40%	7%
Insertion Loss (dB)	0.2	0.8	0.1	0.5	0.3
Fund. Isol. (dB)	22	20	17	30	10
2nd Harm. Isol. (dB)	11	32	11.9	46	14
3rd Harm. Isol. (dB)	27	30	21	36	6
4th Harm. Isol. (dB)	23	-	25	11	– – – –
5th Harm. Isol. (dB)	-	-	25.5	27	– – – –

6. CONCLUSION

In this paper, a modified compact WPD with two transmission zeros for improved harmonics suppression has been presented. The proposed design consists of shunt open stub between two series inductors and an extra microstrip line with isolation resistors at output ports. The lumped inductors provide better harmonic suppression, size reduction, and design degree of freedom. The general design equations for the proposed WPD are derived in closed form, while a flowchart for the design procedure has been presented as well. The proposed design equations and methodology are verified through fabrication and measurements of a 2 GHz modified WPD circuit. It achieves 46 dB and 36 dB suppressions for the 2nd and 3rd harmonics, respectively, while satisfying the other required specifications. Very good agreement has been obtained between the measured performance of the fabricated WPD and the EM circuit co-simulation results. This verifies the proposed technique as well as the design methodology.

Finally, a yield simulation result of 95% proves that the proposed circuit is insensitive to fabrication and component tolerances. Up to the authors' knowledge, this proposed divider achieves enhanced performance better than the best reported state of the art by 7% in miniaturization and at least 6 dB in harmonics isolation and 0.3 dB in insertion loss while providing easy fabrication and closed form design

equations with clear algorithm. These promising results prove that the proposed design equations are fairly accurate and help the designer to avoid going through intensive circuit optimization or 3D EM simulation, while offering design degree of freedom regarding the inductor choice.

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