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A Miniaturized Self-Matched Negative Group Delay Microwave Circuit

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Abstract—A miniaturized self-matched negative group delay (NGD) microwave circuit without the need for external matching networks is proposed. The NGD circuit is based on a modified parallel-type RLC resonator, in which lumped elements (capacitors and inductors) are implemented by microstrip gaps and high-impedance and short-circuited microstrip lines. To verify the design concept, an NGD circuit with the size of $0.21\lambda_g \times 0.29\lambda_g$ is designed and fabricated. From the measurement results, the NGD time of -5.9 ns at the center frequency of 1.532 GHz is obtained with insertion loss of less than 12.5 dB, return losses of more than 25 dB and NGD bandwidth of 45 MHz.

1. INTRODUCTION

With the increase of modern communication system complexity, the group delay (GD) characteristics of RF circuits have drawn more attention [1, 2]. To avoid signal distortion caused by group delay variations, the group delay equalizers are used to compensate the variations [3, 4]. One of the adopted solutions to compensate the group delay is utilizing negative group delay (NGD) circuits [5]. Recently, the characteristics of NGD circuits have been applied to various communication systems, such as neutralizing the disturbing effects produced by LC- and RC-networks [6, 7], shortening or reducing delay lines [8], increasing the efficiency of feed-forward linearization amplifier [9], enhancing the bandwidth of analog feedback amplifier [10], minimizing the beam-squint in phased array antenna systems [11], and realizing the non-Foster reactive elements [12].

In microwave circuits, series and parallel RLC resonators are widely used to achieve NGD phenomenon [8–15]. Most of them are used in the reflection-type NGD circuit. For reflection-type NGD circuits, an extra component, such as a hybrid coupler is always needed to convert these circuits to transmission-type circuits and realize port matching [12–15]. In addition, some RLC resonators are used in the transmission-type NGD circuit with the filter synthesis approach [16]. Similarly, this kind of NGD circuit needs external matching networks. Nowadays, a new method to implement NGD phenomenon based on feedback loop technique is presented [17, 18]. This method cannot directly obtain good reflection coefficient characteristics. Therefore, external matching networks are also necessary. Certainly, the use of external matching networks will increase the number of components and size of circuits.

To obtain input and output matching without extra circuits, matched NGD circuits have been discussed [19–22]. In [19], a passive lumped network is based on a bridged tee circuit with a theoretically matched response. However, the parasitic effects of lumped elements (such as capacitors and inductors) make the implementation difficult at microwave frequencies. As a result, the return loss (RL) is degraded to 14 dB in the 900-MHz frequency band [19]. So the NGD circuits implemented by distributed-parameter technology are put forward. In [20], a $\lambda/4$ transmission line is connected between the input

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and through ports of a coupled-line section to lower the input-port reflection coefficient. In order to simultaneously satisfy input- and output-port matching, another $\lambda/4$ impedance transformer is required to symmetrically configure two coupled-line sections, which increases the size of circuits. In [21, 22], the design of an NGD circuit is based on coupling matrix approach with finite unloaded quality-factor resonators, which are realized by two-end open-circuited $\lambda/2$ microstrip lines with the need for lossy substrates. This method increases the design complexity and reduces the use flexibility. In addition, some NGD circuits implemented through microwave transversal filter approach can also obtain port matching [23, 24], whereas this method demands multi-section structures which increases the circuit size.

In this paper, a miniaturized distributed-parameter NGD circuit is proposed and self-matched without the need for external matching networks. It reduces the circuit size and simplifies its design. The proposed self-matched NGD circuit is built with a modified parallel-type resonator. The theoretical analysis of the proposed NGD circuit is developed. The implemented method with distributed parameters and the simulated and measured results are given and discussed.

2. THEORY ANALYSIS OF PROPOSED NGD CIRCUIT

As shown in Figure 1(a), the proposed self-matched NGD circuit is built with a modified parallel-type resonator. The parallel-type resonator is composed of an inductor (L_1), a resistor (R_1) and two capacitors (C_1). Between the two capacitors, there is a shunted series circuit composed of a resistor (R_2) and an inductor (L_2). The even- and odd-mode equivalent circuits of the proposed NGD circuit are shown in Figures 1(b) and 1(c), respectively. The even- and odd-mode admittances Y_e and Y_o are expressed as

$$Y_e = \frac{1}{\dfrac{1}{\mathrm{j}\omega C_1} + 2R_2 + 2\mathrm{j}\omega L_2}, \tag{1a}$$

$$Y_o = \frac{2}{\mathrm{j}\omega L_1} + \frac{2}{R_1} + \mathrm{j}\omega C_1, \tag{1b}$$

where ω is the angular frequency. After Y_e and Y_o are obtained, the S-parameters of the NGD circuit can be expressed as [25]

$$S_{11} = S_{22} = \frac{Y_0^2 - Y_e Y_o}{(Y_0 + Y_e)(Y_0 + Y_o)}, \tag{2a}$$

$$S_{12} = S_{21} = \frac{Y_0 (Y_o - Y_e)}{(Y_0 + Y_e)(Y_0 + Y_o)}, \tag{2b}$$

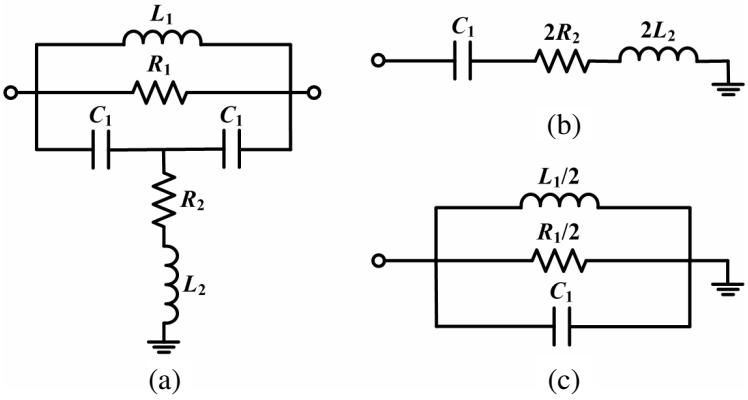

Figure 1. Equivalent circuit of the proposed NGD circuit. (a) Schematic equivalent circuit. (b) Even-mode equivalent circuit. (c) Odd-mode equivalent circuit.

where $Y_0 = 1/Z_0$ and Z_0 is the port impedance. To realize the input- and output-port matching, the condition $S_{11} = S_{22} = 0$ should be satisfied at the center operating frequency, which leads to the relations as follows:

$$\omega_0 C_1 = \frac{2}{\omega_0 L_1}, \tag{3a}$$

$$2\omega_0 L_2 = \frac{1}{\omega_0 C_1}, \tag{3b}$$

$$R_1 = \frac{1}{R_2 Y_0^2}, \tag{3c}$$

where $\omega_0 = 2\pi f_0$ and f_0 is the center operating frequency. According to Equations (1) and (2b), S_{21} can be derived as

$$S_{21} = \frac{M + \mathrm{j}N}{P + \mathrm{j}Q}. \tag{4}$$

The values of M, N, P and Q are given as

$$M = Y_0\left(\frac{4R_2}{R_1} - 1\right) - Y_0\left(\omega C_1 - \frac{2}{\omega L_1}\right)\left(2\omega L_2 - \frac{1}{\omega C_1}\right), \tag{5a}$$

$$N = Y_0\left[2R_2\left(\omega C_1 - \frac{2}{\omega L_1}\right) + \frac{2}{R_1}\left(2\omega L_2 - \frac{1}{\omega C_1}\right)\right], \tag{5b}$$

$$P = \frac{2}{R_1} + Y_0\left(\frac{4R_2}{R_1} + 2R_2 Y_0 + 1\right) - Y_0\left(\omega C_1 - \frac{2}{\omega L_1}\right)\left(2\omega L_2 - \frac{1}{\omega C_1}\right), \tag{5c}$$

$$Q = (2R_2 Y_0 + 1)\left(\omega C_1 - \frac{2}{\omega L_1}\right) + \left(\frac{2Y_0}{R_1} + Y_0^2\right)\left(2\omega L_2 - \frac{1}{\omega C_1}\right). \tag{5d}$$

Thus the GD of the proposed circuit can be obtained as

$$\tau = -\frac{d\angle S_{21}}{d\omega} = \frac{M'N - MN'}{M^2 + N^2} - \frac{P'Q - PQ'}{P^2 + Q^2}, \tag{6}$$

where

$$M' = P' = -Y_0\left[\left(C_1 + \frac{2}{\omega^2 L_1}\right)\left(2\omega L_2 - \frac{1}{\omega C_1}\right) + \left(\omega C_1 - \frac{2}{\omega L_1}\right)\left(2L_2 + \frac{1}{\omega^2 C_1}\right)\right], \tag{7a}$$

$$N' = Y_0\left[2R_2\left(C_1 + \frac{2}{\omega^2 L_1}\right) + \frac{2}{R_1}\left(2L_2 + \frac{1}{\omega^2 C_1}\right)\right], \tag{7b}$$

$$Q' = (2R_2 Y_0 + 1)\left(C_1 + \frac{2}{\omega^2 L_1}\right) + \left(\frac{2Y_0}{R_1} + Y_0^2\right)\left(2L_2 + \frac{1}{\omega^2 C_1}\right). \tag{7c}$$

Satisfying the matching condition, the GD of the proposed circuit at f_0 is obtained as

$$\tau\,|_{\omega=\omega_0} = \frac{2C_1 + \left(2Y_0^2\right)/\left(\omega_0^2 C_1\right)}{Y_0\left(1 + 2R_2 Y_0\right)\left(1 - 2R_2 Y_0\right)}. \tag{8}$$

According to Equation (8), the GD of the proposed circuit at f_0 is determined by the capacitance C_1 and resistance R_2. When $R_2 > 1/(2Y_0)$, the negative GD can be obtained. Figure 2 demonstrates the calculated GD as a function of R_2 with different C_1 at $f_0 = 1.575$ GHz. As seen from the figure, the absolute value of NGD time increases as R_2 and C_1 decrease. The NGD bandwidth is defined as

$$\mathrm{BW_{NGD}} = f_2\,|_{\tau(f_2)=0} - f_1\,|_{\tau(f_1)=0}\,, \tag{9}$$

where f_1 and f_2 are the closest frequencies to f_0 and $f_1 < f_0 < f_2$. The calculated NGD bandwidth as a function of R_2 with different C_1 is shown in Figure 3. The NGD bandwidth increases as R_2 and C_1 increase. Thus, there is a tradeoff between NGD time and NGD bandwidth.

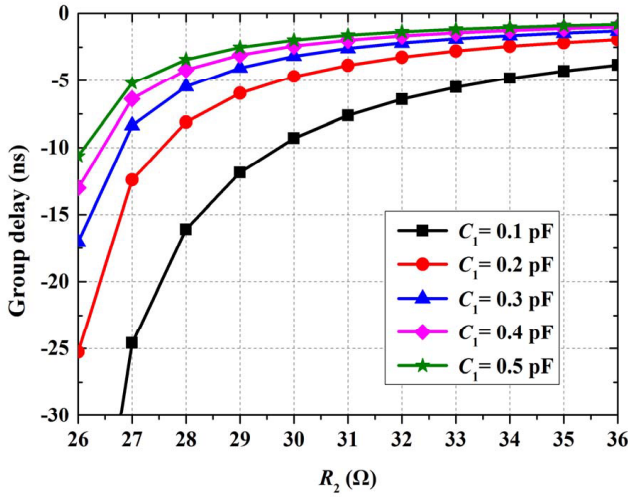

Figure 2. Calculated GD of the proposed circuit as a function of R_2 with different C_1 at $f_0 = 1.575$ GHz.

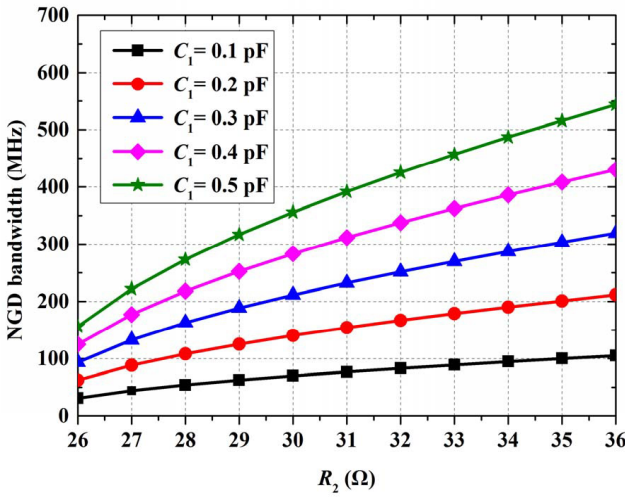

Figure 3. Calculated NGD bandwidth of the proposed circuit as a function of R_2 with different C_1 for $f_0 = 1.575$ GHz.

3. CIRCUIT LAYOUT AND DESIGN PROCEDURE

As shown in Figure 4, the proposed NGD circuit is implemented by distributed microstrip technology with an FR4 substrate having relative permittivity $\varepsilon_r = 4.4$ and thickness $h = 1.5$ mm. The capacitor C_1 is implemented by the microstrip gap. The high-impedance transmission line and short-circuited transmission line are equivalent to the inductors L_1 and L_2, respectively. The connecting lines are 50-Ω microstrip lines. The capacitance value of microstrip gap can be extracted by the ANSYS HFSS simulator. The capacitance value C_1 of the microstrip gap varies with the microstrip width w_c, and the gap s and microstrip length l_c are given in Figure 5. At the center frequency $f_0 = 1.575$ GHz, the value of C_1 increases as w_c and l_c increase, whereas C_1 decreases as gap s increases. So the required capacitance C_1 can be obtained by choosing appropriate w_c, s, and l_c.

The inductor L_1 is implemented by a transmission line with characteristic impedance Z_1 and electrical length θ_1. Then, the even- and odd-mode equivalent circuits of the proposed NGD circuit

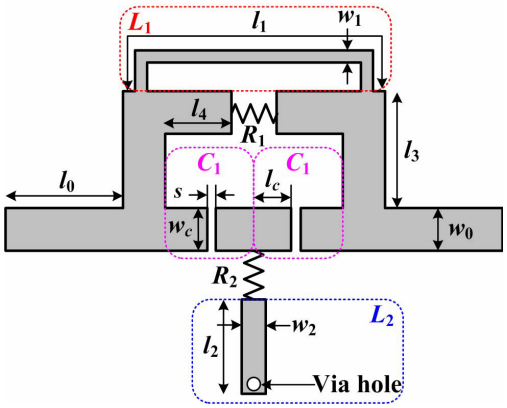

Figure 4. Structure of the proposed NGD circuit.

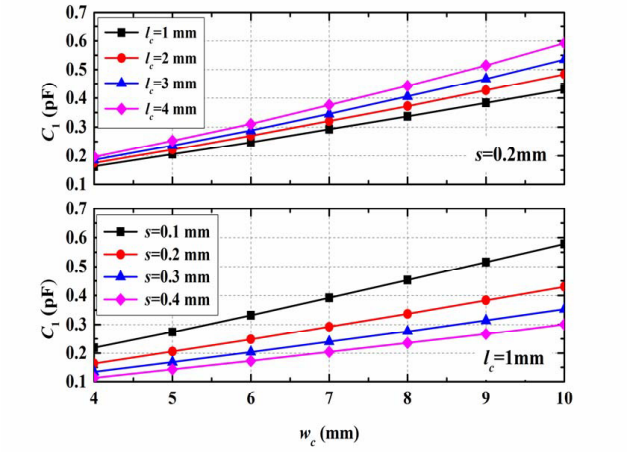

Figure 5. Capacitance value C_1 varying with l_C, w_C and the gap s at $f_0 = 1.575$ GHz.

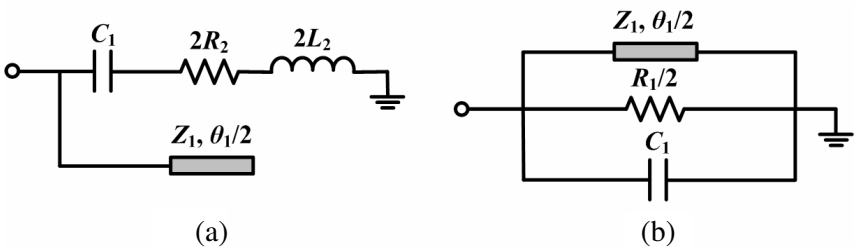

Figure 6. Equivalent circuits of the proposed NGD circuit with a transmission line instead of a inductor L_1. (a) Even-mode. (b) Odd-mode.

are revised and given in Figure 6. The even- and odd-mode admittances Y_{e1} and Y_{o1} of the revised equivalent circuits are expressed as

$$Y_{e1} = \frac{1}{\dfrac{1}{\mathrm{j}\omega C_1} + 2R_2 + 2\mathrm{j}\omega L_2} + \mathrm{j}\frac{\tan(\theta_1/2)}{Z_1}, \tag{10a}$$

$$Y_{o1} = \frac{2}{R_1} + \mathrm{j}\omega C_1 + \frac{1}{\mathrm{j}Z_1\tan(\theta_1/2)}. \tag{10b}$$

Comparing Eqs. (1) and (10), a high-impedance transmission line is chosen to make $\tan(\theta_1/2)/Z_1 \approx 0$. The inductance L_1 can be obtained as

$$L_1 = \frac{2Z_1\tan(\theta_1/2)}{\omega}. \tag{11}$$

According to the transmission line theory [25], the equivalent impedance of a short-circuited transmission line can be expressed as $Z_s = \mathrm{j}Z_2\tan\theta_2$, where Z_2 and θ_2 are the characteristic impedance and electrical length of the transmission line, respectively. Therefore, the inductance L_2 can be obtained as

$$L_2 = \frac{Z_2\tan\theta_2}{\omega}. \tag{12}$$

Considering the influence of the connecting lines, the physical dimensions need to be further optimized. Therefore, the design procedures of the proposed NGD circuit are summarized as follows.

1) Determine the center frequency, NGD time, and NGD bandwidth according to the design requirements. Obtain the values of dielectric constant and thickness of the substrate material.

2) Select proper capacitance C_1 and resistance R_2 based on the design requirements referring to Figures 2 and 3 or Equation (8).

3) Calculate the inductances L_1, L_2 and resistance R_1 using Equation (3).

4) Transform these lumped elements to the distributed parameters using Figure 5 and Equations (11) and (12).

5) Optimize the physical dimensions to obtain the correct NGD time and available NGD bandwidth using a full-wave electromagnetic simulator ANSYS HFSS. If proper physical dimensions with the required performance cannot be realized, the design should be restarted from Step 2) with other potential values.

4. IMPLEMENTATION AND PERFORMANCE

To validate the design concept of the proposed NGD circuit, an NGD circuit is designed for the GD value of -6 ns at the center frequency $f_0 = 1.575$ GHz and is fabricated on an FR4 substrate with relative permittivity $\varepsilon_r = 4.4$ and thickness $h = 1.5$ mm. The dimensions of the connecting lines are chosen as $w_0 = 2.8$ mm, $l_0 = 5$ mm, $l_3 = 5.8$ mm, and $l_4 = 2.2$ mm. The dimensions of the microstrip gap are chosen as $l_c = 1.5$ mm, $w_c = 6$ mm, and $s = 0.2$ mm. When the theoretical analysis was carried out, the connecting lines were not taken into account. The initial designed NGD circuit would

produce frequency shift. Therefore, the length of high-impedance and short-circuited transmission line need to be optimized. Because the extra resistance produced by the microstrip gap and influence of connecting lines, the practical value of resistance R_2 is smaller than the theoretical calculation. The physical dimensions of the designed NGD circuit and values of resistances after an optimization are $l_1 = 19.7\,\text{mm}$, $w_1 = 0.5\,\text{mm}$, $l_2 = 14.4\,\text{mm}$, $w_2 = 0.5\,\text{mm}$, $R_1 = 82\,\Omega$, $R_2 = 1.3\,\Omega$.

A photograph of the fabricated prototype is shown in Figure 7, and the overall size of the circuit is $22\,\text{mm} \times 30\,\text{mm}$. The fabricated prototype was measured with an Agilent N5230A network analyzer. Figures 8 and 9 give the measured and simulated S-parameters and group delays of the proposed NGD circuit. From the measurement, the NGD and insertion losses (IL) at $f_0 = 1.532\,\text{GHz}$ are $-5.9\,\text{ns}$ and 12.47 dB, respectively. The NGD fractional bandwidth is 2.94% from 1.510 to 1.555 GHz. The input/output return losses are higher than 25 dB at 1.532 GHz. And within the NGD bandwidth, the input/output return losses are better than 14 dB. There are some discrepancies between the simulated and measured results, mainly due to the inaccurate value of the relative permittivity ε_r of the substrate used in the fabricated prototype. By means of parametric analysis with the HFSS simulation, Figures 10 and 11 show the effect of ε_r on the performances of the proposed NGD circuit. As the relative permittivity increases, the center operating frequency decreases, and the return losses performance degenerates. By comparing Figures 8 to 10 and Figures 9 to 11, the actual value of the relative permittivity of the substrate used in the fabricated prototype is larger than the required value of 4.4.

Table 1 compares the proposed NGD circuit with previous publications. Compared to the reflection-type NGD circuits in [14] and [15], the proposed NGD circuit has larger NGD bandwidth and better return losses performance without the need for external matching networks. The proposed NGD circuit

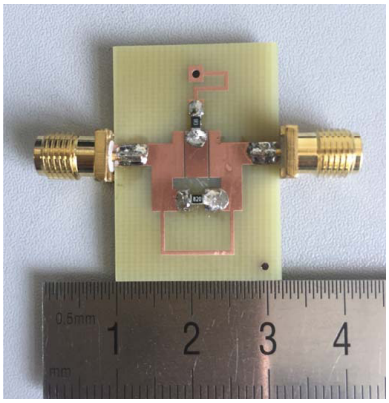

Figure 7. Photograph of the fabricated NGD circuit.

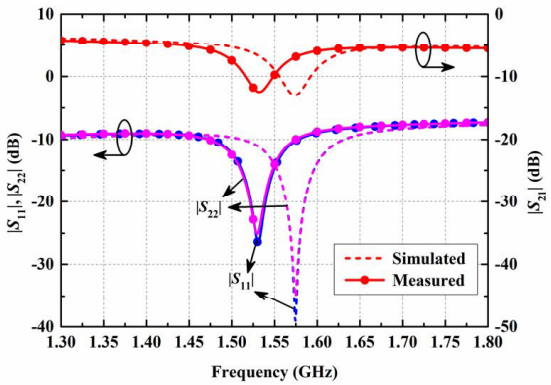

Figure 8. Simulated and measured S-parameters of the proposed NGD circuit.

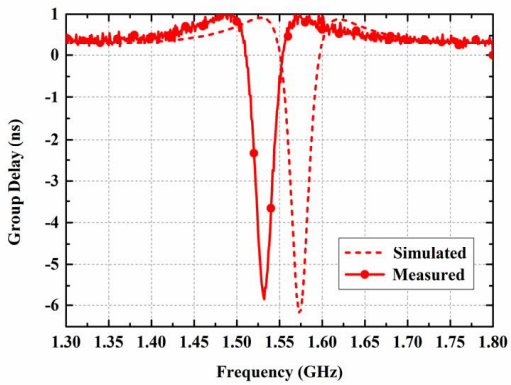

Figure 9. Simulated and measured group delay of the proposed NGD circuit.

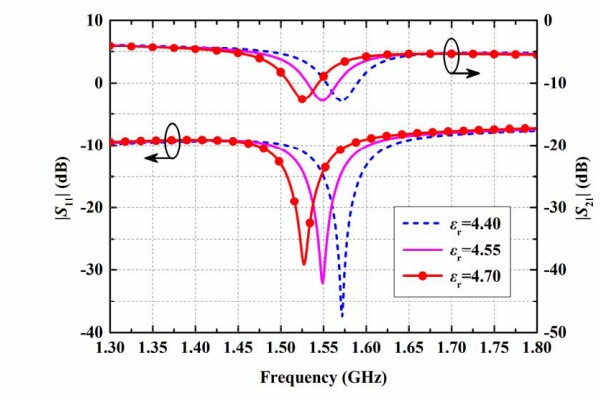

Figure 10. Effect of ε_r on the S-parameters of the proposed circuit.

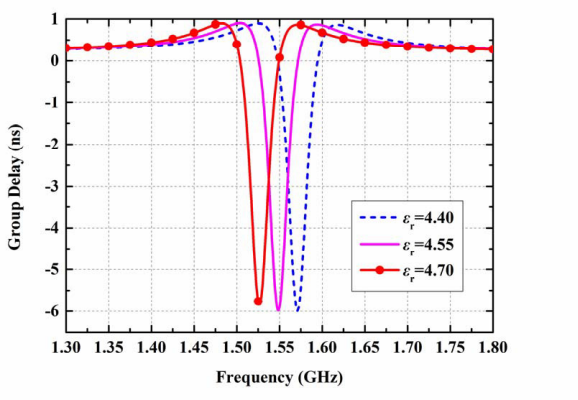

Figure 11. Effect of ε_r on the group delay of the proposed circuit.

Table 1. Performance comparisons between the proposed NGD circuit and the previous publications.

Reference	f_0 (GHz)	Extra matching network required	Achieved NGD (ns)	NGD FBW, (%)	IL at f_0 (dB)	RL at f_0 (dB)	FoM	Size ($\lambda_g \times \lambda_g$)
[14]	2.140	Y	−6.16	1.87	8.65	22	0.0909	0.66×0.63
[15]	2.140	Y	−6.30	1.96	9.23	19	0.0914	0.58×0.48
[16]	1.962	Y	−6.50	4.59	21.2	30	0.0509	0.63×0.54
[17]	1.260	N	−2.20	1.59	2.40	14	0.0334	0.63×0.28
[20]	2.140	N	−6.33	3.27	20.7	30	0.0409	0.53×0.33
[21, 22]	2.140	N	−1.03	2.80	3.82	30	0.0398	0.79×0.40
[23]*	1.000	N	−1.50	37.0	33.0	28	0.0133	0.78×0.06
This work	**1.532**	**N**	**−5.90**	**2.94**	**12.47**	**25**	**0.0624**	$\mathbf{0.29 \times 0.21}$

* Passive approach: three-section directional coupler. Y: yes. N: no.

has the same level of NGD time but provides lower insertion loss than the circuits in [16] and [20]. For the NGD circuits in [17] and [21–23], the NGD level is too small. In addition, except [14] and [15], the proposed NGD circuit has better figure of merit (FoM), which is defined as

$$\text{FoM} = |\tau(f_0)| \times \text{BW}_{\text{NGD}} \times |S_{21}(f_0)|. \tag{13}$$

Moreover, the circuit size of the proposed NGD circuit is much smaller than the previous works [14–17, 20–22].

5. CONCLUSIONS

In this paper, a miniaturized self-matched NGD circuit is proposed. The NGD circuit is built with a modified parallel-type RLC resonator implemented by distributed microstrip technology. To attain perfect matching for any NGD level, design equations are derived. The theoretical analysis shows that the GD of the proposed circuit is a function of capacitance C_1 and resistance R_2. Choosing the appropriate parameters R_1, L_1 and L_2, the matching condition can be easily satisfied. Using the proposed method, an NGD microstrip circuit with the size of $0.21\lambda_g \times 0.29\lambda_g$ is implemented. The NGD bandwidth of the fabricated NGD circuit is 2.94% with an NGD level of −5.9 ns, insertion loss of less than 12.5 dB and return losses of more than 25 dB at 1.532 GHz. The proposed NGD circuit can be used in various applications of communication systems.

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REFERENCES

1. Hwang, M. E., S. O. Jung, and K. Roy, "Slope interconnect effort: Gate-interconnect interdependent delay modeling for early CMOS circuit simulation," *IEEE Trans. Circuits Syst. I. Regul. Pap.*, Vol. 56, 1428–1441, 2009.
2. Myoung, S. S., B. S. Kwon, Y. H. Kim, and J. G. Yook, "Effect of group delay in RF BPF on impulse radio systems," *IEICE Trans. Commun.*, Vol. 90, 3514–3522, 2007.
3. Park, S., H. Choi, and Y. Jeong, "Microwave group delay time adjuster using parallel resonator," *IEEE Microwave Wireless Compon. Lett.*, Vol. 17, 109–111, 2007.
4. Ahn, K. P., R. Ishikawa, and K. Honjo, "Group delay equalized UWB InGaP/GaAs HBT MMIC amplifier using negative group delay circuits," *IEEE Trans. Microwave Theory Tech.*, Vol. 57, 2139–2147, 2009.
5. Ravelo, B., A. Pérennec, and M. Le Roy, "Experimental validation of the RC-interconnect effect equalization with negative group delay active circuit in planar hybrid technology," *IEEE Workshop on Signal Propagation on Interconnects*, 1–4, Strasbourg, France, 2009.
6. Ravelo, B., "Neutralization of LC- and RC-effects with left-handed and NGD circuits," *Adv. Electromagn.*, Vol. 2, 73–84, 2013.
7. Ravelo, B., "Recovery of microwave-digital signal integrity with NGD circuits," *Photonics Opto. Electron.*, Vol. 2, 8–16, 2013.
8. Noto, H., K. Yamauchi, M. Nakayama, and Y. Isota, "Negative group delay circuit for feed-forward amplifier," *IEEE/MTT-S International Microwave Symposium*, 1103–1106, Honolulu, HI, USA, 2007.
9. Choi, H., Y. Jeong, C. D. Kim, and J. S. Kenney, "Efficiency enhancement of feedforward amplifiers by employing a negative group-delay circuit," *IEEE Trans. Microwave Theory Tech.*, Vol. 58, 1116–1125, 2010.
10. Choi, H., Y. Jeong, C. D. Kim, and J. S. Kenney, "Bandwidth enhancement of an analog feed-back amplifier by employing a negative group delay circuit," *Progress In Electromagnetics Research*, Vol. 105, 253–272, 2010.
11. Oh, S. S. and L. Shafai, "Compensated circuit with characteristics of lossless double negative materials and its application to array antennas," *IET Microwaves Antennas Propag.*, Vol. 1, 29–38, 2007.
12. Mirzaei, H. and G. V. Eleftheriades, "Realizing non-Foster reactive elements using negative-group-delay networks," *IEEE Trans. Microwave Theory Tech.*, Vol. 61, 4322–4332, 2013.
13. Lucyszyn, S., I. D. Robertson, and A. H. Aghvami, "Negative group delay synthesizer," *Electron. Lett.*, Vol. 29, 798–800, 1993.
14. Chaudhary, G. and Y. Jeong, "Transmission-line negative group delay networks with improved signal attenuation," *IEEE Antennas Wireless Propag. Lett.*, Vol. 13, 1039–1042, 2014.
15. Chaudhary, G. and Y. Jeong, "Low signal-attenuation negative group-delay network topologies using coupled lines," *IEEE Trans. Microwave Theory Tech.*, Vol. 62, 2316–2324, 2014.
16. Chaudhary, G., Y. Jeong, and J. Lim, "Microstrip line negative group delay filters for microwave circuits," *IEEE Trans. Microwave Theory Tech.*, Vol. 62, 234–243, 2014.
17. Ravelo, B., "Theory of coupled line coupler-based negative group delay microwave circuit," *IEEE Trans. Microwave Theory Tech.*, Vol. 64, 3604–3611, 2016.
18. Ravelo, B., "Innovative theory on multiband NGD topology based on feedback-loop power combiner," *IEEE Trans. Circuits Syst. II. Express Briefs*, Vol. 63, 738–742, 2016.

19. Abunjaileh, A. I. and I. C. Hunter, "A matched bridged tee network with positive phase derivative," *IEEE/MTT-S International Microwave Symposium*, 1–4, Baltimore, MD, USA, 2011.
20. Chaudhary, G. and Y. Jeong, "Transmission-type negative group delay networks using coupled line doublet structure," *IET Microwaves Antennas Propag.*, Vol. 9, 748–754, 2015.
21. Chaudhary, G. and Y. Jeong, "A finite unloaded quality-factor resonators based negative group delay circuit and its application to design power divider," *Microwave Opt. Technol. Lett.*, Vol. 58, 2918–2921, 2016.
22. Chaudhary, G. and Y. Jeong, "Negative group delay phenomenon analysis using finite unloaded quality factor resonators," *Progress In Electromagnetics Research*, Vol. 156, 55–62, 2016.
23. Wu, C. T. M. and T. Itoh, "Maximally flat negative group-delay circuit: A microwave transversal filter approach," *IEEE Trans. Microwave Theory Tech.*, Vol. 62, 1330–1342, 2014.
24. Wu, C. T. M., S. Gharavi, B. Daneshrad, and T. Itoh, "A dual-purpose reconfigurable negative group delay circuit based on distributed amplifiers," *IEEE Microwave Wireless Compon. Lett.*, Vol. 23, 593–595, 2013.
25. Pozar, D. M., *Microwave Engineering*, 4th Edition, John Wiley & Sons, New York, 2012.