

A Miniaturized Multi-Channel TR Module Design Based on Silicon Substrate

Jun Zhou^{1, 2, *}, Jiapeng Yang¹, Donglei Zhao¹, and Dongsheng Yang¹

Abstract—The block diagram of a TR (Transmit Receive) module that consists of four channels using a silicon substrate is presented in this paper. The silicon substrate fabricated by microelectronic process has been adopted to increase the interconnect density of module. Several broadband vertical transitions are simulated and optimized by electromagnetic simulator. The vertical transition works well from DC to 40 GHz. The insertion loss is less than 1 dB, and the return loss is better than -15 dB in back-to-back configuration. A novel TR module based on the silicon substrate is proposed for its miniaturization and high integration advantages. The module occupies a compact area of $30\text{ mm} \times 20\text{ mm} \times 1.8\text{ mm}$, and the weight is 1.77 g.

1. INTRODUCTION

Nowadays, small size and multi-function electronic devices are becoming more and more popular. To meet this growing demand it is necessary to integrate more functions in the same package. Three-dimensional integration technology using novel material has become true, which makes different sizes and function devices stacked vertically integrate in the same package [1–3]. This increases the function and performance of package and reduces the size.

Up to now, most of microwave modules use multilayer LCP (Liquid Crystal Polymer) or LTCC (Low Temperature Co-fired Ceramic) board as the carriers of the microwave and digital ICs and substrate of signal's transmission [4, 5]. All these technologies mentioned above which belong to thick film technology have high transmission line precision, about 0.1 mm level. It is a serious impediment to the development of three-dimensional integration technologies. A silicon interposer with through-silicon-via, using thin film fabrication process is normally used to provide the platform of high density. There are several advantages by using a silicon substrate. Thanks to the lithography process, the lines have higher precision, which can reach 1 μm level. The thin silicon substrate with shorter filled copper through-silicon vias (TSVs) can achieve high RF performance and high packaging density [6–8]. Since the coefficients of thermal expansion of silicon and devices are matched, various ICs are fit to assemble onto the substrate. In addition, the passive devices can also be integrated in the silicon interposer using semiconductor process [9, 10].

In this paper, a X-band multichannel TR module using a silicon substrate is proposed in Section 2. The transmission characteristic of CPW (Co-Planar Waveguide) and vertical transition using TSVs are shown in Section 3. Finally, the measurement results of the TR module and conclusions have been given in Sections 4 and 5.

Received 16 August 2017, Accepted 31 October 2017, Scheduled 4 April 2018

* Corresponding author: Jun Zhou (zhoulu1997@163.com).

¹ Nanjing Electronic Devices Institute, Nanjing, China. ² Science and Technology on Monolithic Integration Circuits and Modules Laboratory, Nanjing, China.

2. SYSTEM OVERVIEW

As shown in Fig. 1, the TR module consists of four TR channels in single package. Each channel includes LNA (Low Noise Amplifier), power amplifier, SPDT (Single-Pole Double-Throw), multifunction chip with phase shifting and attenuation and power modulation circuit. In receiving mode, the signal received by antenna is amplified by LNA and output to the post stage after phase shifting and attenuation. The noise figure of TR module is decided by the loss of switch, LNA and insertion loss of transmission line. In transmitting mode, excitation signal is input to the multifunction chip and amplified by power amplifier. The transmitting and receiving modes can be controlled by TTL (Transistor-Transistor Logic) level.

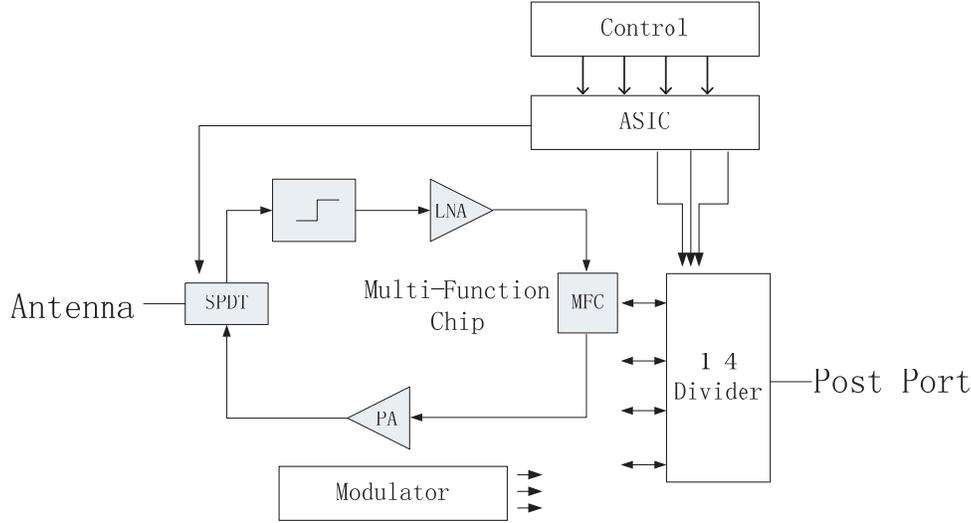


Figure 1. Schematic block diagram.

A typical structure of the TR module is shown in Fig. 2. All of GaAs MMIC (Microwave Monolithic Integrated Circuit) and digital ICs are mounted on the top surface of the silicon substrate. CPW transmission line is chosen to be the interconnection between MMICs. The I/O ports including RF ports, power ports and control ports are also designed by transmission line which can be connected to an external system using wire bonding. The TSVs filled coppers are distributed intensively under the MMICs, which provide thermal paths and grounding design. The fragile chips are protected by a hollow silicon cap which is mounted on the silicon substrate. The finished module can be assembled by the way of surface mounting, as the core part of the phased array antenna.

2.1. Multilayer, High Density Interconnect Silicon Substrate

Due to the quantities of the devices and interfaces in the TR module, the connect density is an absolutely technological bottleneck of high integration module with LTCC or PCB substrate. In this paper, multilayer silicon substrate has been adopted to increase the interconnect density. The silicon substrate is fabricated by microelectronic process and shows great advantages in line width and via diameter.

The width of the finest digital line is decreased to 20 μm , and the gap between lines is no less than 20 μm . In order to prevent short circuit, the polyimide film is covered between layers. The polyimide is a kind of regular organic inter-layer dielectric which has excellent performance at high frequency. Fig. 3(a) shows a photo of the multi-layer routing in the silicon substrate. Owing to the lacking of CMP process, there are 6 μm high raised slopes in the surface of silicon when different metal layers intersect with each other, as shown in Fig. 3(b). The polyimide film at raised slopes is thinner than usual, which may increase the short circuit risk and reduce the yield. The dielectric of polyimide film should be critical control in process, especially focusing on the dielectric between M2 and M3. The via is drilled by lithography and filled by electroplating. The diameter of the via is decreased to 50 μm , as shown in Fig. 3(c).

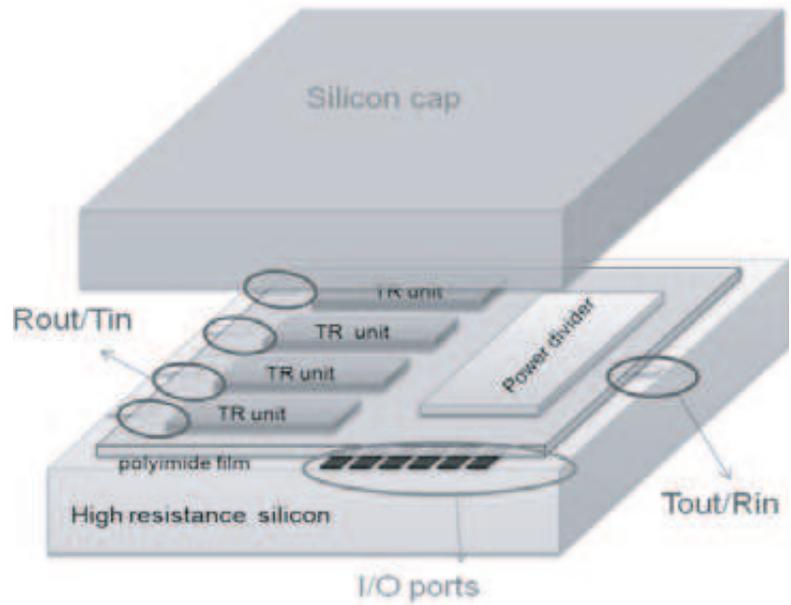


Figure 2. The structure of TR module using silicon substrate.

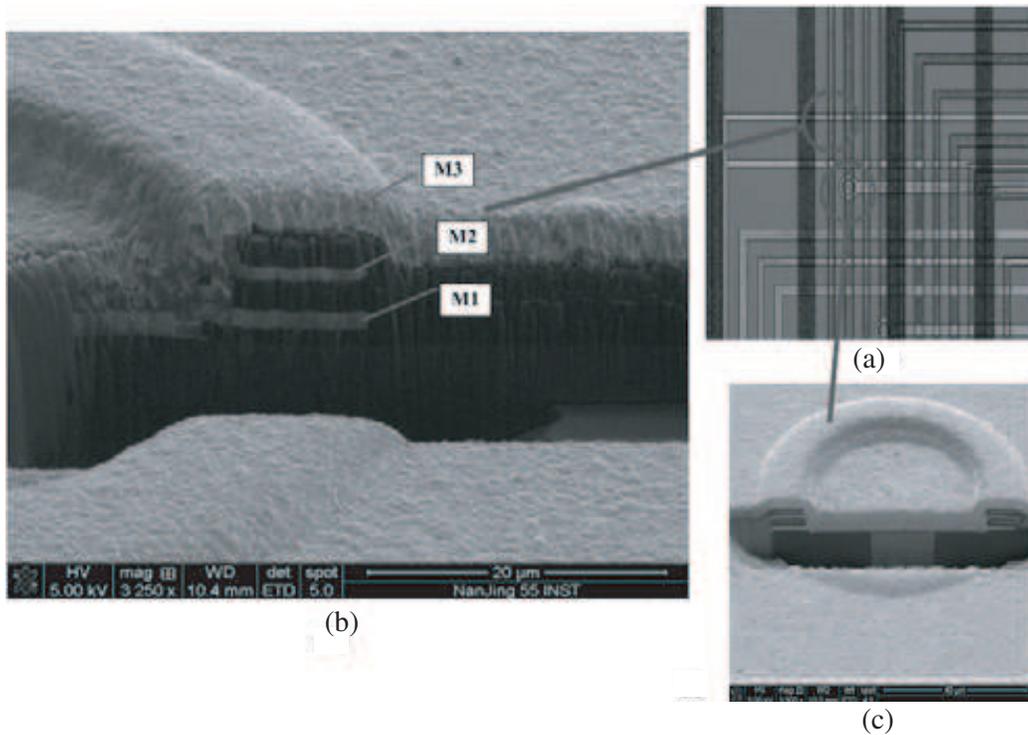


Figure 3. Micrograph of the silicon substrate.

3. TRANSMISSION CHARACTERISTICS OF SILICON SUBSTRATE

Traditionally, microstrip line, strip-line and coplanar waveguide are the most common transmission lines in microwave systems. The structure of a microstrip line is very simple, and it has good performance, but the drawback of microstrip line is that the width of line is larger when the substrate becomes thicker. The structure of CPW is slightly complicated as the electromagnetic field transmits between the signal

line and ground plane. However, the limited electromagnetic field by surfaced ground decreases the signal leakage in the substrate, reduces the process tolerance and increases the working frequency. Therefore, CPW is chosen as the transmission line in this TR module. Fig. 4 shows the structure of CPW on the silicon substrate. To avoid the positive charge between the metal and high resistivity silicon, a $1.7\ \mu\text{m}$ thick layer of silicon dioxide and $8\ \mu\text{m}$ thick layer of polyimide dielectric are covered on the surface of the silicon. The CPW transmission line design ($Z_0 = 50\ \Omega$, $W = 70\ \mu\text{m}$ and $S = 30\ \mu\text{m}$) on silicon wafer is optimized and measured as shown in Fig. 4. The insertion loss is less than $1.3\ \text{dB}/\text{mm}$, and the return loss is better than $15\ \text{dB}$ up to $40\ \text{GHz}$.

To achieve the multilayer stacked, the vertical transitions using TSVs are the most important structure in silicon substrate. Fig. 5(a) depicts the corresponding back to back configuration of CPW-CPW transition using TSVs interconnection. The dimension of CPW specifically references the structure

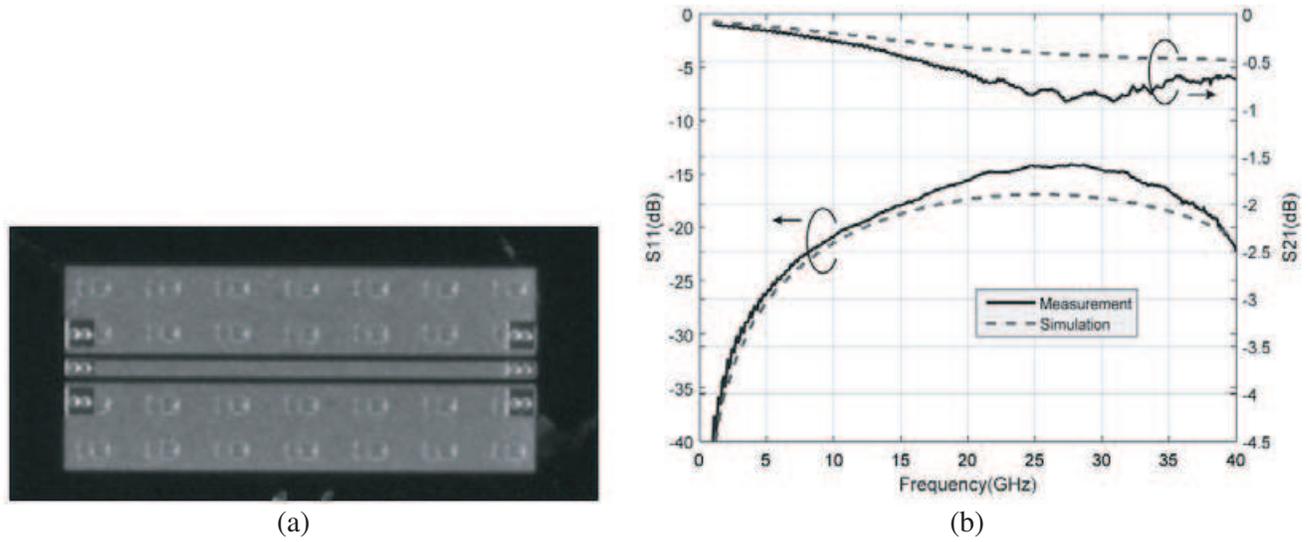


Figure 4. Test of the transmission line. (a) Photo of CPW. (b) Measurement result.

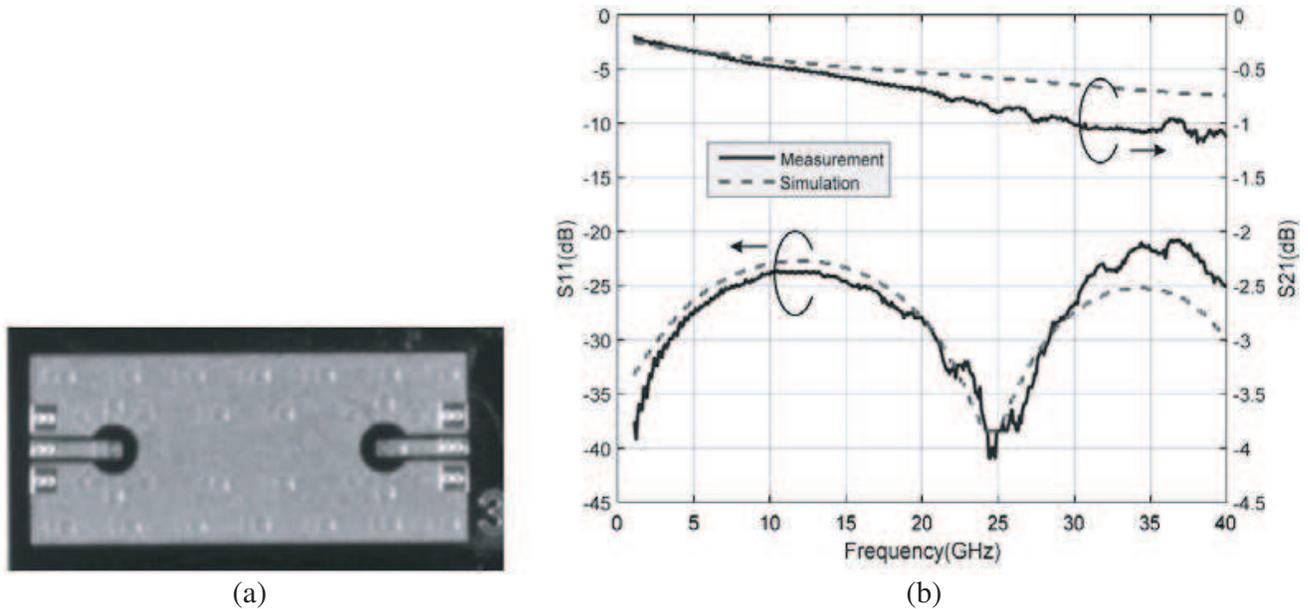


Figure 5. Test of the vertical transition. (a) Photo of quasi coaxial structure. (b) Measurement result.

mentioned above. To obtain better RF performance in the high frequency band, five ground TSVs around the signal TSVs try to form a quasi coaxial structure. TSVs with depth of 198 μm and diameter of 30 μm are fabricated using standard micro-nano processing on the top of the silicon substrate. The optimized and measured results are presented in Fig. 5(b). The insertion loss is less than 1 dB, and the return loss is better than -15 dB in back-to-back configuration. The measured and simulated results are matched closely from 10 GHz to 40 GHz.

4. MEASUREMENT RESULTS

According to the concept above mentioned, a novel TR module based on the silicon substrate is proposed for its miniaturization and high integration advantages. Fig. 6 shows a photograph of this module, which occupies a compact area of $30\text{ mm} \times 20\text{ mm} \times 1.8\text{ mm}$, and the weight is 1.77 g. The measurement results of the sample TR module are shown in Fig. 7.

The measurement was performed in the frequency range from 8.5 GHz to 10.5 GHz using the Agilent N5224A VNA. The frequency range is determined by the bandwidth of the MMIC in channels, including LNA, power amplifier, SPDT, multifunction chip with phase shifting and attenuation and power modulation circuit. Fig. 7 shows the measurement results of the TR module. The channel receiving gain is larger than 21 dB and differs within 2 dB due to the chip inconsistency as shown Fig. 7(a). Channel saturated output power is larger than 31 dBm which is determined by the saturated

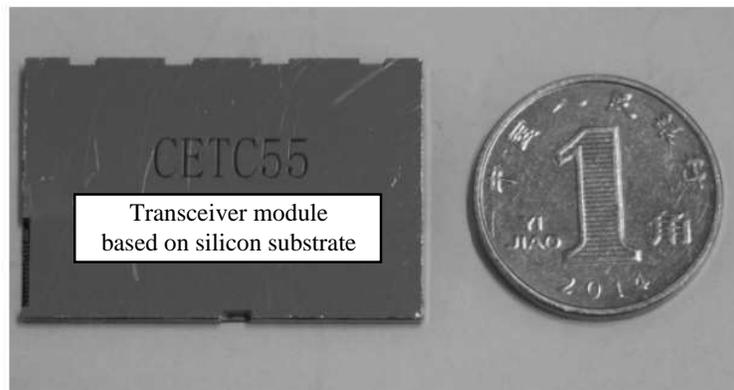
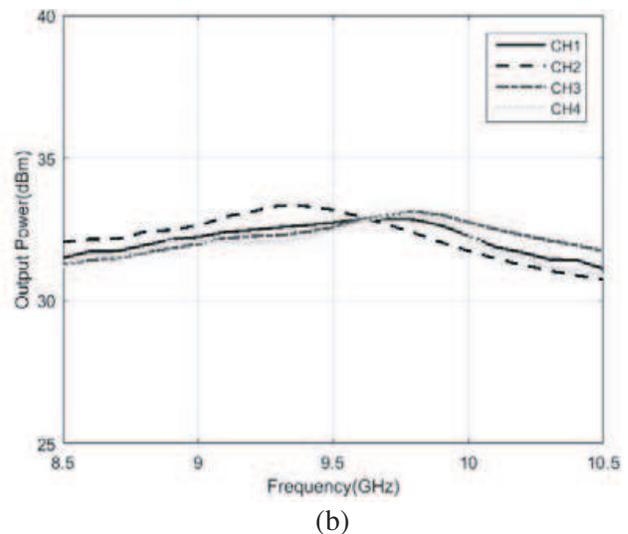
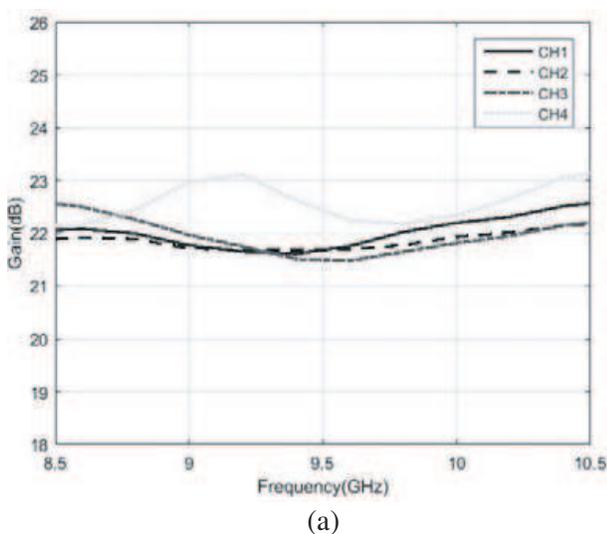


Figure 6. Photo of the transceiver module based on silicon substrate.



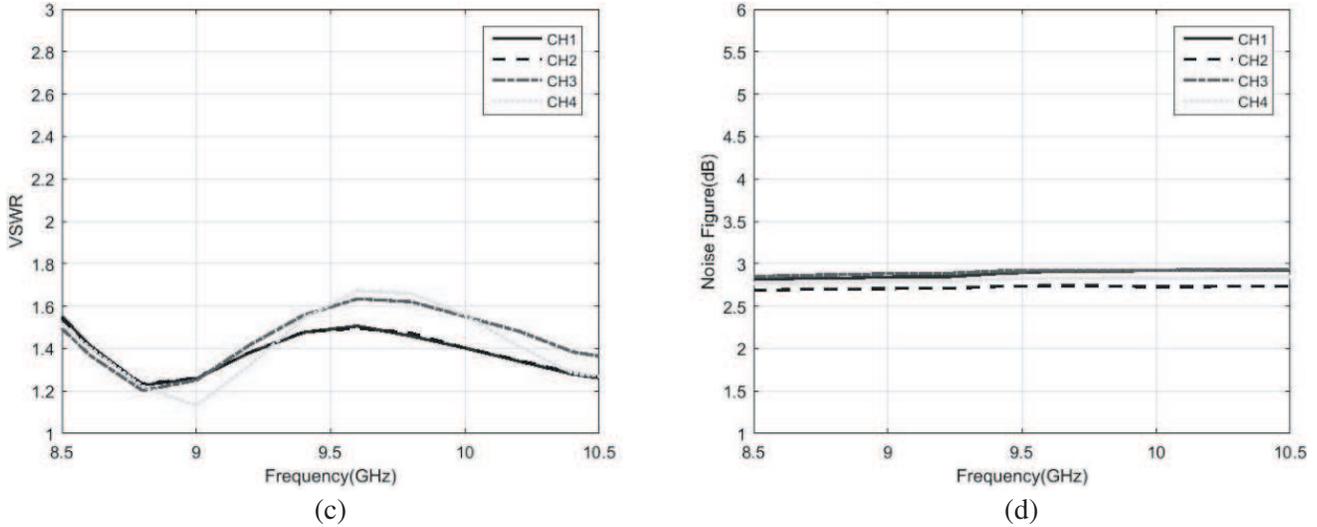


Figure 7. Measurement results of the TR module. (a) RX gain. (b) TX output power. (c) Antenna port VSWR. (d) Noise figure.

output power of PA minus the insertion loss of the SPDT and transmission line as shown in Fig. 7(b). Antenna port VSWR is better than 1.6 as shown in Fig. 7(c). The noise figure is better than 3 dB as shown in Fig. 7(d).

5. CONCLUSIONS

With the development of the wireless communication and mobile terminal, miniaturization and low weight of module are more attractive. Due to the high performance and processing accuracy, silicon technology is one of the most suitable solutions to accomplish the goal. This paper has reported a miniaturized multi-channel TR module using a silicon substrate. The whole size of the module is only $30\text{ mm} \times 20\text{ mm} \times 1.8\text{ mm}$, and the weight is 1.77 g. It shows great advantage compared with TR module using a traditional method such as LTCC or LCP technology.

REFERENCES

1. Merkle, T. and Reiner Götzen, "Millimeter-wave surface mount technology for 3-D printed polymer multichip modules," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 5, 201–206, 2015.
2. Mi, X., O. Toyoda, and S. Ueda, "A 3D heterogeneous integration method using LTCC wafer for RF applications," *2011 IEEE International 3D Systems Integration Conference (3DIC)*, 1–5, 2012.
3. Lim, K., S. Pinel, M. Davis, A. Sutono, "RF-system-on-package (SOP) for wireless communications," *IEEE Microwave Magazine*, Vol. 3, 88–99, 2002.
4. Tummala, R. R. and J. Laskar, "Gigabit wireless: System-on-a-package technology," *Proceedings of the IEEE*, Vol. 92, 376–387, 2004.
5. Juntunen, E., W. Khan, and C. Patterson, "An LCP packaged high-power, high-efficiency CMOS millimeter-wave oscillator," *2011 IEEE MTT-S International Microwave Symposium*, 1–4, 2011.
6. Tripodi, L., X. Hu, and R. Gotzen, "Broadband CMOS millimeter-wave frequency multiplier with vivaldi antenna in 3-D chip-scale packaging," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 60, 3761–3768, 2012.
7. Titz, D., R. Pilard, F. Ferrero, and F. Gianesello, "60 GHz antenna integrated on High Resistivity silicon technologies targeting WHDMI applications," *2011 IEEE Radio Frequency Integrated Circuits Symposium*, 1–5, 2011.

8. Jin, C., V. N. Sekhar, and X. Bao, "Antenna-in-package design based on wafer-level packaging with through silicon via technology," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 3, 1498–1505, 2013.
9. Zhang, R., J. C. C. Lo, and S. W. R. Lee, "Design and fabrication of a silicon interposer with TSVs in cavities for three-dimensional IC packaging," *IEEE Transactions on Device and Materials Reliability*, Vol. 12, 189–193, 2012.
10. Li, R., C. Jin, and S. C. Ong, "Embedded wafer level packaging for 77-GHz automotive radar front-end with through silicon via and its 3-D integration," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 3, 1481–1488, 2013.