Progress In Electromagnetics Research M, Vol. 61, 185–195, 2017

Control of a MOS Inverter by Out-of-Band Pulsed Microwave Excitation

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Abstract—An intentional focusing of High-Power Microwave (HPM) energy on microelectronic systems can produce effects that will potentially upset or damage the target. However, the physical mechanisms at work within the device are not often well understood. We provide a detailed understanding of the physical mechanisms involved in a common-source Metal Oxide Semiconductor (MOS) transistor inverter when Pulsed Microwave Excitation (PME) in a frequency range from 10 MHz to 1 GHz is applied on the gate terminal. Our study is based on the measurements of the current waveforms on all transistor access and explains the MOS response with and without the Radio-Frequency (RF) interference.

1. INTRODUCTION

The intentional use of High-Power Microwave (HPM) sources to disturb electronic systems is a major threat to civil and military infrastructures. Overall, HPM sources are able to produce at least 100 MW of peak RF power within the frequency range of 1 MHz to 100 GHz, with pulse duration ranging from 10 ns to 1 µs [1]. HPM couple to electronic systems many ways [2]:

(i) *Front door coupling*: The electromagnetic interference couple to systems through ports intended to transmit or receive signals for communication with other systems, such as antennas or sensors.

(ii) *Back door coupling*: The electromagnetic energy uses any parts of the system not intended to transmit or receive RF signals, such as apertures, seams, wires, power sockets or printed circuit boards traces.

HPM interferences are classified according to their severity, such as destruction, permanent damage or a variety of non-destructive failures [3, 4]. Nonetheless, it is often difficult to trace an upset to a particular individual component or circuit mechanism. It is necessary to study the electromagnetic susceptibility of each sub-system constituting the target in order to determine which physical mechanisms are at work. The aim of the present paper is to provide a physical analysis of a MOS transistor inverter under Pulsed Microwave Excitation (PME) by means of an experimental setup and methodology.

Various susceptibility effects may take place when an RF interference is superimposed on transistor pins [5–10]. Their intensity and dangerousness depend on RF power level, frequency and operating regime. Anyway, intrinsic transistor non-linearities, especially considering the current-voltage characteristic, are the main causes of distorted current waveform induced by RF excitations, which finally leads to a bias point shift. This modification of the nominal current is called the rectification effect [11].

The most recent research efforts were focused on circuits including electrostatic discharge (ESD) protection and stressed by HPM [12]. Because of their own saturation mechanism, these protections

Received 31 May 2017, Accepted 8 August 2017, Scheduled 30 October 2017

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were thought to bring some extra protection against HPM that one must quantify. However, it was shown that an HPM excitation having a sufficiently large voltage amplitude can induce — through ESD protections — a significant DC voltage at the input pin of a CMOS IC, which finally leads to a change of the logic state at its output [12]. Unfortunately, this study does not propose any physical understanding on the underlying mechanisms affecting the circuit via interference.

By using another MOS technology that also includes ESD protections, but with larger triggering thresholds, we conduct here PME attacks on a MOS common-source inverter without activating its ESD protection devices. The effective PME is the result of HPM coupling onto printed circuit board (PCB) traces (back door coupling) [13]. It is observed that a MOS inverter that initially follows the interference may switch to a state where it is totally inhibited and pinned down to the lower logic level. As a major outcome, we develop a methodology to clearly understand the EMI effect. It is based on the measurement of the transient currents on all access of the transistor, bringing many informations about average values, distortion, peak values... With the support of these measurements, the physical understanding of the response of the device under excitation becomes possible and may help to explain the system susceptibility at frequencies up to 1 GHz.

The paper is organized as follows. Section 2 describes the experimental setup used to apply the direct injection and assess all transistor instantaneous currents up to 1 GHz. Section 3 provides detailed results when the device's gate is stressed by a typical PME. We analyze the input/output voltage waveforms and their evolutions versus frequency to identify the conditions where PME causes the dramatic effect of gain inhibition and logic level pinning, which could upset digital circuits. The Section 4 details all the transistor's input/output current waveforms to provide a physical analysis of the occurrence of this dramatic effect. A first numerical approach is proposed in Section 5 to confirm and identify the elements that drive the observed response. Conclusion follows in Section 6.

2. RF INJECTION EXPERIMENTS SETUP AND METHODOLOGY

The test setup used for the direct injection experiments [14] and the measurement of all transistor currents waveform up to 1 GHz is described in Fig. 1. The Device Under Test (DUT) is mounted on a printed circuit board (PCB) made from Rogers RO3010 substrate, and the short 50 ohm microstrip tracks (< 2 cm) allow neglecting parasitic elements up to 1 GHz. Each ground connections to the chip is made through a via to the ground-plane. The commercial transistor (DUT) is a BSS83, an enhancement n-channel MOSFET from NXP, with a 140- nm gate oxide thickness and a threshold voltage of 1.2 V. It is designed for RF switching applications, and its peak transition frequency is around 500 MHz. This transistor has also been chosen because of its 4-pin SOT-143 package providing access to the bulk terminal, thus allowing direct bulk current measurement. DC measurements were used to extract the threshold voltage, see Table 1.

Table 1. Useful parameters from the NXP MOSFET datasheet.

Parameter	Value
Gate Length (L)	6 µm
Gate Width (W)	1200 µm
Oxide Thickness (t_{ox})	140 nm
Threshold Voltage (V_T)	1.2 V

Fig. 1 shows the measurement circuit when a PME is injected into the nMOS gate, which is the most likely entry for the RF signal. A Tektronix AWG 7122B arbitrary waveform generator is used to generate the PME, subsequently fed into an RF amplifier to raise the desired power output capability.

Four Tektronix CT6 high-frequency (2 GHz) current probes provide a stable measurement of all transistor currents, which are probed on a small 20-gauge wire, and measured using a first high-bandwidth DSO9254A oscilloscope, whose averaging mode was used to reduce noise on the recorded currents.

A high impedance active probe N2796A senses the instantaneous drain-source voltage $v_{DS}(t)$ across the 510 ohm drain resistor R_D. This probe introduces a load capacitance of 1.2 pF and has

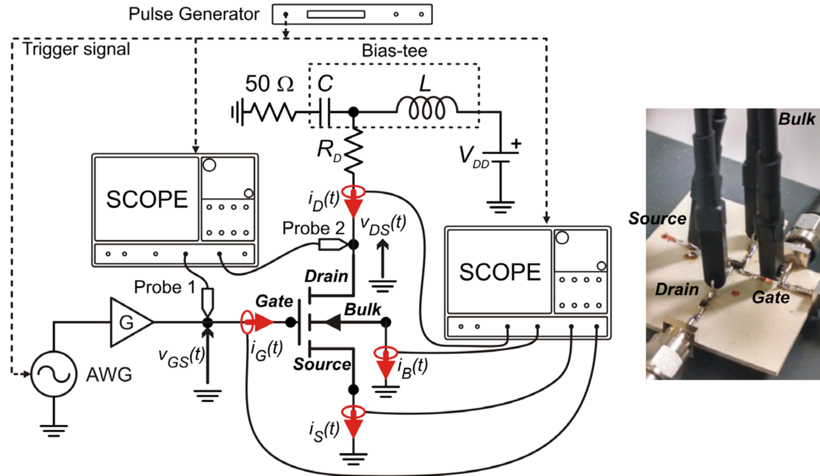

Figure 1. Block diagram of the measurement setup for transistor currents and voltages, with a photograph of the test PCB design and the current probes.

a measurement bandwidth of 2 GHz. The N2796A is provided with connections maintaining the probe head as close as possible to the measurement point, thereby greatly reducing any excess parasitic inductance. The probe is connected to a second DSO 9254A oscilloscope as shown in Fig. 1. The gate-source voltage $v_{GS}(t)$ is probed through an SMA cable and a T-junction, and measured with the same oscilloscope. A de-embedding of the T-junction and SMA cable allows to assess the gate voltage at the exact same point where the gate current is measured.

A bias-tee is connected to the MOS drain terminal to separate the RF signal and the supply path. A 50 ohm resistor was connected to the RF output of the bias-tee. This is important to minimize reflections at higher frequencies, which otherwise impair the measurements.

An 8110A pulse generator synchronizes both the two oscilloscopes and the arbitrary waveform generator (AWG). The two oscilloscopes were triggered with great precaution so that the current waveform measurement coincided with the injected RF pulse. Oscilloscopes and AWG were computer-controlled. The input signal was pulse modulated in order to prevent thermal effects in the DUT and the modulation pulse width was set to 300 ns with a repetition period of 1 ms. The fall and rise times of the modulation are 20 ns. The output voltage from the RF amplifier was maintained constant at 3 V over the frequency range of [10 MHz–1 GHz].

In the next section we will present the measurements when the inverter is stressed by typical PME.

3. RESPONSE OF A MOS INVERTER TO A PME

The effect of the PME is functionally observed on the measurement of the output voltage of the MOS inverter shown in the center part of Fig. 1. The curves in Fig. 2 are input/output voltage waveforms for frequencies of 10 MHz, 30 MHz and 50 MHz with the same peak value of 3 V of the PME applied to the gate terminal. These plots depict v_{DS} voltages exhibiting a logic waveform in response to the PME excitation. In essence, the inverter follows the input frequency.

Figs. 3(a) and (b) show the alteration of the inverter response when the frequency is increased to 100 MHz or 200 MHz. The output voltage v_{DS} no longer looks like a logic waveform and the v_{DS} voltage swing decreases with frequency. At the frequency of 400 MHz (see Fig. 3(c)) this voltage swing is so reduced that the inverter output is a sine signal between -0.7 V and $+0.7$ V. In fact, as the carrier frequency increases, the inverter response tends to reproduce the opposite of the pulse envelope with a small amount of the RF signal superimposed, the latter being so small at 400 MHz that the output signal is always below the commutation threshold of a classic logic gate. As a main result, the input of any logic block following the inverter will be totally inhibited and pinned on the lower logic level. We get a blocking of the output state, while we were expecting a tracking of the control voltage. This effect will be hereafter referred to as the "blocked state" of the inverter. This blocked state occurs

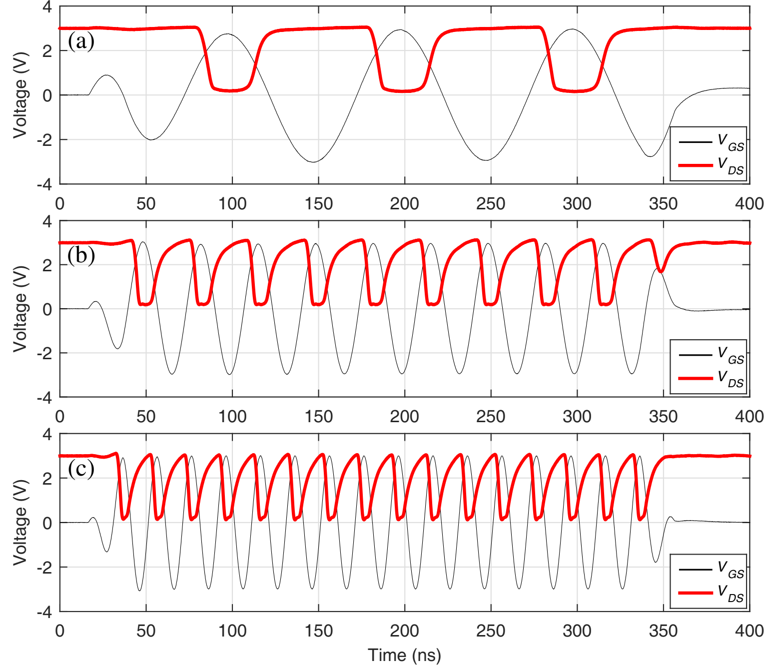

Figure 2. Input/Output voltages for an input PME of 3 V at 10 MHz (a), 30 MHz (b) and 50 MHz (c). $V_{DD} = 3$ V.

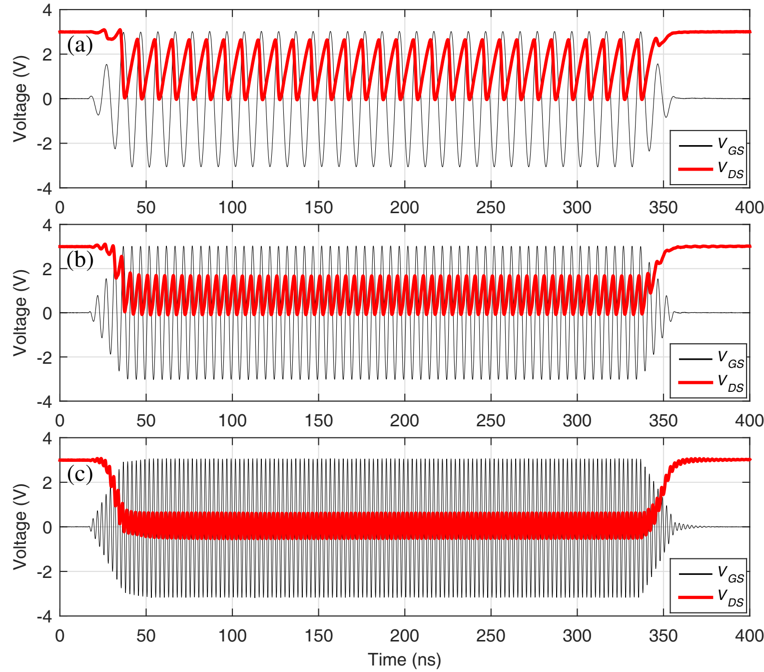

Figure 3. Input/Output voltages for an input PME of 3 V at 100 MHz (a), 200 MHz (b) and 400 MHz (c). $V_{DD} = 3$ V.

up to a PME frequency of 500 MHz. Beyond this value, this phenomenon disappears, as illustrated in Fig. 4. For such a high frequency, the output voltage v_{DS} again follows the input voltage and exhibits an increased peak amplitude of $\hat{v}_{DS} \approx 3$ V, behaving as if the input voltage v_{GS} directly ends up to the inverter output.

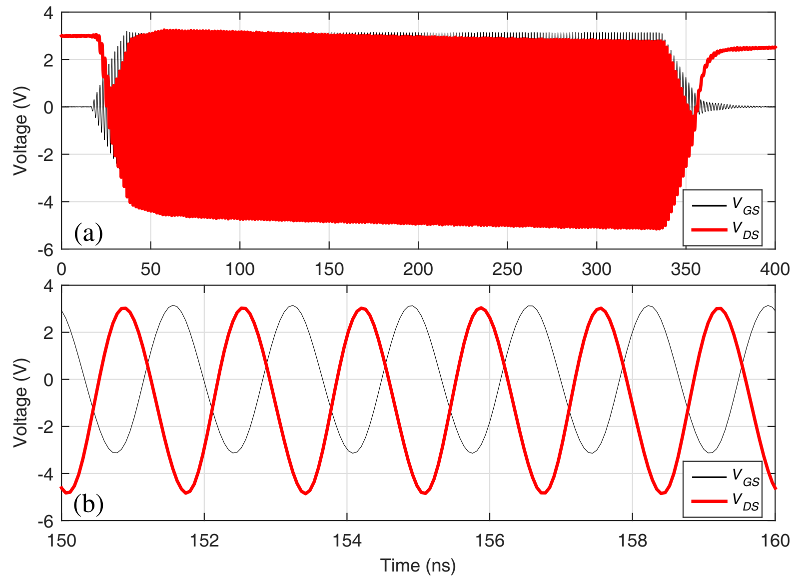

Figure 4. Input/Output voltages for an input PME of 3 V at 600 MHz (a). $V_{DD} = 3$ V. (b) Zoom of (a) from 160 ns to 170 ns.

In the next section, an in-depth analysis will be carried out to explain these observed behaviours with the help of the measured currents.

4. INPUT/OUTPUT CURRENT WAVEFORMS UNDER PME

The study of current waveforms during switching operation aims at getting insights of the "blocked state" of the MOS inverter induced by the PME. In this section, input/output voltage and current waveforms are given in Figs. 5 to 9 for increasing frequencies from 10 MHz to 600 MHz, and with the same PME peak value of 3 V applied to the gate terminal. As the input impedance of the circuit decreases with frequency rise, the power of the PME has to be increased in order to maintain the input voltage constant.

For the lower frequencies, classical current-waveforms measured on an NMOS inverter under switching operation are obtained. Actually in our experiments, the switching of the MOS inverter is caused by a sinusoidal gate control signal, unlike the conventional square input. At 10 MHz, v_{DS} follows the input signal v_{GS}, and looks like a normal logic waveform (Fig. 5(a)). Corresponding currents (Fig. 5(b), i_D, i_S, i_G and i_B are the drain, source, gate and bulk currents, respectively) show a device operating in a switched mode driven by a sinusoidal input. As a result, the transistor charge distribution varies continually, generating charging currents dominated by the extrinsic part of the device, particularly the one associated with the depletion regions [15].

When v_{GS} exceeds the threshold voltage V_T, i_S starts flowing; the device turns on; the output voltage v_{DS} tends to switch from V_{DD} to 0 V. Overshoots observed on i_S and i_B with a relatively large peak value are explained by these charging currents caused by the large-signal dynamic operation of the MOS transistor. Once the peak input value is reached ($v_{GS} = 3$ V), the DC steady-state is reached with $i_S = i_D = 5.5$ mA. The subsequent decrease of v_{GS} drives a corresponding decrease of i_S and a change in the inversion layer charge distribution. When the control voltage falls below V_T, the device tends to turn off and v_{DS} grows back to its higher value. As observed on Fig. 5(b), the time required to turn-off is longer than the turn-on time. During the turn-on process the device operates in a non-saturation region and the resulting low channel resistance speeds up the switching, to the contrary of the turn-off process where the drain resistance limits the return to zero of i_D. The time to turn-off, here named the recovery time, t_{rec}, is depicted in Fig. 6. Its measured value $t_{\text{rec}} = 11$ ns is of tremendous importance in the interpretation of the experimental results of this paper because it is associated with the slower

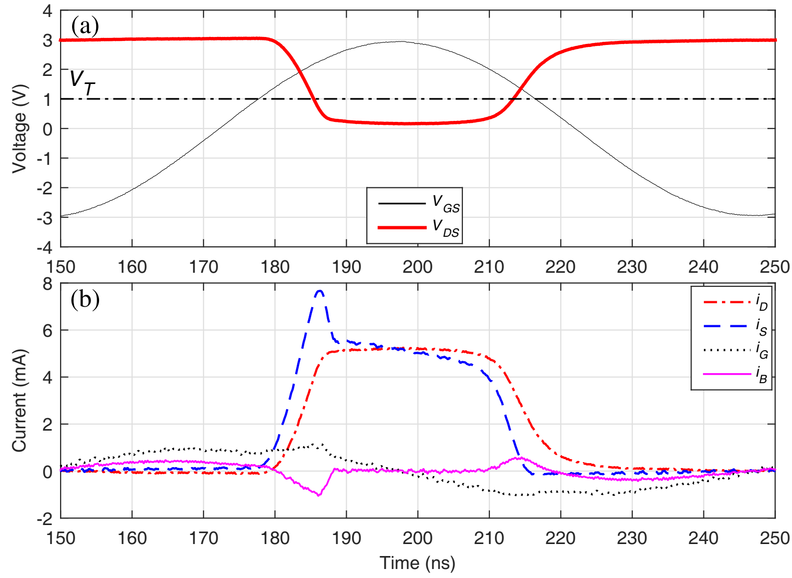

Figure 5. Zoom of Input/Output voltages and currents of a MOS inverter with a 10 MHz/3 V PME applied ($V_{DD} = 3$ V). (a) Voltages. (b) Currents.

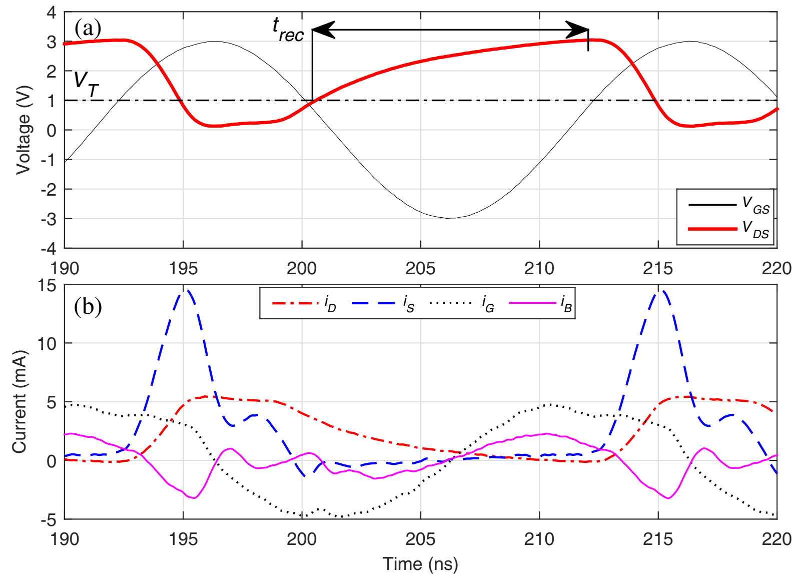

Figure 6. Zoom of Input/Output voltages and currents of a MOS inverter with a 50 MHz/3 V PME applied ($V_{DD} = 3$ V). (a) Voltages. (b) Currents.

process.

At 50 MHz (see Fig. 6), the qualitative behaviour of the switching process is similar to that observed at lower frequency. All currents exhibit shapes similar to that obtained at 10 MHz. Once the peak input value is reached, the drain current reaches its DC steady state value $i_D = 5.5$ mA, with the same turn-on time. Overshoots of source and substrate currents are more intense because of the larger dv_{GS}/dt that drives higher charging currents. Let us note that the off-state of the transistor is barely reached.

Increasing further the PME frequencies lead to a non-logic waveform for v_{DS}, close to a sawtooth, with a peak-to peak drain voltage that tends also to decrease. The input voltage period, $T \approx 10$ ns, now smaller than t_{rec}, indeed limits the v_{DS} increase rate and its previous maximum value $V_{DD} = 3$ V is no longer reached (see e.g., Fig. 7(a) at 100 MHz). At the same time the DC steady-state value

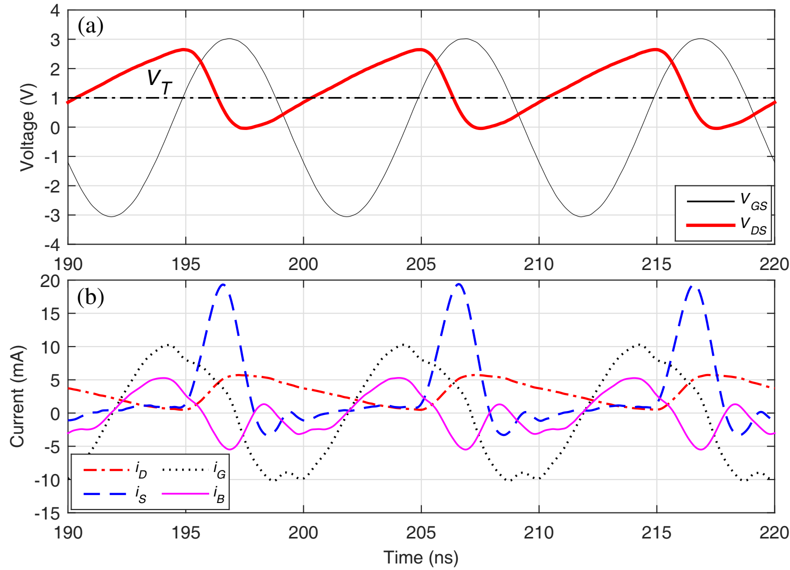

Figure 7. Zoom of Input/Output voltages and currents of a MOS inverter with a 100 MHz/3 V PME applied ($V_{DD} = 3$ V). (a) Voltages. (b) Currents.

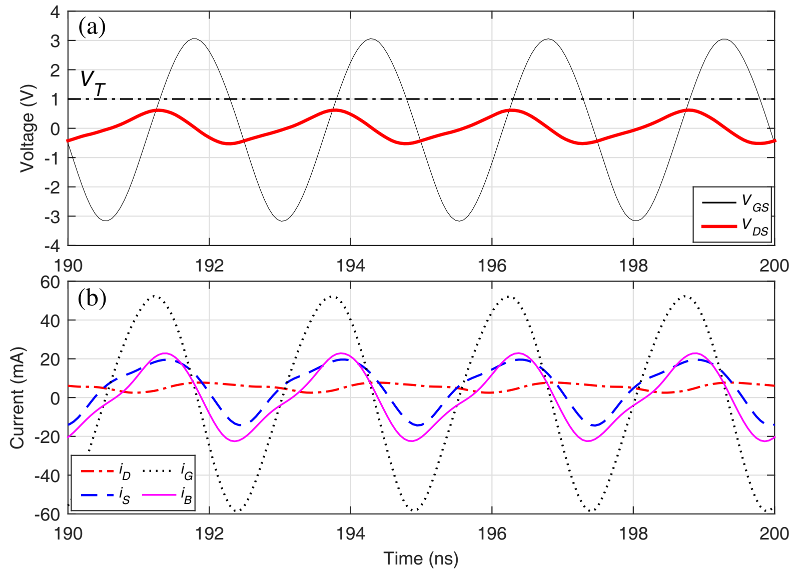

Figure 8. Zoom of Input/Output voltages and currents of a MOS inverter with a 400 MHz/3 V PME applied ($V_{DD} = 3$ V). (a) Voltages. (b) Currents.

$i_D = 5.5$ mA is still reached, but during the turn-off process. Since the drain current never vanishes, the device is never off. The i_D-waveform now differs from the half-wave rectified current observed at low frequencies, where i_D flows only when $v_{GS} \geq V_T$. The consequence is an increase of $\overline{i_D}$, the mean value of i_D, and according to the load-line of the inverter, a decrease of $\overline{v_{DS}}$, the mean value of v_{DS}.

When switching to 400 MHz (Fig. 8), the effects previously pointed out are reinforced. The v_{DS}-waveform is very close to a sine of 1 V peak voltage superimposed to a DC component. Waveforms of Fig. 8(a) correspond to a "blocked state" of the inverter, lasting as long as the pulsed RF signal is applied. The period of the driven voltage v_{GS} is 2.5 ns, a value nearly four time shorter than t_{rec}. As already mentioned i_D no more vanishes and consequently $\overline{i_D}$ further increases while $\overline{v_{DS}}$ decreases. In the same time, $v_{DS_{p\text{-}p}}$, the v_{DS} swing, also tends to decrease with the PME frequency. To the contrary,

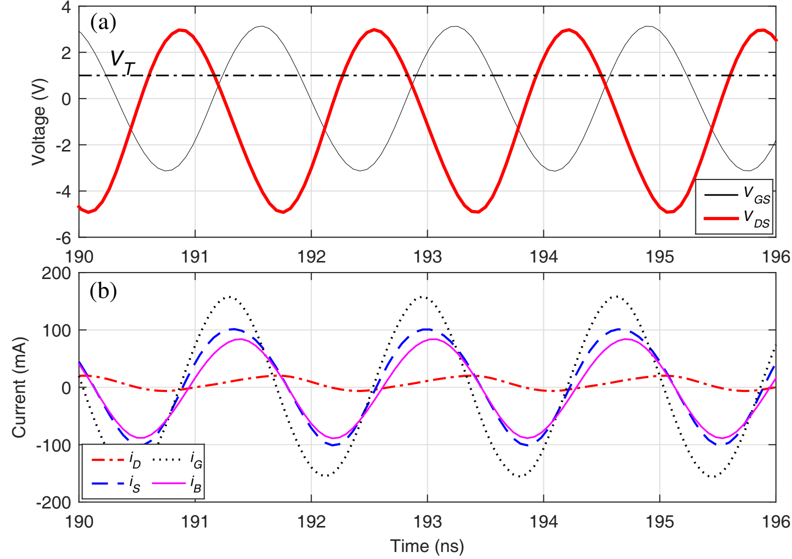

Figure 9. Zoom of Input/Output voltages and currents of a MOS inverter with a 600 MHz/3 V PME applied ($V_{DD} = 3\,\text{V}$). (a) Voltages. (b) Currents.

we observe a noticeable increase in the amplitude of source, gate and bulk currents. Moreover i_D is delayed with respect to the control voltage and its peak value of 7.5 mA is slightly higher than the DC steady-state value of 5.5 mA. The frequency of the control signal is now so high that the device reacts more to the time-variation of the input voltage than to its absolute value. At such high frequency, the impedances associated with the strong extrinsic capacitances of the device become so small that they lead to a "blocked state" of the MOS inverter.

A further increase of frequency to 600 MHz together with a constant peak value of 3 V applied to the gate produces the waveforms given in Fig. 9. The inverter is no more in its "blocked state" and all currents are almost sinusoidal. Reasons are the too fast v_{GS} changes with respect to the MOS charges that are unable to follow such a rapid variation. The major part of the current flows through the inverter using shortcuts brought by the parasitic and external elements. Above 600 MHz new paths for the electromagnetic interference are opened by these parasitics, which shunt any transistor action, namely the classical intrinsic non-linearities associated with the transport current.

5. NUMERICAL SIMULATION

SPICE-like simulations were performed with Keysight ADS software to bring additional information, particularly regarding extrinsic parasitics that are believed mandatory to understand the circuit disruption. Note that our purpose here is not to reach a perfect fit between experimental and simulated results, but instead to confirm and identify the parasitics that drive the observed response of our inverter.

Lumped elements models are used for the transistor, package, tracks and active probe measuring v_{DS}. They are all represented in Fig. 10 with values in Table 2, and will be discussed step by step.

The MOS inverter is simulated using the compact model Philips MOS Model 9. This choice is fully appropriate to the present device. This model is simplified in that only few input parameters are required and should be determined from experiments. As for the intrinsic MOS, parameters values are obtained from the measured DC characteristics and the gate-to-channel capacitance. All charge storage provided by the extrinsic part of the MOS are modeled via bias-dependent and layout-dependent capacitances. They account for the overlap of the gate over both source and drain extensions (C_{gs,e_0} and C_{gd,e_0}), the body-source and body-drain junctions ($C_{bs,e}$ and $C_{bd,e}$), and for layout-dependent capacitances because of the large source and drain contacts ($C_{c,gs}$ and $C_{c,gd}$). The only extrinsic resistance taken into account is the gate resistance because of its importance for high speed and RF signals. Bias-dependent capacitances and gate resistance are included in Philips MOS Model 9, and contact capacitances are added outside this model (cf Fig. 10). Parameters describing the DC characteristics and storage effects

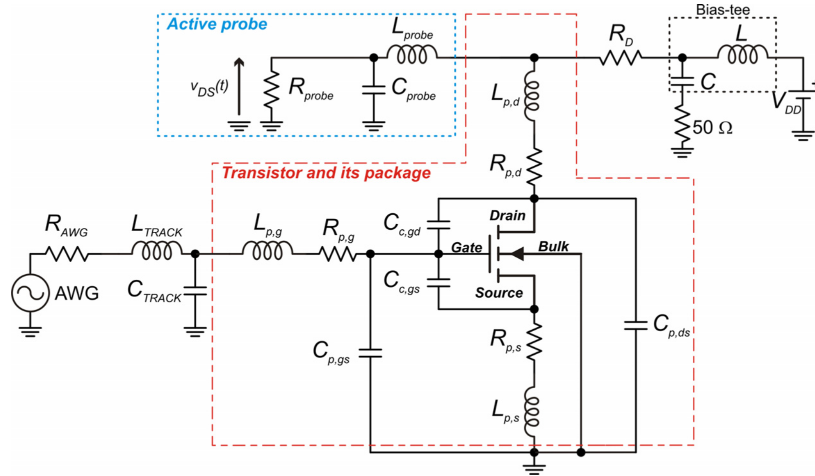

Figure 10. Schematic diagram used to simulate the response of a MOS inverter to a PME.

Table 2. Circuit model lumped elements values.

Circuit part	Element	Value
MOS extrinsic	C_{gd,e_0}, C_{gs,e_0}	0.6 pF
	$C_{bd,e}$, $C_{bs,e}$	3.5 pF
	$C_{c,gd}$, $C_{c,gs}$	0.5 pF
Package	$R_{p,g}$, $R_{p,s}$, $R_{p,d}$	1 Ω
	$L_{p,g}$, $L_{p,d}$	0.6 nH
	$L_{p,s}$	1 nH
	$C_{p,gs}$	0.15 pF
	$C_{p,ds}$	0.1 pF
Active probe	L_{probe}	5 nH
	C_{probe}	1.2 pF
Track	L_{track}	9 nH
	C_{track}	4 pF

were extracted from static characteristics and from S-parameters at various bias conditions in the frequency range of interest [16, 17]. Once intrinsic and extrinsic parts of the transistor have been modeled, its SOT-143 package is considered. Because the excitation frequency exceed the normal operating frequency of the device, the parasitic elements from the die to the external pads of the device cannot be ignored. New parasitic capacitances ($C_{p,gs}$, $C_{p,ds}$), inductances ($L_{p,g}$, $L_{p,d}$, $L_{p,s}$), and resistances ($R_{p,g}$, $R_{p,d}$, $R_{p,s}$) such as pin-to-pin capacitance, as well as bond wire inductances and resistances, were added to the equivalent circuit of the MOS transistor.

In the considered frequency range, connections between package pins and chip are assumed as regular wires and not transmission lines. A simplified model based on few lumped elements is thus used. Package parasitics are extracted from S-parameters at various bias points and for an extended frequency range (compared to the nominal frequency band of operation). A set of parasitics can be found using a conventional de-embedding process with the reasonable hypothesis that they do not change with bias. Finally, the active probe electrical model is added to the schematic diagram of the inverter under PME. Again, it is extracted from measurements, namely the input impedance characteristics over the whole frequency range of interest. Owing to the knowledge of L_{probe} and C_{probe}, the drain-source voltage v_{DS} is numerically obtained in a way similar to what we did on the high impedance input of the oscilloscope.

The time-variation of the output voltage v_{DS} is computed using circuit envelope simulation mode

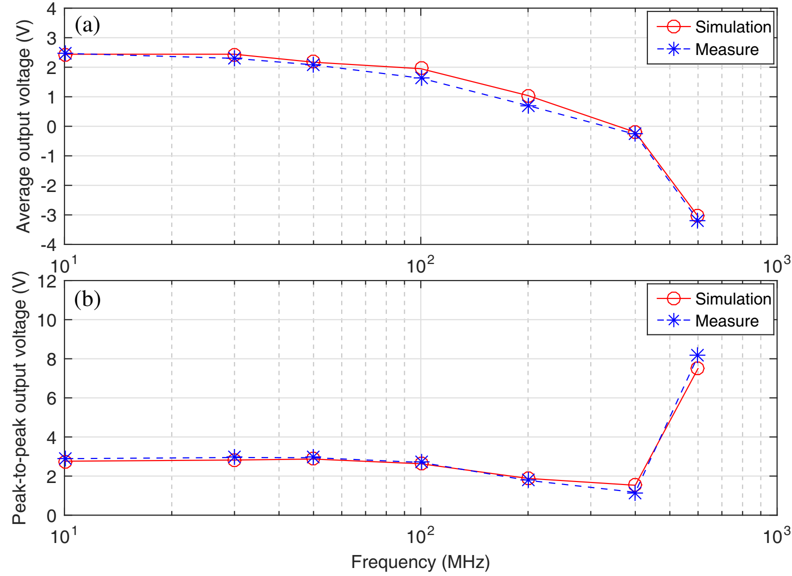

Figure 11. Comparison between measured (stars) and calculated (circles) outputs of the inverter as a function of the PME frequency, (a) average output voltage, (b) peak-to-peak output voltage.

of ADS. This technique consists in an harmonic balance analysis with time-varying envelop that particularly suits the PME modulated excitation signal used here. Note that a classical transient simulation-mode could also be used. The steady-state output of the nonlinear circuit is thus computed over a specified duration chosen in accordance with the repetition time of the PME. To compare with experiments we summarized the experimental time traces of Figs. 2–4 during the application of the PME with $v_{DS_{p\text{-}p}}$ and $\overline{v_{DS}}$. These two values were also calculated with the numerical model and the results are both plotted for comparison in Fig. 11 as a function of f, the carrier frequency of the PME.

Both the measured and computed results show a regular decrease of $\overline{v_{DS}}$ with f. The evolution of $v_{DS_{p\text{-}p}}$ is a little bit more complicated and exhibits a sudden regrowth above 400 MHz according to the resonance brought by parasitics, the latter being estimated ≈ 700 MHz from values of Table 2. The internal gate voltage is thus far much higher than the one externally fed to the device. Again, both the experimental and computed curves compare favorably. The "blocked state" of the inverter is thus highlighted for frequencies between approximately 100 MHz and 400 MHz. In fact, the correspondence between calculations and experiments was only possible when accounting for all the parasitics surrounding the ADS Philips MOS Model 9. It confirms the tremendous role played by all MOS extrinsic elements but also by the parasitics brought by the package and the PCB tracks, that act together in the occurrence of the circuit disruption observed experimentally.

6. CONCLUSION

In this paper, we have experimentally studied the electromagnetic susceptibility of the MOS transistor to PME. The methodology and equipment setup for direct injection experiments and acquisition of all transistor instantaneous currents/voltages developed here have helped to get insights of the understanding of PME effects on MOS technology at the device level.

Experimental results have highlighted the dramatic effect of electromagnetic interferences that may lead to a "blocked state" of a MOS inverter. In this particular state, the output is maintained in a constant low state as long as the RF pulse is applied, and the transistor no more follows the control voltage v_{GS}. It was shown to occur if the excitation frequency is set within a bandwidth just beyond the maximum switching frequency of the inverter.

The analysis of current waveforms during this "blocked state" has led to the conclusion that the MOS transistor's extrinsic elements and the PCB parasitics play a very important role in the occurrence of this effect. Numerical simulations have confirmed this point, as the phenomenon only appeared if

these elements were taken into account.

This "blocked state" could potentially generate upset events in larger electronic systems and will certainly also appear on more recent MOS technologies, but probably at higher frequencies because intrinsic and extrinsic capacitances are indeed reduced when shortening the gate length. The knowledge of the involved physical mechanisms is the basis to accurately understand the EM susceptibility. From the defender viewpoint, this study may help to predict how PME can upset circuits and thereby help in designing more robust electronic systems. From the attacker side, it can be useful to upset the targeted system more efficiently.

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