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A 6.6 GHz Quadrature Frequency Synthesizer with −78 dBc Reference Spur for UWB Application

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Abstract—An integer-N quadrature frequency synthesizer for single-band UWB application was designed in 0.18 µm CMOS technology. A modified bottom-series quadrature voltage-controlled oscillator (QVCO) based on reconfigurable LC tank is employed to provide quadrature signals and cover a range from 6.48 GHz to 7.07 GHz. In order to suppress the reference spur levels, an improved charge-averaging charge pump and a highly linear phase-frequency detector (PFD) are used. From the carrier of 6.6 GHz, the measured reference spur is −78.2 dBc, and the measured phase noise is −115.4 dBc/Hz at 1 MHz offset. The frequency synthesizer including buffers consumes a total power of 99 mW from a 1.8 V power supply. Chip size is 1.6 mm × 0.9 mm.

1. INTRODUCTION

Ultra-wideband (UWB) technologies are mainly employed to achieve short-distance, high-data-rate wireless communications with less than 10 meters of transmission range and higher than 480 Mb/s of transmission rate for wireless personal area networks (WPANs). These technologies are designed to replace cables between different devices' communication and to provide new applications. Examples of possible applications include high definition video streaming and home networking [1].

In China, 6–9 GHz frequency band was allocated for UWB application and 528 MHz channel bandwidth is used to expand the data rate of communications. The objective of this work is to design a frequency synthesizer that generates a single 6.6 GHz carrier for a UWB transceiver in China's UWB frequency bands, which is used for high speed video transfer demonstration and supports only one band at 6.6 GHz. Quadrature LO signals are needed for up/down mixing.

An important problem associated with frequency generation in a wideband system such as a UWB radio is the presence of spurious tones in the LO signal since they can downconvert transmissions from peer devices, degrading the signal of interest at baseband. Besides the low-spurious levels requirement, low phase noise is also critical for frequency synthesizer, to ensure receiver to achieve good sensitivity and transmitter to meet the stringent spectrum mask requirement.

In order to suppress the reference spur levels, an improved charge-averaging charge pump and a highly linear phase-frequency detector (PFD) are used. To achieve low phase noise and quadrature output, a bottom-series QVCO is employed. Wide band tuning range is achieved by using reconfigurable LC tank which simultaneously reduces the tuning sensitivity. The QVCO has 32-bands by using binary-coded MIM capacitor array for frequency coarse tuning and accumulation-mode MOS varactors for fine tuning.

This paper is organized as follows. Section 2 describes the architecture of the frequency synthesizer reported in this work and the key building blocks. Section 3 presents the experimental results. Finally, the paper is concluded in Section 4.

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2. CIRCUIT DESIGN

Typical architectures of PLL-based frequency synthesizer include integer-N, fractional-N and dual loop. Among them, the integer-N architecture is the most popular one because it is relatively simple.However its channel spacing is required to be equal to reference frequency, thus it suffers from narrow loop bandwidth resulting in long settling time. This design is to generate only a single 6.6 GHz carrier for UWB transceiver in China's UWB frequency bands. Only one band is supported, thus there is no frequency hopping. So the setting time is not stringent. Therefore, the integer-N architecture is adopted.

Figure 1 shows the block diagram of the frequency synthesizer presented in this paper. The synthesizer is composed of a highly linear phase-frequency detector (PFD), an improved charge-averaging charge pump (CP), an off-chip loop filter, a modified bottom-series QVCO that employs an on-chip analog and digital tuning technique, buffers, and a programmable divider divided from 128 to 255. A divider dummy is used to generate the test signal, it also helps to mitigate the mismatch of amplitude and phase between I signal and Q signal. Additionally, controlled by 5 bits of sub-band selection, the QVCO with a reconfigurable LC tank generates 32 overlapping sub-bands of oscillation frequency which ranges from 6.48 GHz to 7.07 GHz. The reference frequency (Fref) is 44 MHz, and the frequency resolution is also 44 MHz.

2.1. Improved Charge-Averaging Charge Pump

In charge pump PLLs, the mismatch between up-current source and down-current source in CP is the major contribution to the reference spur. Due to this mismatch, the conduction time of one current

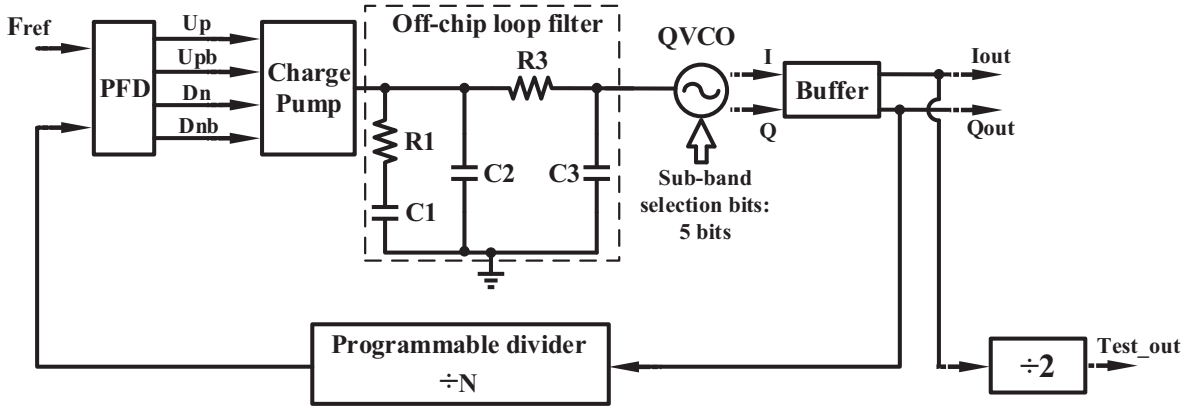

Figure 1. Block diagram of frequency synthesizer.

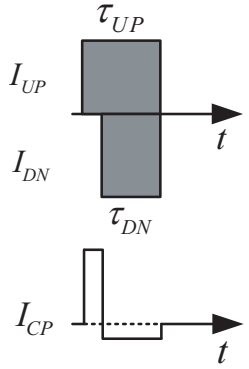

Figure 2. Charge pump output current in locked state due to current mismatch.

source is longer than that of another in clocked state, leading to a phase offset between the reference clock and feedback clock. The CP outputs a ripple current as like in Figure 2. The ripple current is then converted to ripple on the VCO control voltage by the loop filter, resulting in VCO spurs.

As illustrated in [9], the magnitude of the reference spurs relative to the carrier of frequency synthesizer is shown in expression (1)

$$Spurs = 20\log\left[\frac{\delta^2 \cdot \Delta I \cdot K_{VCO}}{4\pi \cdot C_2}\left(1 + \frac{\Delta I}{I_{CP}}\right)\right] \tag{1}$$

where δ is the delay time of the reset path of PFD, C_2 a capacitance in the loop filter, K_{VCO} the tuning gain of VCO, ΔI the mismatched amount of current sources in charge pump, and I_{CP} the up/down current of charge pump.

From expression (1), we get to know that ΔI plays a critical role for the spurs. To improve the performance of spurs, ΔI need to be minimized. In addition, other non-ideal effects of charge pump, such as charge sharing and charge injection, also need to be mitigated. Therefore, an improved charge-averaging charge pump [2, 3] shown in Figure 3 is employed for the proposed synthesizer.

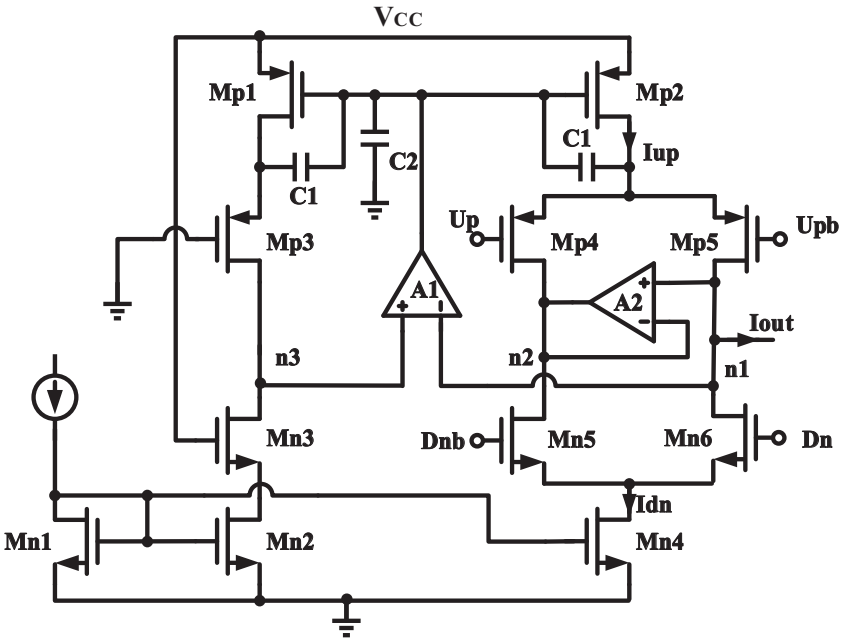

Figure 3. Schematic of the charge pump circuit.

Amplifiers A1 and A2 are adopted to reduce reference spur induced by current mismatch and charge sharing. The unity gain amplifier A2 is used to prevent the node n2 from drifting to the rails when neither of the Up and Dn signals is active, and A2 also manages to keep n1 and n2 at the same potential and thus reduce charge sharing [10]. To improve matching between the up current (Iup) and the down current (Idn), amplifier A1 is introduced. A1 compares the voltage of node n1 with that of node n3 and changes the voltage on the gate of MP1 correspondingly. Thus Ip and In are forced to be equal, regardless of the output voltage at n1. Additionally, Mn3 and Mp3 are dummy transistors which are helpful to make Iup and Idn to achieve better matching. The lengths of switch transistors are designed as the minimum available value, which can mitigate the charge injection. Increasing CP current also helps to reduce the spur, and in this work up/down currents are set as 1 mA.

Figure 4 shows the simulated up/down currents and mismatch between up/down currents versus CP output voltage. It shows that Iup and Idn match to each other very well when the CP output voltage at node n1 ranges from 0.3 V to 1.69 V under the supply voltage of 1.8 V. Over the CP output voltage from 0.3 V to 1.69 V, the simulated maximum current mismatch is 0.57% and maximum current deviation is 4.4%.

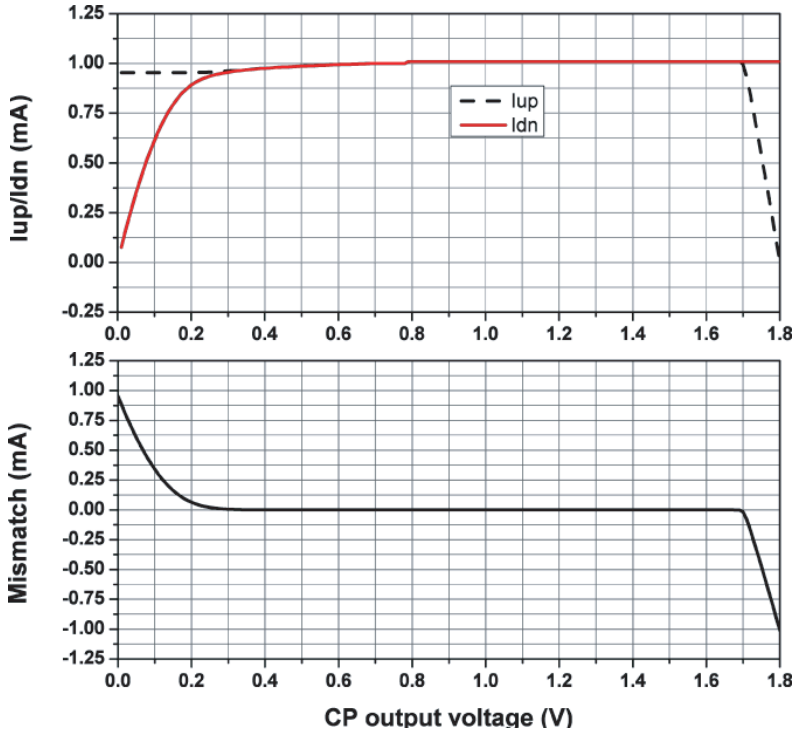

Figure 4. Simulated up/down currents and mismatch between up/down currents versus CP output voltage.

2.2. Highly Linear Phase Frequency Detector (PFD)

Phase frequency detector (PFD) generates a pair of signals which are commonly referred as up and down signals to control the up/down current sources in the charge pump. Ideally, the phase frequency detector and charge pump should have a linear transfer function of output charge versus input phase error. However, due to current mismatch in the charge pump, this linear transfer function is typically not achieved. Figure 5(a) shows traditional PFD which puts the delay cell at output of the AND gate.The delay cell generates a pulse width to prevent dead zone. Figure 6(a) shows the timing diagram of traditional PFD. If reference clock leads feedback clock, the output charge of CP is expressed as:

$$Q_T(\Delta T) = (I + \Delta I) \cdot \Delta T + \Delta I \cdot \delta = I \cdot \Delta T + \Delta I \cdot \Delta T + \Delta I \cdot \delta \quad (2)$$

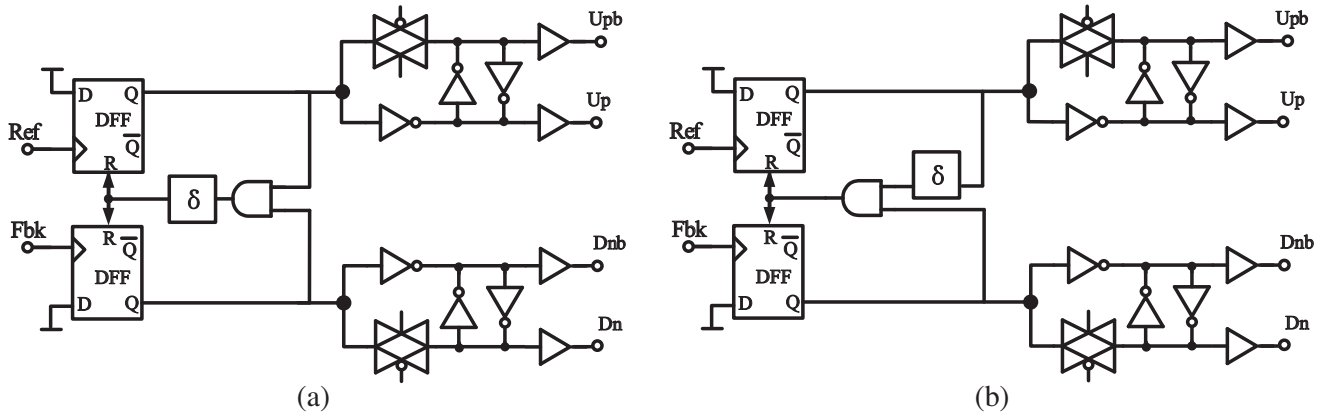

Figure 5. (a) Schematic of the traditional PFD, (b) schematic of the highly linear PFD used in this work.

while feedback clock leads reference clock, the output charge of CP is

$$Q_T(-\Delta T) = -I \cdot \Delta T + \Delta I \cdot \delta \tag{3}$$

where ΔT is the time difference between the rising edge of the reference clock and the rising edge of the feedback clock, ΔI the mismatch between up and down currents in CP, and δ the delay time in the reset path. The term $\Delta T \cdot \Delta I$ in Equation (2) varies with ΔT variation, corresponding to a non-linear distortion component, and that non-linear component degrades phase noise, spur level and cause other deleterious effects [4].

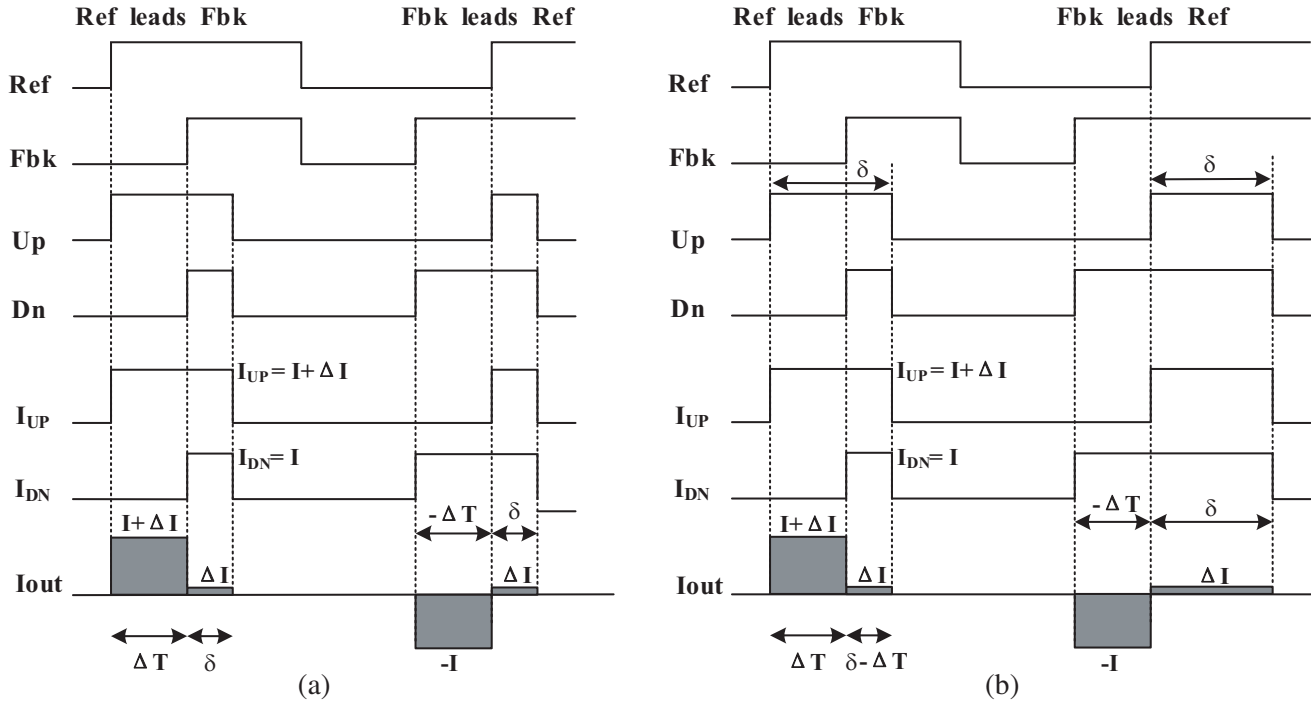

Figure 6. Timing diagram for PFD and CP: (a) traditional delay scheme, (b) new delay scheme.

To eliminate the effect of the non-linear component, a highly linear PFD topology is used in this work, as shown in Figure 5(b). Unlike the traditional PFDs, a new clocking scheme which places the reset delay cell δ on the reset path of Up signal, generates Up and Down signals such that up/down current mismatch in the charge pump does not show up in the output of the charge pump. Figure 6(b) shows the timing diagram for this new delay scheme. When reference clock leads feedback clock, the output charge of CP is expressed as

$$Q_N(\Delta T) = (I + \Delta I) \cdot \Delta T + \Delta I \cdot (\delta - \Delta T) = I \cdot \Delta T + \Delta I \cdot \delta \tag{4}$$

while feedback clock leads reference clock, the output charge of CP is

$$Q_N(-\Delta T) = -I \cdot \Delta T + \Delta I \cdot \delta \tag{5}$$

In Equations (4) and (5), the terms $I \cdot \Delta T$ and $-I \cdot \Delta T$ are the desired linear components, and the term $\Delta I \cdot \delta$ is fixed, corresponding to DC offset. The non-linear component is canceled by introducing a fixed delay δ after the rising edge of the up signal. The cancellation of the nonlinear component results in a linear transfer function of CP output charge versus phase error.

Figures 7(a) and (b) show the simulated curves of CP output charge versus PFD input phase difference for the traditional and the new clocking schemes, respectively. Here, PFD input phase difference is expressed as the time difference between the rising edges of reference clock and feedback clock. The CP output charge Q_{CP} is converted to the time by equation $T = Q_{CP}/I_{CP}$, where I_{CP} is the CP up/down current sources. Integral nonlinearity (INL) is used to compare the linearity of the

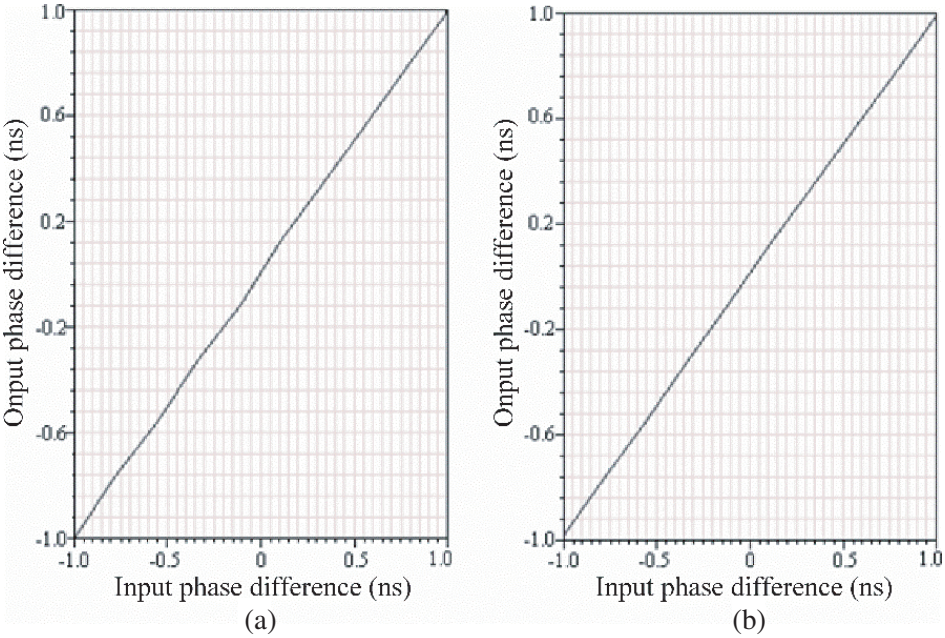

Figure 7. Simulated transfer-function curves of PFD and CP: (a) traditional delay scheme, (b) new delay scheme.

two transfer functions. The ideal transfer function of PFD and CP is a straight line. Here, the INL is defined as the maximal deviation between the actual output value and the ideal output value. The traditional clocking scheme has an INL of 0.11 ns while the new clocking scheme has an INL of 0.024 ns. Compared to the traditional PFD, the new clocking scheme PFD achieves much better linearity which helps to reduce the spurs level and phase noise.

The buffers and inverters at the outputs are used to minimize the timing mismatch between the Up/Dn and Upb/Dnb signals. The complementary control signals at the charge pump input can be perfectly matched by a symmetrical layout, which helps to reduce the phase noise and spurs induced by timing mismatch.

2.3. Bottom-series QVCO

In order to achieve excellent phase noise and good quadrature accuracy, a modified bottom-series structure with two symmetric coupled LC oscillators is employed as shown in Figure 8. In this topology, the coupling injection transistors are in series with and placed at bottom of the cross-coupled negative-gm cells [5]. The LC-type QVCOs include a complementary cross-coupled NMOS/PMOS pair for generation of negative conductance, LC resonators consisting of a differential coil, accumulation-mode MOS varactors and coarse tuning capacitor array. To cover the VCO tuning range, conventional coarse tuning capacitances composed of MIM capacitors and switches are used in the switched capacitor array based on binary-weighted architecture.

From expression (1), the lower the K_{VCO} is, the better the spur level is. In order to lower the tuning gain and extend the tuning range simultaneously, a 5 bits binary-weighted array of switched MIM capacitor is used. In this work, the tuning gains of 32 overlapping frequency sub-bands are varied from 53 MHz/V to 64 MHz/V.

The width ratio of the coupling transistor to the negative-gm cell transistor is a key parameter in the design of QVCO. The ratio is optimized for best performance such as phase noise, phase accuracy and amplitude balance. In this work, the value of this ratio for our bottom-series QVCO design is chosen to be 7, in order to obtain the desired phase noise performance and quadrature accuracy [6]. The simulated phase noise is better than -120 dBc/Hz at 1 MHz offset.

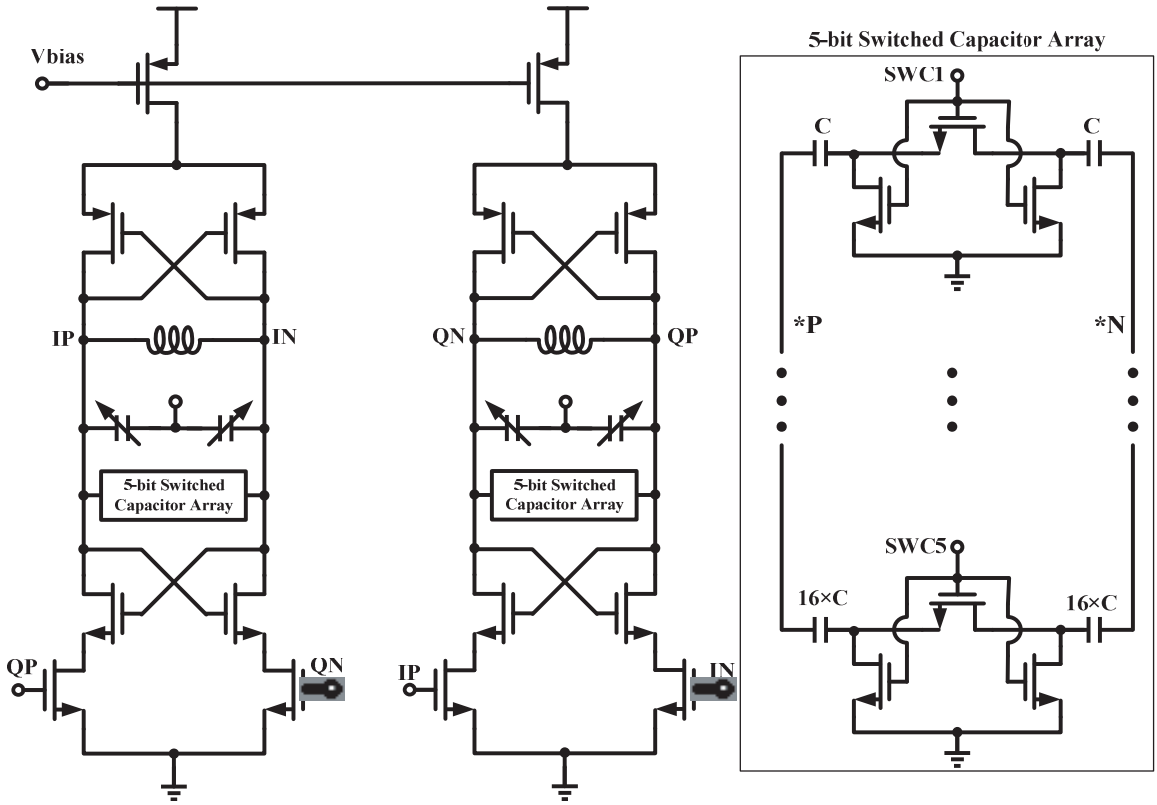

Figure 8. Schematic of the bottom-series QVCO.

QVCO inductors' differential Q-factor and inductance versus frequency are shown in Figure 9. The inductor has a differential inductance of 595 pH and a differential Q-factor of 14 at 6.6 GHz, while the self-resonant frequency is 48.9 GHz. Transistor mismatch, inductor mismatch and capacitor mismatch all have effect on the QVCO quadrature accuracy. Introducing a 0.1% mismatch between the two LC tanks in simulation, deteriorates the quadrature error by less than 1°. Because inductor mismatch model is not achieved in TSMC 0.18 µm CMOS, here, the effect of capacitor and transistor mismatches on QVCO quadrature phase based on 1000 Monte Carlo simulations is shown in Figure 10. It shows that the quadrature phase error is smaller than 1.25°.

2.4. Programmable Divider

In this work, programmable divider is composed of a chain with 7 stages of divide-by-2/3 divider cell series connected, as shown Figure 11. The divide-by-2/3 divider cells are implemented in differential cascade voltage switch logic (DCVSL) [7, 8] for saving the power consumption. The multi-modulus divider provides a division ratio as in expression (6). By changing the control bits $P_i\,(i = 0, 1, \ldots, 6)$ of these cells, the division ratio can be varied from 128 to 255. Table 1 shows the simulated performance of the frequency synthesizer in different process corners and temperatures.

$$\frac{f_{out}}{f_{in}} = \frac{1}{P_0 + P_1 \times 2^1 + P_2 \times 2^2 + P_3 \times 2^3 + P_4 \times 2^4 + P_5 \times 2^5 + P_6 \times 2^6 + 2^7} \tag{6}$$

3. MEASUREMENT RESULTS

The frequency synthesizer in this work is integrated in a UWB transceiver and fabricated with a 0.18 µm CMOS technology. A chip photograph of the circuit, with an area of 1.6 mm × 0.9 mm, is shown in Figure 12.

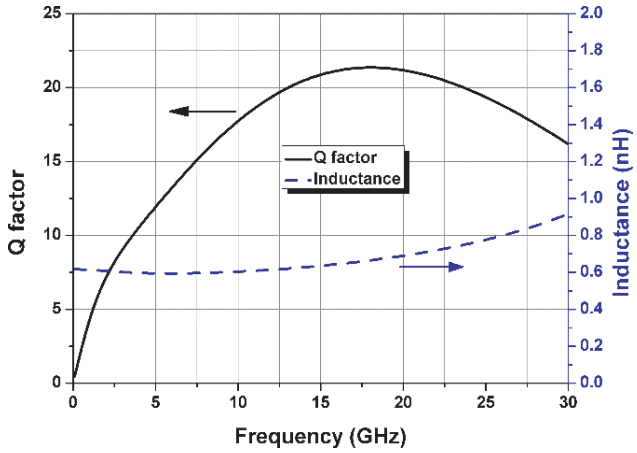

Figure 9. Inductor Q-factor and inductance versus frequency.

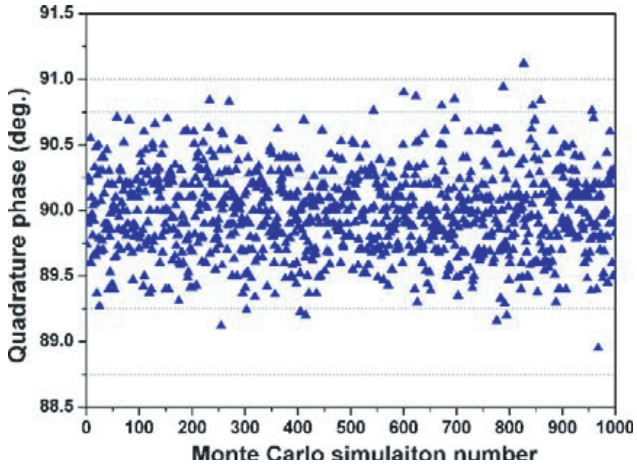

Figure 10. Effect of capacitor and transistor mismatches on QVCO quadrature phase based on Monte Carlo simulation.

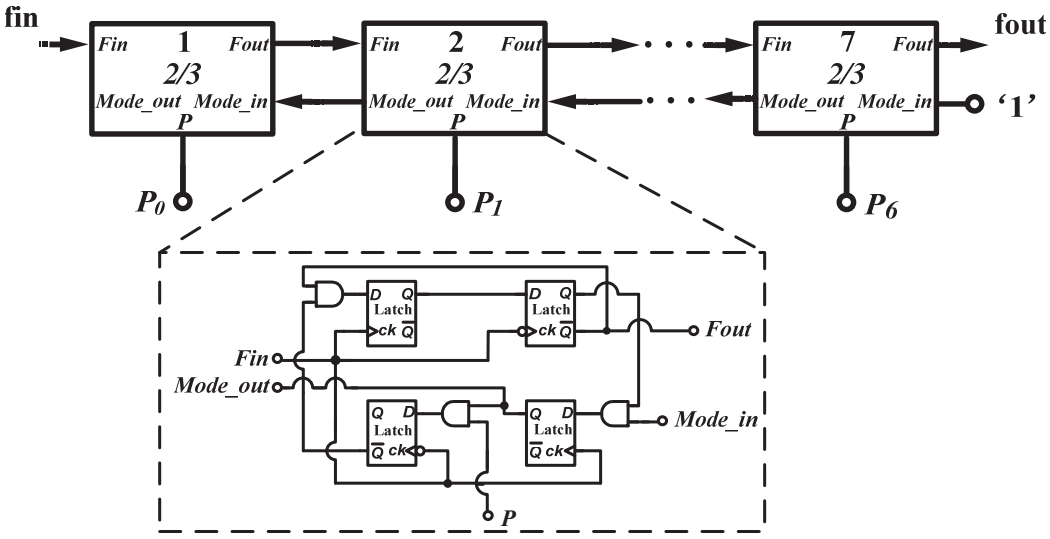

Figure 11. Schematic of the programmable multi-modulus divider.

Table 1. Simulated performance of the frequency synthesizer in different process corners and temperatures.

	$FF/-40°$	$TT/27°$	$SS/85°$
Tuning Range (GHz)	$6.56 \sim 7.19$	$6.28 \sim 6.98$	$6 \sim 6.78$
Phase Noise @1 MHz (dBc/Hz)	$-117.7 \sim -117$	$-117.1 \sim -116.6$	$-117.2 \sim -117.5$
Spur Level (dBc)	-82	-80	-77
Power (mW)	98.6	96.2	92.7

The synthesizer is mounted on PCB for testing. An external reference of 44 MHz is generated from Agilent N5182A MXG vector signal generator. The test signal is measured from divider dummy divided by 2, as shown in Figure 1. The power dissipation of the frequency synthesizer is 99 mW from a 1.8 V supply, including buffers.

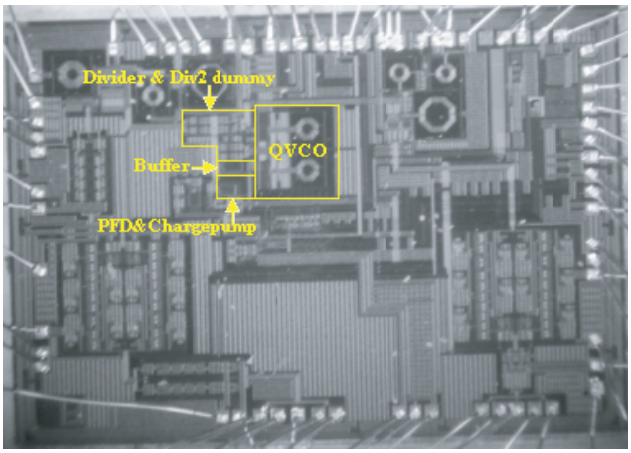

Figure 12. Chip photograph of frequency synthesizer integrated in a UWB transceiver.

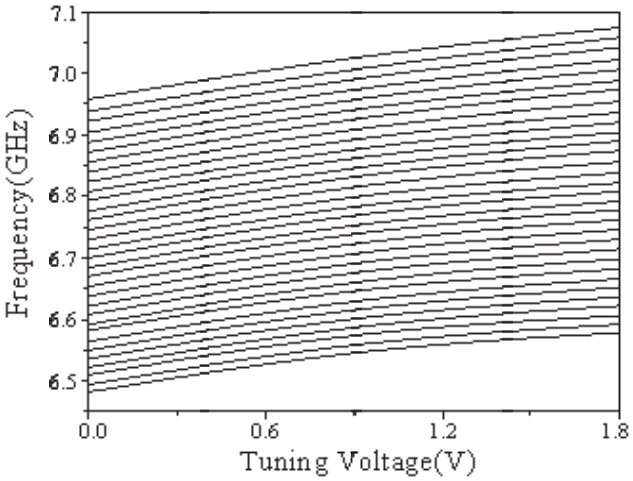

Figure 13. Measured frequency tuning characteristic of bottom-series QVCO.

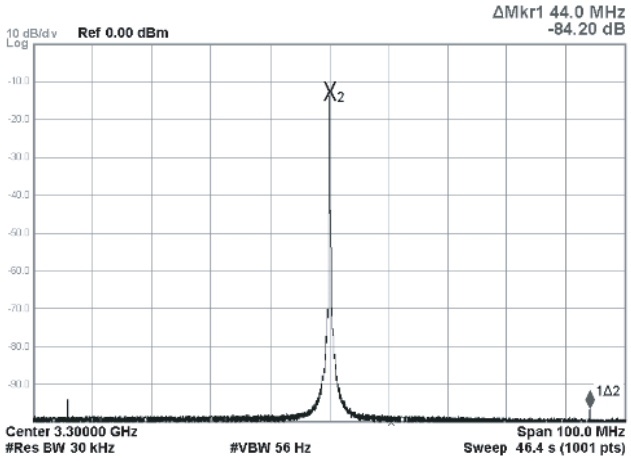

Figure 14. Measured 3.3 GHz frequency spectrum of the synthesizer locked in 6.6 GHz.

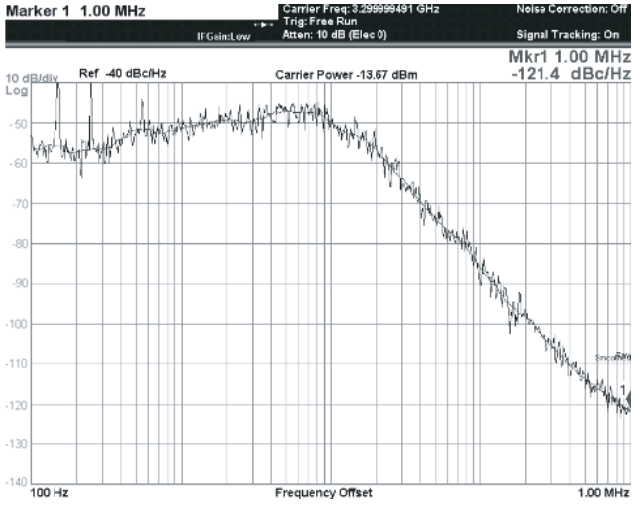

Figure 15. Measured 3.3 GHz close-loop phase noise of the synthesizer locked in 6.6 GHz.

The tuning range of the bottom-series QVCO is measured to be from 6.48 GHz to 7.07 GHz, and the measured tuning gain (K_{VCO}) is from 53 MHz/V to 64 MHz/V, as shown in Figure 13.

When the frequency synthesizer is locked at 6.6 GHz, the frequency of test signal is 3.3 GHz. As shown in Figure 14 and Figure 15, from 3.3 GHz test signal, the measured reference spur suppression is 84.2 dB at an offset of 44 MHz, and the phase noise is −121.4 dBc/Hz at 1 MHz offset. Theoretically, the spur level and phase noise of 6.6 GHz are worse than 3.3 GHz by 6 dB. Therefore, at the local frequency of 6.6 GHz, the reference spur suppression is 78.2 dB at an offset of 44 MHz, and the phase noise is −115.4 dBc/Hz at 1 MHz offset.

Table 2 summarizes the performance of the proposed quadrature frequency synthesizer and presents a performance comparison with other synthesizers. As shown in Table 2, the proposed synthesizer has a much better spur level and phase noise than previous works in the same technology.

The tuning range figure of merit (FOM_T) [16] is used to compare the performances of frequency synthesizers and is expressed as:

$$FOM_T = PN(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\cdot\frac{FTR}{0.1}\right) + 10\log\left(\frac{P_d}{1\,\text{mW}}\right) \tag{7}$$

Table 2. Performance summary and comparison.

	This work	[11]	[12]	[13]	[14]	[15]	[17]	[18]	[19]
Quadrature Output	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Phase Noise @1 MHz (dBc/Hz)	−115.4	−104	−106	−98	−95	−128	−98	−130	−116.2
Spur Level (dBc)	−78.2	−60	< −45	−55	< −43	< −42	−71	−28	−63.2
Power (mW)	99	88.5	108	117	29.6	64	0.69	62.7	26.9
Frequency Range (GHz)	6.48 –7.07	6.34 –10.56	9.27 –10.25	3 –10	3.43 –4.49	2 –16	5.94 –5.97	10 –10.55	26.2 –32.4
FOM$_T$ @1 MHz (dBc/Hz)	−170.9	−177	−165.5	−174.2	−160.8	−201.9	−149.2	−186.8	−197.8
Area (mm^2)	1.44	3.5	3.61	1.83	0.42	1.08	0.74	0.56	0.28
Technology	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.13 µm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS

where $PN(\Delta f)$ is the phase noise measured at Δf offset from f_0 carrier frequency, P_d the power consumption, and FTR the frequency tuning range.

4. CONCLUSION

In this paper, an integer-N quadrature frequency synthesizer fabricated in a 0.18 µm CMOS technology for UWB application is presented. In this synthesizer, to achieve excellent performance and great quadrature accuracy, a modified bottom-series structure with two symmetric coupled LC oscillators is adopted. To optimize the reference spur and phase noise performance, many spur suppression and phase noise improvement techniques are adopted in the circuit design. The measured results show outstanding spur suppression ability and good phase noise performance that validate the feasibility of these techniques.

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