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A Novel Interconnection Technique Using Zero-Degree Phase Shifting Microstrip TL for RF QFN Package at S-Band

Mohssin Aoutoul[1, *], Abderrahim Haddad[2], Mohammed Essaaidi[3], and Mustapha Faqir[4]

Abstract—In this paper, we propose a novel interconnection technique for a flip-chip quad flat no-lead (FC QFN) package which can decrease the amount of the transmission line (TL) phase shift. The RF die inputs and outputs (I/O) are connected to the package lead fingers by a small size, 1000 µm length, microstrip line having a gap capacitor consisting of staked plates (fingers) where the space in between is filled by a ceramic material of 10.2 dielectric constant value. This technique can reduce the effect of transmission line inductance and makes the novel package interconnection behaving as a composite left right handed (CLRH) TL; hence, one can set the TL phase shift to zero degree at the desired operating frequency band (i.e., S-band) by just tuning geometrical and/or physical interconnection structure parameters.

1. INTRODUCTION

RF packaging industry is gaining increasing interest due to extensive consumer's demand on microwave components for civilian RF and wireless industry as well as for military applications. A perfect electronic package is assumed to be, electrically, transparent and to keep the chip functionalities unchanged. However, packaging processes operating in microwave frequency range are still suffering because of electromagnetic phenomena such as reflections and signal retardation for high speed circuits [1].

Packaged microwave phase shifters are critical components in communication systems and phased array antennas used for radar systems. However, the conventional electronic packaging approach involves different interconnection techniques which are responsible of introducing additional phase shift because of the inevitable parasitic wire bond inductance, as an example, which depends on the wire bonding width and length. To remedy this problem, some techniques have been used to reduce the wire bonding effect such as double or multiple wire bond for an RF I/O or the use of ribbon bonding technique to reduce their inductance. Those techniques can significantly improve the return loss and insertion loss, but having an interconnection technique with zero degree phase shifting is still a dream [1].

Transmission lines with desired phase shifting at specific frequencies are still attracting more interest of academia and professional researchers. The ideal lossless left-handed transmission line (LH TL) having serial capacitance and shunt conductance layout design is one of the perfect solutions which actually absorbs extensive research effort; however, it is difficult to realise an equivalent layout design, with distributed element, of the ideal LH transmission line shown in Figure 1; hence, approximate designs able to present a positive phase shifting or similar behaviour have been proposed, guided by a circuit modeling process which tries to insert shunt conductance and serial capacitance. These transmission lines are known as L-C loaded transmission lines.

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* Corresponding author: Mohssin Aoutoul (aoutoul.m@ucd.ac.ma).
[1] STIC Lab., Physics Department, Faculty of Science, Chouaib Doukkali University (UCD), Morocco. [2] EIE Lab., Department of Physics, Faculty of Science, Chouaib Doukkali University El-Jadida, Morocco. [3] Higher National School of Computer and Systems Analysis (ENSIAS), Morocco. [4] School of Aerospace Engineering, Rabat International University (UIR), Morocco.

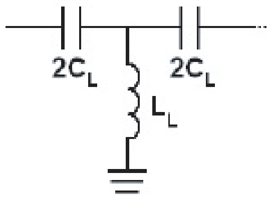


Figure 1. Unit cell for Left-Handed transmission line.

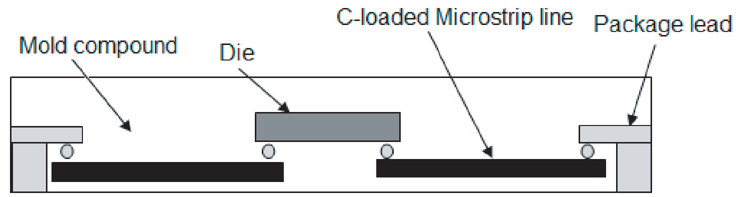


Figure 2. Envisaged RF QFN package with low phase shifting TL inside (C-Loaded MST line).

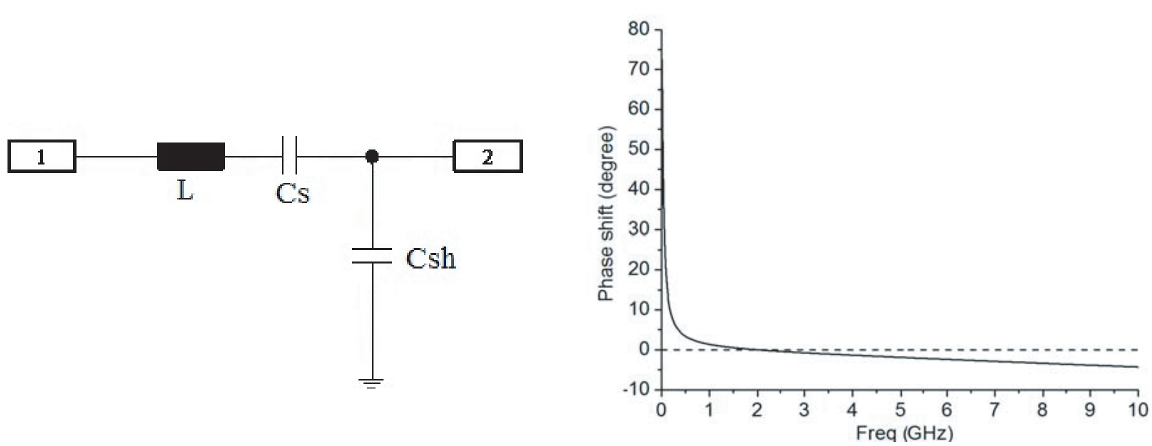
In this paper, we present a C-loaded microstrip line where the serial capacitance is a set of stacked stubs (fingers or plates) separated by a ceramic substance of 10.2 dielectric constant. Our aim is to design a very small size microstrip line for RF QFN package interconnection (Figure 2) with a controllable phase shifting parameter for a given frequency band by modifying the fingers' geometrical parameters (length, width) and/or their number.

First, a circuital model, having a similar response of a CRLH TL, has been proposed and studied using CST Design Studio; its optimal lumped elements values have been extracted. Then we have implemented this model in microstrip line distributed elements to design the equivalent 3D layout, and this interconnection structure has been simulated by the full wave EM CST MWS simulator. Results carried out by the two simulators have been discussed and compared in order to validate the feasibility of our proposed C-loaded microstrip interconnection design.

2. DESIGN APPROACH

As mentioned previously, our goal is to design an electrical interconnection technique, for electronic package, having very low phase shift at microwave bands using a C-loaded microstrip TL instead of the well-known wire bonding technique. So we began by discussing the feasibility of the circuital model shown in Figure 3(a), designed in CST Design Studio, for the following given circuit lumped element values, $C_{\text{serial}} = 50\,\text{pF}$ (C_{s}), $C_{\text{shunt}} = 0.01\,\text{pF}$ (C_{sh}) and $L = 0.1\,\text{nH}$. The simulated response of this transmission line, as shown in Figure 3(b), is excellent over the S-band frequency: $-0.3°$ at 2.5 GHz and $-1.3°$ at 4 GHz.

In the literature, many structure designs [2–7] have been proposed, where microstrip interdigital capacitor technique is widely used in RF transmission lines and filters. This technique requires larger TL sizes (few millimetres, up to some centimetres), but in the case of electronic package, where size



(a) (b)

Figure 3. (a) Loss less TL circuital model with serial capacitance (CST Design studio), $C_{\text{serial}} = 50\,\text{pF}$, $C_{\text{shunt}} = 0.01\,\text{pF}$ and $L = 0.1\,\text{nH}$, (b) simulated phase shift.

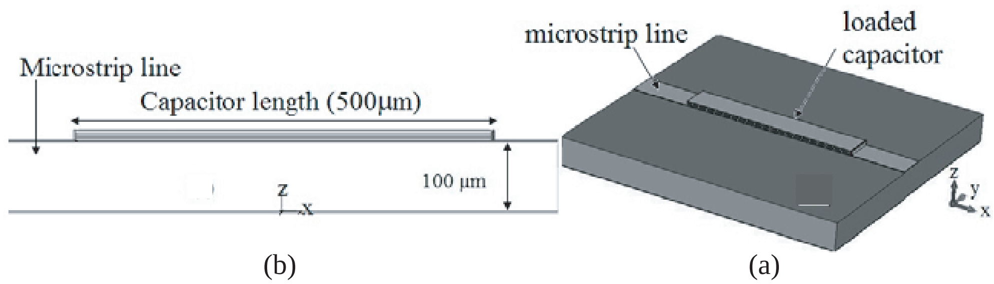


Figure 4. C-loaded Microstrip line with stacked capacitors strips (plates), (a) 3D view and (b) side view.

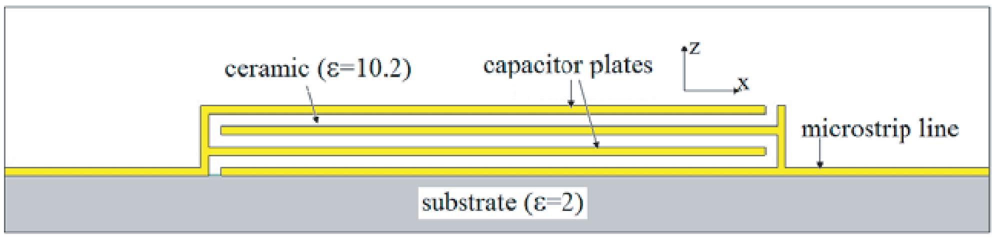


Figure 5. Four-plates stacked capacitor of Figure 4(b).

is a hard constraint, these structures are not appropriate. Reducing the size of interdigital capacitor component leads to lower capacitance values which is reflected by a high return loss values and very low insertion loss values making the interconnecting structure behaving as a reject band filter and not useful for low band frequencies such as S-band. The solution idea, proposed in this paper, is to insert a serial capacitor in microstrip transmission line, as stacked plates portions separated by an insulating ceramic substance of 10.2 dielectric constant value, to form a serial loaded microstrip capacitor with high capacitance value as shown in Figures 4 and 5. The capacitance value can be controlled by increasing the number of fingers, the capacitor length/width, or by increasing the material dielectric constant between the fingers (plates).

The microstrip line shown in Figure 4(b) has 1000 μm length, 100 μm width. The capacitance component has 500 μm length formed with 4 stacked microstrip (plates) pieces, and the ceramic thickness is 3 μm (Figure 5).

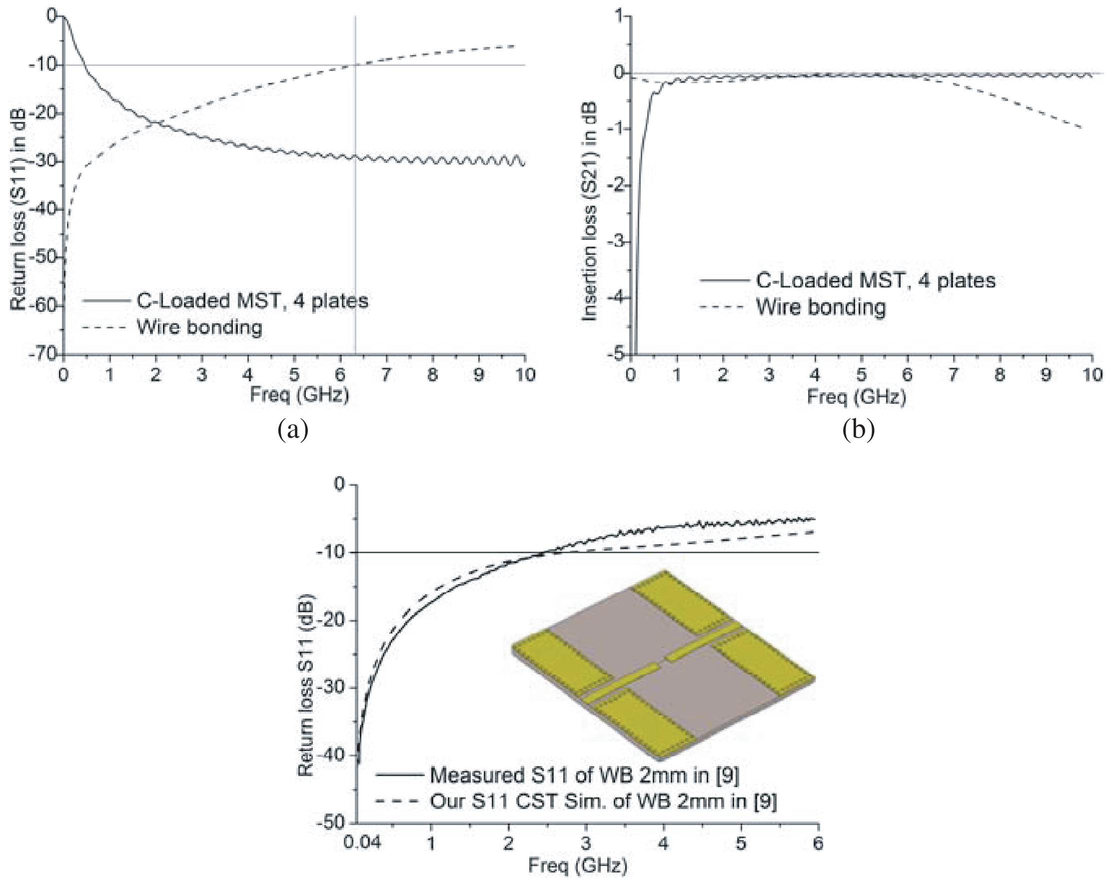
3. RESULTS AND DISCUSSION

3.1. Return Loss Parameter

In the case of electronic packaging operating at microwave frequencies bands or higher, the return loss and insertion loss are critical parameters which validate the feasibility of any involved interconnection structures. Figures 6(a), (b) illustrate a comparison in term of S-parameters (S_{11} should be less than -10 dB) between the wire-bonding technique and the proposed serial C-loaded microstrip technique. The gain of the proposed technique is approximately flat and closer to zero at the frequency band of interest. Theoretically, the last interconnection method seems to offer an unlimited impedance bandwidth [8]. To confirm our computed results, we have simulated a similar wire bonding (WB) of 2 mm length where the measured return loss result is reported in [9]. Figure 6(c) shows that our recent CST simulated results are in good agreement with the measured ones.

3.2. Phase Shift Parameter Comparison and Group Delay

Since the aim of this study is to present a packaging interconnection technique having negligible phase shift over S-band, the phase shifting parameter of the proposed interconnection versus frequency is



(a) (b) (c)

Figure 6. Simulated (a) return loss S_{11}, (b) insertion loss S_{21} of a WB and the C-loaded TL having the same length 1 mm, and (c) S'_{11} newly simulated result and extracted measures of the WB, 2 mm, from [9].

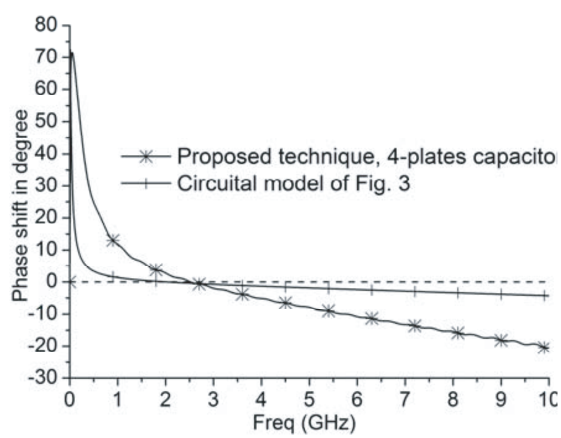


Figure 7. EM Simulated phase shift parameter of 4-plates and 500 μm length capacitor vs. circuital model.

illustrated in Figure 7. The structure behaves as a composite right left handed (CRLH) transmission line [10], and the results are encouraging despite the slight difference compared to those obtained for circuital model simulation. As confirmed by the results of Figure 8(a), this is due to lower capacitance value of our proposed serial stacked capacitor than the C_s value (50 pF) used in the circuit model. Figure 8(a) shows the results of a parametric study where the number of capacitor plates has been increased from two to four in order to increase the serial capacitance. Very good effect on the phase

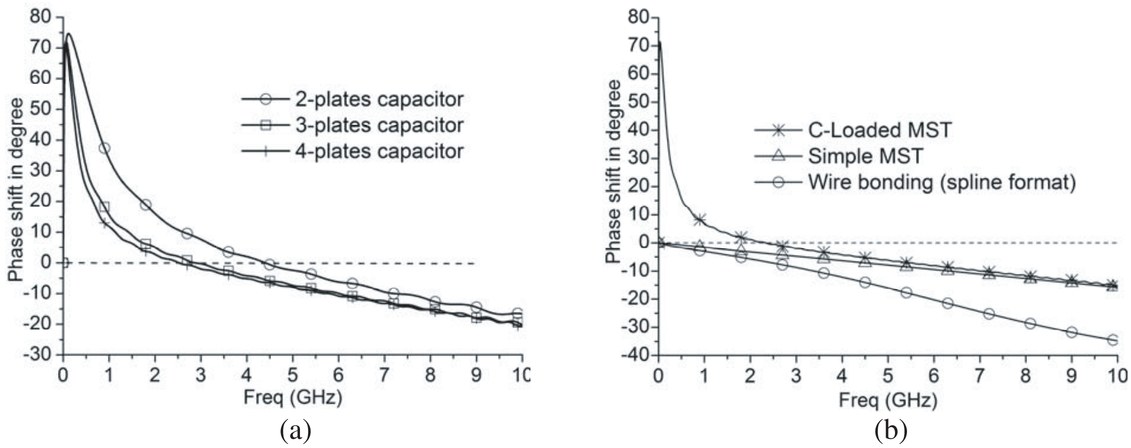


Figure 8. Simulated phase shift parameter vs. frequency for: (a) different fingers (plates) number, (b) three interconnection methods having the same length = 1000 µm.

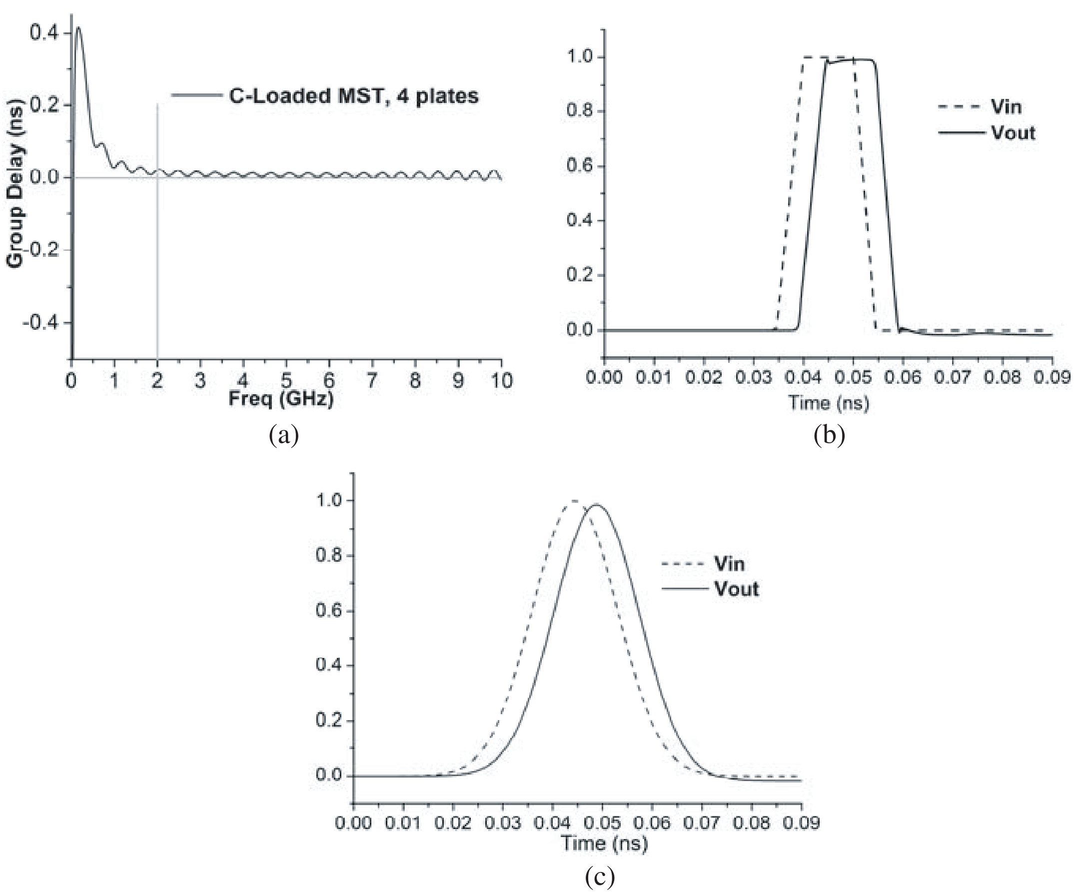


Figure 9. (a) Group delay of the proposed design, (b) and (c) schematic showing input/output signal waveforms for the proposed RF package interconnection technique for trapezoidal and Gaussian-type signals.

shift's sloop parameter is observed for higher capacitor plates' number. Results can be improved by using capacitor's insulating material with higher dielectric constant, or/and increasing the length and width of its plates.

Figure 8(b) presents the phase shift parameter of three interconnection techniques having the same length (1000 μm): a wire bonding with a spline format, an ordinary microstrip line, and a C-loaded microstrip line. The proposed interconnection structure offers more advantages in term of stable and controllable phase shift parameter values around 2.4 GHz.

The calculated group delay (GD), using the differential-phase GD relation and the full-wave simulated time domain response have been plotted in Figure 9. Throughout the frequency range of interest, the GD is nearly flat while presenting very small positive ripples with values less than 0.03 ns. The computed output signal versus the input one (Figures 9(b) and 9(c)), in time-domain, is excellent and shows a time delay about 0.0043 ns for both output signal responses.

4. CONCLUSIONS

In this paper, a novel interconnection technique for flip-chip quad flat no-lead (FC QFN) package is presented. The bandwidth's upper frequency, where the return loss is less than −10 dB, is unlimited (theoretically), and the amount of the TL phase shift can be decreased significantly compared to conventional techniques and can be adjusted to zero-degree for a given operating frequency band. This structure has a simple design and behaves as a composite right left handed transmission line.

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