*Progress In Electromagnetics Research M, Vol. 57, 81–89, 2017*

# A Small-Signal Analysis Based Thermal Noise Modeling Method for RF SOI MOSFETs

**Xiang Wang, Yu Ping Huang, Jun Liu*, and Jie Wang**

**Abstract**—We investigate thermal noise mechanisms and present analytical expressions of the noise power spectral density at high frequencies (HF) in Silicon-on-insulator (SOI) MOSFETs. The developed HF noise model of RF T-gate body contact (TB) SOI MOSFET for 0.13-μm SOI CMOS technology accounts for the mechanisms of 1) channel thermal noise; 2) induced gate noise; 3) substrate resistance noise and 4) gate resistance thermal noise. The extraction method of modeling parameter utilized by $Y$-parameter analysis on the proposed small-signal equivalent circuit is demonstrated in this paper. Excellent agreement between simulated and measured noise data is obtained at different temperatures.

## 1. INTRODUCTION

SOI technology has been considered as a potential technology for low-power microwave circuits due to its excellent RF performance such as gain, speed, and cutoff frequency ($f_T$) [1]. It is prerequisite for the application of modern SOI technologies in RF circuits to better understand noise mechanisms [2–5]. For the applications in low noise CMOS RF circuits such as low noise amplifier (LNA), accurate modeling of noise is quite important. In the past decade, HF noise characterization and modeling for bulk and floating body SOI MOSFETs has been widely studied [6–15], and some modeling methods have been proposed. In [16], the authors proposed a channel segmentation model for accurate channel noise by several independent MOS model. In [17], the author presented a physical understanding of both intrinsic and extrinsic noise mechanisms in a MOSFET [18], a simple analytical model for the thermal channel noise of deep-submicron MOS transistors including hot carrier effects. However, the HF noise model of TB SOI MOSFET is rarely presented and discussed. Accurate physical-based noise model is needed to shorten the design cycle.

To HF noise modeling, the small signal circuit parameters and noise sources play important roles. In Section 3, we perform an extensive study of the noise mechanisms at high frequencies. The small signal equivalent circuit and parameter extraction techniques for TB SOI MOSFET are presented. In Section 4, we model the total drain-current noise, the gate-current noise, their cross-correlation and the four noise parameters. Finally, experimental verifications of the derived noise model are given at different temperatures.

## 2. PROPOSED DEVICE STRUCTURE

To suppress floating body effect (FBE), body contacts with different structures have been proposed. In this paper, multi-finger PD SOI nMOSFETs with TB structure are investigated. For a TB device, $P+$ implantation is performed to form the $P+$ body contact area. At one end of the T-type gate, a $P+$ injection region is connected to the P-type body region. Because of the $P+$ body contact area is connected with the ground, the hole produced by the impact ionization can be released from the body region in order to eliminate the Kink effect. The layout of TB SOI nMOSFET is shown in Fig. 1.

*Received 6 March 2017, Accepted 24 May 2017, Scheduled 2 June 2017*

* Corresponding author: Jun Liu (ljun77@hdu.edu.cn).

The authors are with the Key Laboratory for RF Circuits and Systems of Ministry of Education, Hangzhou Dianzi University, Hangzhou, China.

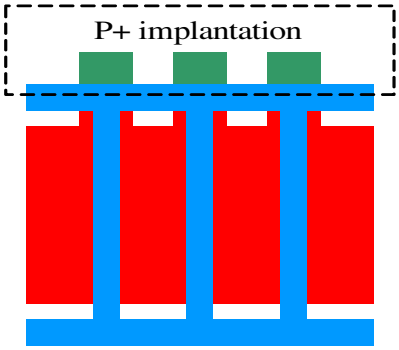


**Figure 1.** Top view of the proposed TB SOI nMOSFET structure.

## 3. MODEL PARAMETER EXTRACTION

A simplified small-signal equivalent circuit with the associated noise sources of TB SOI MOSFET is proposed in Fig. 2. $R_g$, $R_s$, $R_d$ are gate resistance, source resistance, and drain resistance, respectively. $G_{ds}$ is the ac drain conductance and $G_m$ the ac transconductance. $C_{ds}$, $C_{gs}$ and $C_{gd}$ are drain-to-source capacitance, gate-to-source capacitance and gate-to-drain capacitance, respectively.

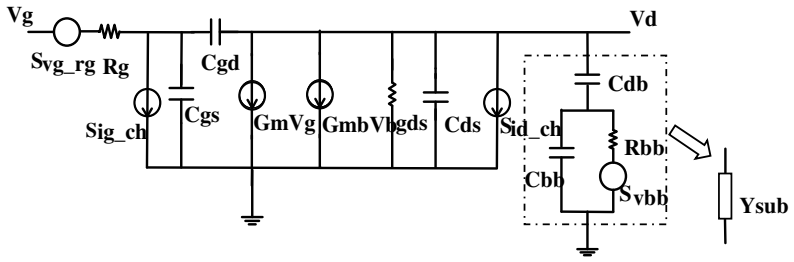


**Figure 2.** SOI MOSFET simplified small-signal equivalent circuit including the relevant noise sources.

In order to verify the accuracy of the proposed noise model at different temperatures, on-wafer two-port high-frequency scattering parameters ($S$ parameters) and noise figure (NF) under ultra-low temperatures are measured from 1 to 20 GHz with a step size of 1 GHz by Université de Bordeaux. We use an accurate parameter-extraction approach [19] to get $Y$-parameters from deembedded $S$-parameters. The higher order terms of $\omega R_X C_X$ are too small to be neglected in the measurement frequency range. $Y$-parameter analysis on the proposed small-signal equivalent circuit can be approximated as follows:

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \approx \omega^2 \left(C_{gd}+C_{gs}\right)^2 R_g + j\omega\left(C_{gd}+C_{gs}\right) \tag{1}$$

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \approx -\omega^2 C_{gd}\left(C_{gd}+C_{gs}\right) R_g - j\omega C_{gd} \tag{2}$$

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \approx G_m - j\omega\left(C_{gd}+C_{gs}\right) R_g G_m \tag{3}$$

$$Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \approx Y_{sub} + G_{ds} + j\omega\left(C_{gd}+C_{gs}\right) + G_{mb}\left[\frac{V_{bs}}{V_{ds}}\right] \tag{4}$$

$$\left[\frac{V_{bs}}{V_{ds}}\right] = Y_{sub}\left[\frac{\left(1-j\omega R_{bb}C_{bb}\right)R_{bb}}{1+\omega^2 R_{bb}^2 C_{bb}^2}\right] \tag{5}$$

For the extraction of substrate components, $Y_{sub}$ can be defined as follows:

$$Y_{sub} = \frac{\omega^2 R_{bb} C_{db}^2 + j\omega C_{db} + j\omega^3 R_{bb} C_{db} C_{bb} \left(C_{db} + C_{bb}\right)}{1 + \omega^2 R_{bb}^2 \left(C_{db} + C_{bb}\right)^2} \tag{6}$$

All the components of the equivalent circuit can be extracted by the $Y$-parameter analysis. $G_m$, $G_{ds}$, $R_g$, $C_{gd}$, $C_{gs}$ and $C_{ds}$ are expressed as.

$$G_m \approx \mathrm{Re}\left[Y_{21}\right]|_{\omega^2=0} \tag{7}$$

$$G_{ds} \approx \mathrm{Re}\left[Y_{22}\right]|_{\omega^2=0} \tag{8}$$

$$R_g \approx \frac{\mathrm{Re}\left[Y_{11}\right]}{\mathrm{Im}\left[Y_{11}\right]^2} \tag{9}$$

$$C_{gd} \approx -\frac{\mathrm{Im}\left[Y_{12}\right]}{\omega} \tag{10}$$

$$C_{gs} \approx \frac{\mathrm{Im}\left[Y_{11}\right] + \mathrm{Im}\left[Y_{12}\right]}{\omega} \tag{11}$$

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{22}\right)}{\omega} - G_{ds} \tag{12}$$

$R_{bb}$, $C_{bb}$ and $C_{db}$ can be derived as [13]. In this paper, we simplify the extraction that $R_{bb}$ is obtained from the slope of the relationship for $\omega^2/\mathrm{Re}[Y_{sub}]$ versus $\omega^2$ as follows:

$$\frac{\omega^2}{\mathrm{Re}\left[Y_{sub}\right]} = \omega^2 R_{bb} + \frac{1}{R_{bb} C_{db}^2} \tag{13}$$

$C_{db}$ is extracted from (13) as follows:

$$C_{db} = \left(\frac{\omega^2 R_{bb}}{\mathrm{Re}\left[Y_{sub}\right]} - \omega^2 R_{bb}^2\right)^{-\frac{1}{2}} \tag{14}$$

In this paper, the parameter-extraction technique is performed using multi-finger PD SOI nMOSFETs with TB structure of the channel length $L = 0.13\,\mu\mathrm{m}$, channel width $W = 5\,\mu\mathrm{m}$ and number of fingers $N = 4$ at a biasing condition of $V_{gs} = 0.8\,\mathrm{V}$, $V_{ds} = 1.2\,\mathrm{V}$. The cryogenic DC performance and small signal AC performance of PD SOI nMOSFETs with TB structure can refer to [20, 21]. As shown in Fig. 3, the simulated $Y$-parameters are found to agree well with the measured $Y$-parameters which indicates that the proposed small-signal equivalent circuit model can describe linear two-port characteristics commendably. The small signal parameters extracted at 300 K and 77 K are enumerated in Table 1. The decrease in the gate resistance $R_g$ at 77 K is due to lower poly/silicide resistances at low temperatures. The capacitances are almost invariant with temperature. $G_m$ and $G_{ds}$ increase with decrease in temperature, largely due to increase in the effective mobility.

**Table 1.** Values of the extracted model parameters biased at $V_{gs} = 0.8\,\mathrm{V}$, $V_{ds} = 1.2\,\mathrm{V}$, at 300 K and 77 K.

| Temperature | $R_g$ | $C_{gs}$ | $C_{gd}$ | $C_{ds}$ | $G_m$ | $G_{ds}$ |
|---|---|---|---|---|---|---|
| 300 K | 47.5 Ω | 20.5 fF | 10.36 fF | 13.8 fF | 13.5 mS | 2.06 mS |
| 77 K | 36.3 Ω | 18.9 fF | 10.03 fF | 10.67 fF | 21.2 mS | 2.53 mS |

## 4. HIGH-FREQUENCY NOISE MODEL

The MOSFET $1/f$ noise becomes negligible, and thermal noise is the dominant source of device noise at high frequencies. As the small-signal equivalent circuit already describes the linear two-port characteristics, the total drain-current noise $S_{id}$, total gate-current noise $S_{ig}$ and their cross-correlation

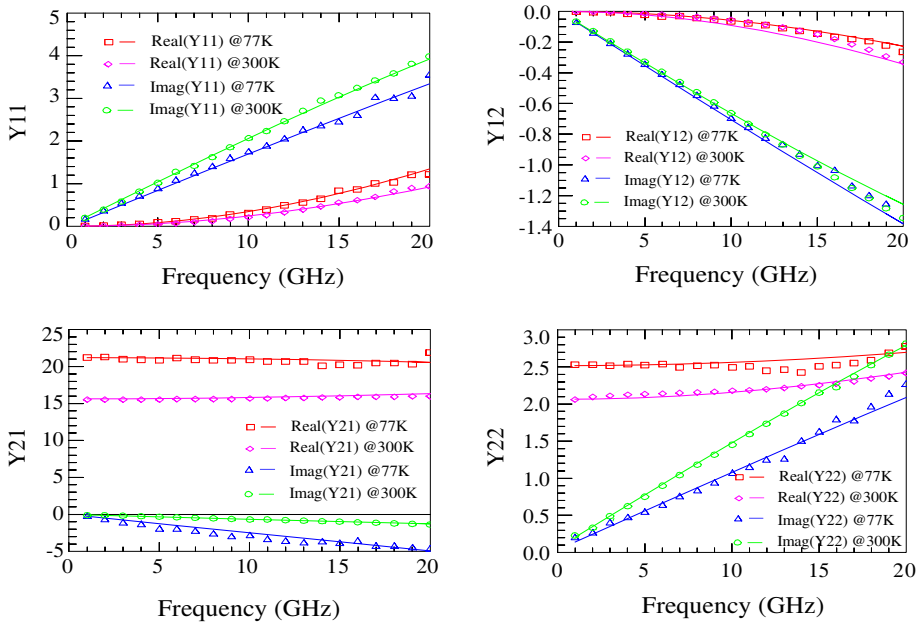


**Figure 3.** Extracted (symbols) and simulated (lines) $Y$-parameters versus frequency.

$S_{igid*}$ are required, and the noise performance of any noisy two-port network can be represented by Eq. (15).

$$NF = NF_{\min} + \frac{R_n}{G_s} |Y_s - Y_{opt}|^2 \tag{15}$$

$NF$ is the noise figure, $NF_{\min}$ the minimum noise figure, $R_n$ the equivalent noise resistance, $Y_{opt}$ $(= G_{opt} + j * B_{opt})$ the optimum source admittance that results in $NF_{\min}$, and $Y_s$ $(= G_s + j * B_s = 50)$ the source admittance.

### 4.1. Channel Thermal Noise

The channel thermal noise induced by the random motion of the carriers in the inversion channel of the MOS transistor is the main contribution to the drain current noise power spectral density (PSD) [22]. The channel thermal noise model is developed based on Tsividis' method [23], and the linear part of channel is divided into small sections of length $\Delta y$ as shown in Fig. 4. However, Tsividis cannot consider the impact of channel length modulation (CLM), velocity saturation effect (VSE) and hot carrier effect (HCE) [24–26]. In addition, experimental results indicate that GCR (gradual channal region) significantly contribute to the channel thermal noise [27]. Fig. 5 shows a detailed schematic indicating the partition in the GCR and velocity saturation region (VSR), which is used in the noise analysis. The negligible contribution from the VSR can be attributed to the fact that carriers travel at constant velocity and therefore are insensitive to channel voltage random fluctuations [28]. With consideration of these effects [29], the channel thermal noise can be derived,

$$S_{id\_ch} = \frac{4kT}{I_{DS}} \left[ \frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DS_{eff}}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DS_{eff}}} \left( 1 + \frac{V_{DS_{eff}}}{E_c L_{eff}} \right) \times \left[ Q'_I (V_y) \right]^2 dV_y \tag{16}$$

$Q'_I(V_y) = C'_{ox}(V_{GT} - \alpha V_y)$ is the inversion layer charge density. $C'_{ox}$ is the gate capacitance per unit area. $k$ is Boltzmann's constant. $\alpha$ is the bulk charge effect coefficient, $\mu_{eff}$ the effective mobility of the carrier, $L_{eff} = L - dL$ the length of the gradual channel region, and $V_{DSeff}$ the drain bias smoothening function, which are obtained from BSIMSOI4. $E_y$ is the lateral electric field and $E_c$ the critical electric field.

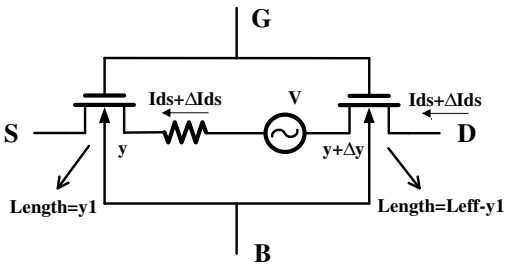


**Figure 4.** Thevenin equivalent circuit.

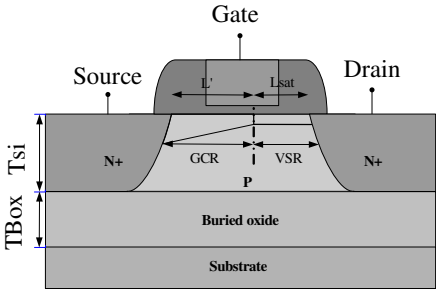


**Figure 5.** Cross-sectional view of SOI MOSFETs indicating the GCR and the VSR.

The channel thermal noise can be derived as follow:

$$S_{id\_ch} = 4kT\left(\frac{W}{L_{eff}}\mu_{eff}C'_{ox}\right) \times \left(\frac{V_{GT}^2 - \alpha V_{GT}V_{DS_{eff}} + \frac{\alpha^2}{3}V_{DS_{eff}}^2}{V_{GT} - \frac{\alpha}{2}V_{DS_{eff}}}\right) \tag{17}$$

### 4.2. Induced Gate Noise

The channel thermal noise is coupled to the gate terminal through the gate capacitance, resulting in the induced gate noise. The magnitude of this noise is directly proportional to the frequency as the earlier work by van der Ziel [30], and the induced gate noise was modeled for a MOSFET by Shoji [31] that treated the channel as an active distributed $RC$ transmission line. Based on [13, 30], we consider the gradual channel approximation, and the induced gate noise spectral density can be obtained,

$$S_{ig\_ch} = \omega^2 W^2 C'^2_{ox}\left(\frac{L_{eff}^2}{I_{DS}^2}\right)\left(\frac{4kT}{I_{DS}}\right)\left[\frac{\frac{W}{L_{eff}}\mu_{eff}}{1+\frac{V_{DS_{eff}}}{E_c L_{eff}}}\right]^2 \times \int_0^{V_{DS_{eff}}}\left(1+\frac{E_y}{E_c}\right)Q'^2_I\left[V_{as}-V_y\right]^2 dV_y \tag{18}$$

With $V_{as} = V_{DS_{eff}} + \frac{1}{E_c L_{eff}}\left(\frac{V_{DS_{eff}}^2}{2}\right) - \left(1+\frac{V_{DS_{eff}}}{E_c L_{eff}}\right)\left(\frac{\frac{1}{2}V_{GT}V_{DS_{eff}} - \frac{\alpha}{6}V_{DS_{eff}}^2}{V_{GT}-\frac{\alpha}{2}V_{DS_{eff}}}\right)$.

By integrating Eq. (18) over the whole channel, the induced gate noise spectral density is given as,

$$S_{ig\_ch} = \frac{4kT\omega^2 W^4 C'^4_{ox}\mu_{eff}^2}{I_{DS}^3}\left(\frac{1}{1+\frac{V_{DS_{eff}}}{E_c L_{eff}}}\right) \times \left[\frac{\alpha^2}{5}V_{DS_{eff}}^5 - \frac{\alpha}{2}\left(\alpha V_{as}+V_{GT}\right)V_{DS_{eff}}^4\right.$$
$$\left. + \frac{1}{3}\left(\alpha^2 V_{as}^2 + 4\alpha V_{as}V_{GT} + V_{GT}^2\right)V_{DS_{eff}}^3 - V_{as}V_{GT}\left(\alpha V_{as}+V_{GT}\right)V_{DS_{eff}}^2 + V_{GT}^2 V_{as}^2 V_{DS_{eff}}\right] \tag{19}$$

### 4.3. Substrate Resistance Noise

According Jindal's original analysis [32], the thermal voltage fluctuations across the total distributed substrate resistance Rbb induces a fluctuating substrate potential, and these random variations are coupled to the FET channel. Based on Nyquist's assertion of thermal noise [33], the noise voltage spectrum can be adequately described by Equation (15) and coupled to the channel through the back-gate (substrate) transconductance $G_{mb}$.

$$S_{vbb} = 4kTR_{bb} \tag{20}$$

$$S_{id\_sub} = 4kTR_{bb} \times \frac{G_{mb}^2}{1+\omega^2 C_b^2 R_{bb}^2} \tag{21}$$

The thermal noise generated in the substrate network is coupled to the gate terminal through the gate–bulk capacitance $C_{gb}$, resulting in gate-current noise $S_{ig\_sub}$. Due to the small $C_{gb}$, $S_{ig\_sub}$ can be negligible. Effective substrate capacitance $C_b$ is approximately equal to the channel-substrate series capacitance. Due to the thick buried oxide (BOX) in SOI MOSFET, $C_b$ is approximately equal to $C_{db}$. The noise contribution from the substrate resistance can be reduced by using a high resistive substrate ($R_{bb} \to \infty$) or a "metallic" substrate ($R_{bb} \to 0$).

### 4.4. Gate Resistance Thermal Noise

When the device transconductance approximates the conductance of the resistive gate, the resistive gate becomes important and can be a significant contributor to noise. Thornber [34] first proposed a solution to this problem for a simple gate geometry. In fact, typical IC layouts are far more complex, so Jindal developed new formulation with many effects [35]. Like any other AC signal, the voltage noise across the gate resistance can be amplified to the drain through transconductance $G_m$. An additional drain current noise can be derived as Eq. (22). At high frequency, the gate-current noise due to the voltage noise across the gate resistance cannot be recognized [35] and can be obtained as Eq. (23).

$$S_{id\_Rg} = 4kTR_gG_m^2 \tag{22}$$

$$S_{ig\_Rg} = 4kTR_g\omega^2C_{gg}^2 \tag{23}$$

### 4.5. Correlation between Drain-Current Noise and Gate-Current Noise

Since the noise sources of the channel current noise $S_{id\_ch}$ and channel-induced gate noise $S_{ig\_ch}$ are both from the channel, $S_{id\_ch}$ and $S_{ig\_ch}$ are correlated, and this noise correlation can be given by,

$$S_{igid^*\_ch} = j\omega WC'_{ox}\left(\frac{L_{eff}}{I_{DS}}\right)\left(\frac{4kT}{I_{DS}}\right)\left[\frac{\dfrac{W}{L_{eff}}\mu_{eff}}{1+\dfrac{V_{DS_{eff}}}{E_cL_{eff}}}\right]^2 \times \int_0^{V_{DS_{eff}}}\left(1+\frac{E_y}{E_c}\right)Q_I^{'2}\left[V_{as}-V_y\right]^2dV_y \tag{24}$$

$$\begin{aligned} S_{igid^*\_ch} = {} & \frac{4kT\omega W^3C_{ox}^{'3}\mu_{eff}^2}{L_{eff}I_{DS}^3}\left(\frac{1}{1+\dfrac{V_{DS_{eff}}}{E_cL_{eff}}}\right)\times\left[-\frac{1}{4}V_{DS_{eff}}^4+\frac{\alpha}{3}\left(\alpha V_{as}+2V_{GT}\right)V_{DS_{eff}}^3\right. \\ & \left.-\frac{(V_{gs}-V_{th})}{2}\left(2\alpha V_{as}+V_{gs}-V_{th}\right)V_{DS_{eff}}^2+\left(V_{gs}-V_{th}\right)^2V_{as}\left(\alpha V_{as}+V_{GT}\right)V_{DS_{eff}}\right] \end{aligned} \tag{25}$$

The contributions of the gate resistance to drain current and gate current noise are correlated, and the correlation is expressed as [36]:

$$S_{igid^*\_Rg} = j4kT\omega C_{gg}R_gG_m \tag{26}$$

Based on the calculated noise sources, we can summarize the total drain-current noise $S_{id}$, total gate-current noise $S_{ig}$ and their cross-correlation $S_{igid^*}$.

$$S_{id} = S_{id\_ch} + S_{id\_rg} + S_{id\_sub} \tag{27}$$

$$S_{ig} = S_{ig\_ch} + S_{ig\_rg} \tag{28}$$

$$S_{igid^*} = S_{igid^*\_ch} + S_{igid^*\_rg} \tag{29}$$

In the end, the four noise parameters can be modeled from the noise power spectral density [37].

$$R_n = \frac{S_{id}}{4kT|Y_{21}|^2} \tag{30}$$

$$B_{opt} = -B_{cor} = \frac{S_{igid^*}\mathrm{Re}\left[Y_{21}\right]}{4kTR_n\left|Y_{21}\right|^2} - \mathrm{Im}\left[Y_{11}\right] \tag{31}$$

$$G_{opt} = \left(|Y_{opt}|^2 - B_{opt}^2\right)^{\frac{1}{2}} = \left[\frac{S_{ig}}{4kTR_n} - |Y_{11}|^2 + 2\left(\mathrm{Re}\left[Y_{11}\right]G_{cor} + \mathrm{Im}\left[Y_{11}\right]B_{cor}\right) - B_{opt}^2\right]^{\frac{1}{2}} \tag{32}$$

$$G_{cor} = \mathrm{Re}\left[Y_{11}\right] + \frac{S_{igid^*}\mathrm{Im}\left[Y_{21}\right]}{4kTR_n\left|Y_{21}\right|^2} \tag{33}$$

$$F_{\min} = 1 + 2R_n\left(Y_{opt} + Y_{cor}\right) = 1 + 2R_n\left(G_{opt} + G_{cor}\right) \tag{34}$$

Extracted total drain-current noise $S_{id}$, total gate-current noise $S_{ig}$ and their cross-correlation $S_{igid^*}$ versus frequency for different temperatures are shown in Fig. 6. A positive temperature coefficient of the NF extracted in Eq. (15) versus temperature can be seen in Fig. 7. The good fitting results prove the accuracy of the proposed noise model.

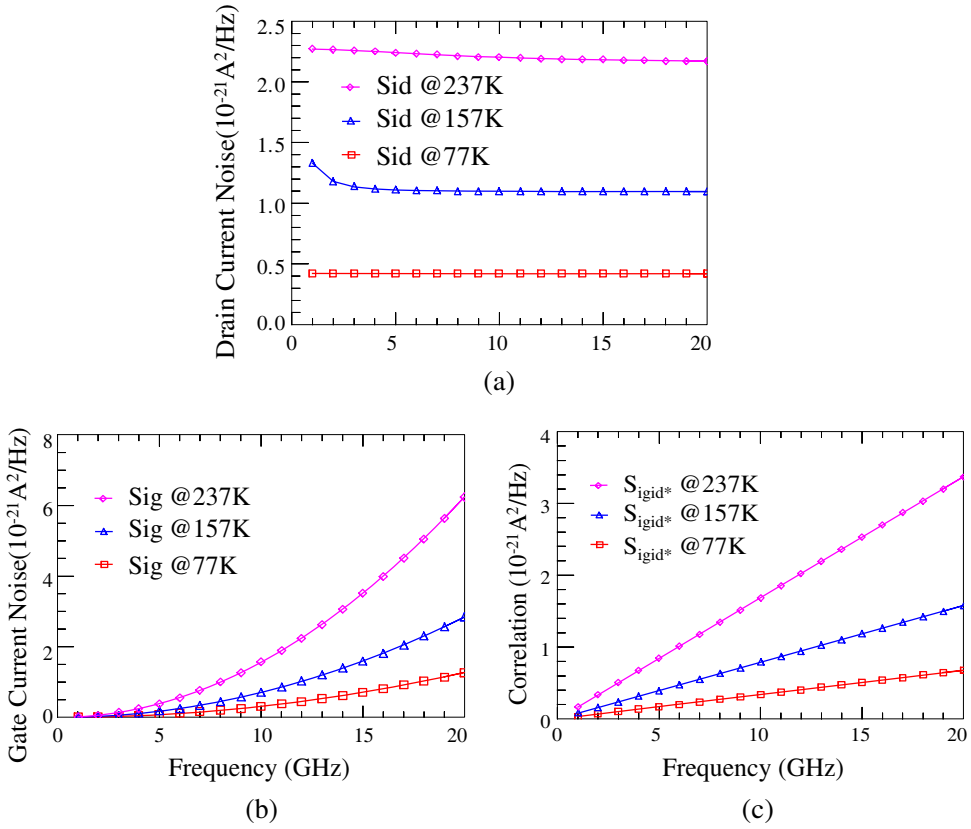


**Figure 6.** Extracted noise power spectral density versus frequency at 77 K, 157 K and 237 K. (a) Total drain-current noise, (b) total gate-current noise Sig, (c) cross-correlation.

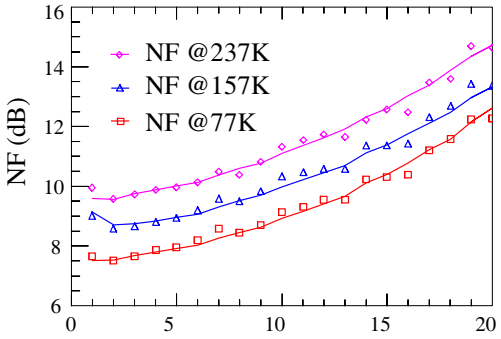


**Figure 7.** Extracted (symbols) and simulated (lines) values of the noise figure NF versus frequency at 77 K, 157 K and 237 K.

## 5. CONCLUSION

A thermal noise modelling method for RF SOI MOSFETs is developed based on small signal analysis. The model parameter-extraction technique is demonstrated by utilizing $Y$-parameter analysis on the proposed small-signal equivalent circuit. Excellent agreement between the simulated and measured data of 0.13 μm TB SOI nMOSFETs is obtained, which indicate that the proposed noise equivalent circuit model is accurate, and its parameter-extraction method is reliable.

## ACKNOWLEDGMENT

This work was supported in part by the Zhejiang Provincial Natural Science Foundation of China (LQ15F010005), and by the National Natural Science Foundation of China (No. 61372021).

## REFERENCES

1. Lee, B. J., K. Kim, C. G. Yu, et al., "Effects of gate structures on the RF performance in PD SOI MOSFETs," *IEEE Microwave & Wireless Components Letters*, Vol. 15, No. 4, 223–225, 2005.
2. Scholten, A. J., L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, Vol. 50, No. 3, 618–632, Mar. 2003.
3. Smit, G. D. J., A. J. Scholten, R. M. T. Pijper, et al., "RF-noise modeling in advanced CMOS technologies," *IEEE Trans. Electron Devices*, Vol. 61, No. 2, 245–254, 2014.
4. Mukherjee, C. and C. K. Maiti, "Channel thermal noise modeling and high frequency noise parameters of tri-gate FinFETs," *IEEE Physical and Failure Analysis of Integrated Circuits*, 732–735, 2013.
5. Chan, L. H. K., K. S. Yeo, K. W. J. Chew, et al., "High-frequency noise modeling of MOSFETs for Ultra low-voltage RF applications," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 63, No. 1, 141–154, 2015.
6. Chen, C.-H., M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements," *IEEE Trans. Electron Devices*, Vol. 48, No. 12, 2884–2892, Dec. 2001.
7. Antonopoulos, A., M. Bucher, K. Papathanasiou, et al., "CMOS small-signal and thermal noise modeling at high frequencies," *IEEE Trans. Electron Devices*, Vol. 460, No. 11, 3726–3733, 2013.
8. Chen, C., "Accuracy issues of on-wafer microwave noise measurement," *Fluctuation & Noise Letters*, Vol. 48, No. 03n04, L281–L303, 2012.
9. Chalkiadaki, M. A. and C. C. Enz, "RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 463, No. 7, 1–12, 2015.
10. Chen, C. H., D. Chen, R. Lee, et al., "Thermal noise modeling of nano-scale MOSFETs for mixed-signal and RF applications," *IEEE Custom Integrated Circuits Conference*, 1–8, 2013.
11. Ong, S. N., "High frequency noise modeling of deep-submicron MOSFETs," Ph.D. Thesis, NTU, 2015, https://repository.ntu.edu.sg/bitstream/handle/10356/63701/High?sequence=1.
12. Deen, M. J., C.-H. Chen, S. Asgaran, G. A. Rezvani, J. Tao, and Y. Kiyota, "High-frequency noise of modern MOSFETs: Compact modeling and measurement issues," *IEEE Trans. Electron Devices*, Vol. 53, No. 9, 2062–2081, Sep. 2006.
13. Ong, S. N., et al., "Substrate-induced noise model and parameter extraction for high-frequency noise modeling of sub-micron MOSFETs," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 62, No. 9, 1973–1985, 2014.
14. Adan, A. O., M. Koyanagi, and M. Fukumi, "Physical model of noise mechanisms in SOI and bulk-silicon MOSFETs for RF applications," *IEEE Trans. Electron Devices*, Vol. 55, No. 3, 872–880, Sep. 2008.

15. Wang, S. C., et al., "Investigation of temperature-dependent high-frequency noise characteristics for deep-submicrometer bulk and SOI MOSFETs," *IEEE Trans. Electron Devices*, Vol. 59, No. 3, 551–556, 2012.
16. Scholten, A. J., L. F. Tiemeijer, R. Van Langevelde, et al., "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, Vol. 50, No. 3, 618–632, 2003.
17. Jindal, R. P., "Compact noise models for MOSFETs," *IEEE Trans. Electron Devices*, Vol. 53, No. 9, 2051–2061, 2006.
18. Knoblinger, G., P. Klein, and H. Tiebout, "A new model for thermal channel noise of deep-submicron MOSFETs and its application in RF-CMOS design," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 5, 831–837, 2001.
19. Ickjin, K., J. Minkyu, L. Kwyro, and S. Hyungcheol, "A simple and analytical parameter-extractionmethod of a microwave MOSFET," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 50, No. 6, 1503–1509, Jun. 2002.
20. Venkataraman, S., B. Banerjee, C. H. Lee, et al., "Cryogenic small signal operation of 0.18 µm MOSFETs," *2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 52–55, 2007.
21. Chen, S., C. Cai, T. Wang, et al., "Cryogenic and high temperature performance of 4H-SiC power MOSFETs," *IEEE Applied Power Electronics Conference & Exposition*, 207–210, 2013.
22. Scholten A. J., et al., "Accurate thermal noise model for deep-submicron CMOS," *IEDM Tech. Dig.*, 155–158, Dec. 1999.
23. Tsividis, Y., *Operation and Modeling of the MOS Transistor*, 2nd Edition, WCB/McGraw-Hill, Boston, 1999.
24. Chen, C. H. and M. J. Deen, "High frequency noise of MOSFETs I modeling," *Solid-State Electron*, Vol. 42, 2069–81, 1998.
25. Jeon, J., J. D. Lee, B.-G. Park, and H. Shin, "An analytical channel thermal noise model for deep-submicron MOSFETs with short channel effects," *Solid-State Electron*, Vol. 51, 1034–8, 2007.
26. Han, K., H. Shin, and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs," *IEEE Trans. Electron Devices*, Vol. 51, No. 2, 261–9, 2004.
27. Scholten, A. J., et al., "Accurate thermal noise model for deep-submicron CMOS," *IEDM Tech. Dig.*, 155–158, Dec. 1999.
28. Chen, C.-H. and M. J. Deen, "Channel noise modeling of deep submicron MOSFETs," *IEEE Trans. Electron Devices*, Vol. 49, No. 8, 1484–1487, Aug. 2002.
29. Ong, S. N., et al., "Impact of velocity saturation and hot carrier effects on channel thermal noise model of deep sub-micronMOSFETs," *Solid State Electron*, Vol. 72, 8–11, 2012.
30. Van Der Ziel, A., *Noise in Solid State Devices and Circuits*, Wiley, New York, NY, USA, 1986.
31. Shoji, M., "Analysis of high frequency thermal noise of enhancement mode MOS field-effect transistors," *IEEE Trans. Electron Devices*, Vol. 13, No. 6, 520–524, June. 1966.
32. Jindal, R. P., "Distributed substrate resistance noise in fine line NMOS fieldeffect transistors," *IEEE Trans. Electron Devices*, Vol. 32, No. 11, 2450–2453, Nov. 1985.
33. Nyquist, H., "Thermal agitation of electric charge in conductors," *Phys. Rev.*, Vol. 32, No. 1, 110–113, Jul. 1928.
34. Thornber, K. K., "Resistive-gate-induced thermal noise in IGFET's," *IEEE J. Solid-State Circuits*, Vol. 16, No. 4, 414–415, Aug. 1981.
35. Jindal, R. P., "Noise associated with distributed resistance of MOSFET gate structures in integrated circuits," *IEEE Trans. Electron Devices*, Vol. 31, No. 10, 1505–1509, Oct. 1984.
36. Razavi, B., R. H. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits Syst. I*, Vol. 41, 750–754, 1994.
37. Dambrine, G., H. Happy, F. Danneville, and A. Cappy, "A new method for on wafer noisemeasurement," *IEEE Transactions on Microwave Theory & Techniques*, Vol. 41, No. 3, 375–381, Mar. 1993.