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2 to 4 GHz Frequency Discriminator for RF Front-End Instantaneous Frequency Measurement Receivers

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Abstract—The instantaneous measurement of RF & microwave frequencies is widely used in electronic warfare (EW) for the determination of unknown signals over a broad frequency band. This paper presents an enhanced frequency measurement accuracy using three stages of novel RF frequency discriminator (FD) for RF front-end IFM Receivers. The appropriate structure of the designed frequency discriminator is implemented using a conventional PCB fabrication process. The frequency discriminator consists of two different hybrid layouts and one Wilkinson power divider, and all these components are implemented in microstrip technology, which is particularly important due to lower cost and easy integration into the PCB. To demonstrate the feasibility of the proposed structure, an RF-FE instantaneous frequency measurement (IFM) receiver has been realized based on 3-stage RF frequency discriminator. Simulation and measurement results have shown a frequency measurement accuracy less than 1 MHz (RMS) over the entire S-band.

1. INTRODUCTION

Instantaneous frequency measurement (IFM) receivers, using delay line discriminators, have demonstrated high performance characteristics for EW applications, such as multi-octave instantaneous bandwidth and probability of intercept approaching 100%. The essential component used in IFM receiver is the frequency discriminator FD, which provides fast real time measurement of instantaneous frequency, good sensitivity and high accuracy in frequency measurement. The FD consists of an input power divider, a delay line, a phase discriminator, diode detectors and low pass filters. Figure 1 shows a realization of such a discriminator. The input signal is split and fed into a phase discriminator via delayed and non-delayed two paths, and the delay line is indicated with a known constant time delay τ. The phase discriminator consists of three quadrature hybrid (90° coupler) and one power divider, and it combines the delayed and non-delayed input signals in special ways to convert the input RF signal to video signals via diode detectors and low pass filters. These video signals appear as the sine and cosine of the phase difference between the delayed and non-delayed paths. This phase difference θ is related to the input frequency by the following relation [1]:

$$\theta = \omega \cdot \tau \tag{1}$$

where $\omega = 2\pi f$ and τ is the time delay constant.

The output voltages are related to the phase difference by the following relations [1]:

$$V_A = 1 + \sin(\theta) \tag{2}$$

$$V_B = 1 - \sin(\theta) \tag{3}$$

$$V_C = 1 + \cos(\theta) \tag{4}$$

$$V_D = 1 - \cos(\theta) \tag{5}$$

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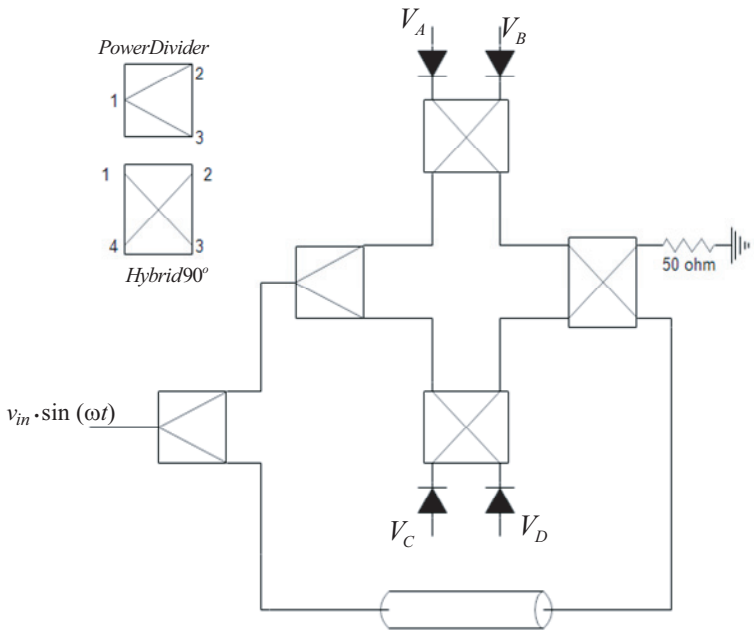


Figure 1. Frequency discriminator.

Then, the input frequency is determined by calculating the phase difference as follows [1]:

$$\theta = \tan^{-1}\left(\frac{V_A - V_B}{V_C - V_D}\right) \tag{6}$$

$$f = \frac{\theta}{2\pi \cdot \tau} \tag{7}$$

The accuracy of the measured frequency depends on the length of the delay line, so the desired frequency measurement accuracy could be achieved using multistage frequency discriminator with different delay time constants, allowing the measurement of the frequency value in practically real time within a broad frequency band, and providing high frequency measurement accuracy

This paper presents the design of a frequency discriminator (excluding the diode detectors and low pass filters) over the frequency band from 2 to 4 GHz, and the realization of an RF front-end IFM receiver consisting of three stages of the proposed FD. The architecture of the designed FD has the advantages of simplicity, low cost, and compact size. Output ports are placed on the same side of the circuit to ease the integration with the video processing circuit, which is not included in this work. The proposed design has been simulated and implemented using an Arlon25N substrate with a dielectric constant of 3.38, loss tangent of 0.0025 and thickness of 0.762 mm.

2. DESIGN OF FREQUENCY DISCRIMINATOR

The design of the FD shown in Figure 1 consists of the design of a quadrature hybrid (QH) coupler and power divider. Since the capability of the available conventional PCB fabrication process is taken into account, the input and isolated ports of the QH coupler have to be placed on the same side of the circuit. In addition, the design requires a 3-dB coupling factor for the QH coupler and a 3-dB power division ratio for the power divider over the entire S-band. Then, a Wilkinson power divider and two different coupler layouts are chosen for the design of the FD.

The multi-section branch-line coupler has wide operating bandwidth, but it consumes a large area on the substrate and cannot be fabricated by the available conventional PCB. On the other hand, using coupled microstrip lines, the tight coupling can be achieved using the Lange or tandem coupler, but they require wire crossover, and the tandem coupler may require wiggles or serpentines, which will cause difficulty at the fabrication stage.

To avoid these problems, a slot-coupled directional coupler between double-sided substrate microstrip lines (broadside coupler) can be realized to achieve a tight coupling and a very compact size over broad bandwidth.

In order to accomplish the design of the FD, there is a need to design a quadrature hybrid coupler with a single-layer substrate structure. An enhanced coupled line structure for tight couplers, which was proposed by Liang [5], will be used to validate the proposed architecture of the designed FD. It should be noted that the input and isolated ports for this coupler are placed on different sides of its structure, so it is inappropriate to use this coupler as the quadrature hybrid for the whole design of FD, because it will lead to crossover to deal with and complicate the architecture of the FD. Thus, two different structures have been designed: the broadside coupler and the enhanced coupled line quadrature hybrid.

2.1. Wilkinson Power Divider Design

A wideband equal-split Wilkinson power divider was designed according to [2] having a quarter wave transformer at its input. The topology of the designed divider was chosen to be elliptical in order to decrease the substrate area. Figure 2 shows the optimized circuit design with the following dimensions: $w_{50} = w_c = 1.76\,\text{mm}$, $w_q = 2.9\,\text{mm}$, $l_q = 16\,\text{mm}$, $D_1 = 11.56\,\text{mm}$, $D_2 = 7.14\,\text{mm}$, $l_{pad} = 0.9\,\text{mm}$.

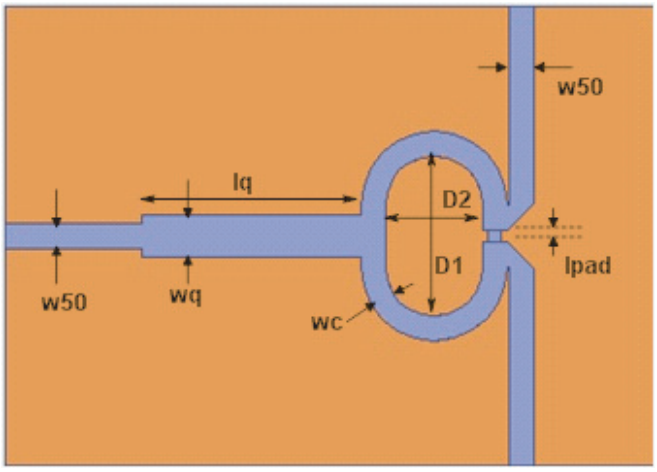


Figure 2. A 3-dB power divider.

The frequency response of the simulated power divider is shown in Figure 3, resulting in a $3\,\text{dB} \pm 0.3\,\text{dB}$ coupling between input port 1 and output ports 2 and 3, and in a return loss better than 14 dB at all ports. The isolation between output ports 2 and 3 is also better than 15 dB over the entire S-band. A good balance in amplitude and phase is obtained as shown in Figure 4, where the amplitude difference between the output ports is less than 0.05 dB, and their phase variation is $0^\circ \pm 0.05^\circ$ over the entire S-band.

2.2. Broadside Coupler Design

The configuration of the proposed broadside coupler is a slot-coupled directional coupler between double-sided substrate microstrip lines as shown in Figure 5. The coupler consists of three conductor layers with two substrates interleaved between each of the layers. The top conductor layer includes port 1 and 2; meanwhile bottom conductor layer includes port 3 and 4. Both of this top and bottom layers are coupled through the slot in the duplicated common ground plane. The widths of microstrip w_p and slot w_s of the coupler can be calculated using the even- and odd-mode analysis approach presented in [3] to have a 3 dB coupling coupler.

Having obtained the initial dimensions of the coupler, the final dimensions determined by optimization are as follows: $w_p = 6.1\,\text{mm}$, $w_s = 9.2\,\text{mm}$, $l_p = 15.3\,\text{mm}$.

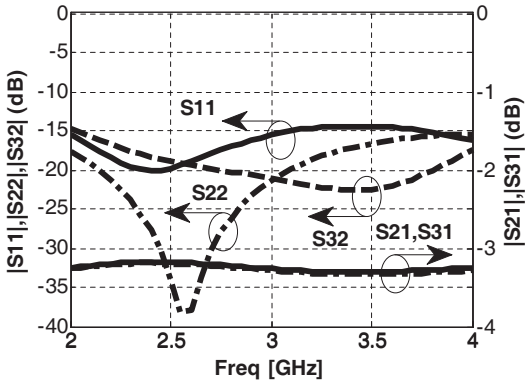


Figure 3. Simulated S-Parameter performance of the designed power divider.

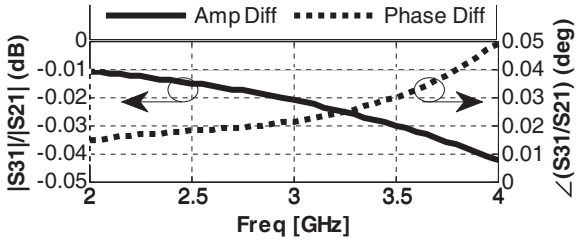


Figure 4. Amplitude difference and phase variation between the output ports of the designed power divider.

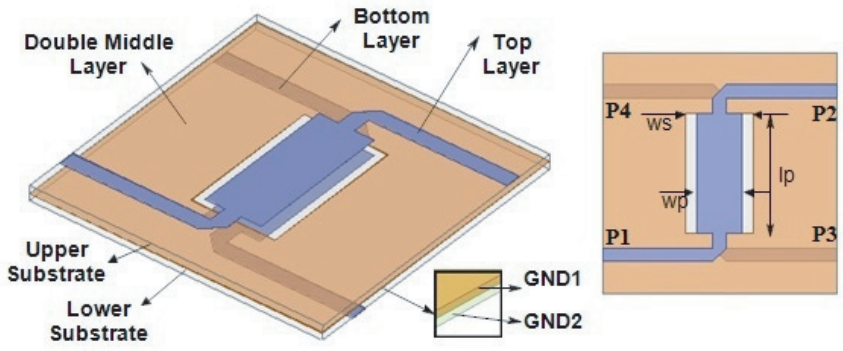


Figure 5. Broadside coupler layout.

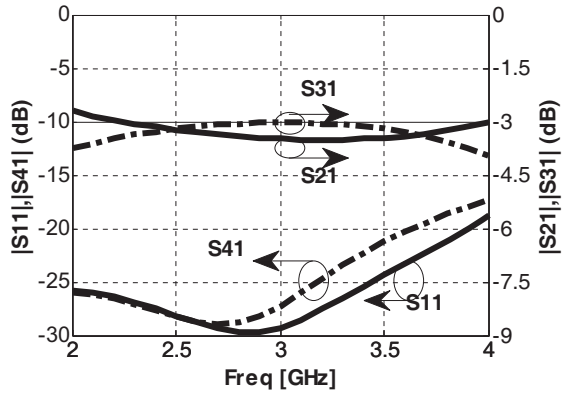


Figure 6. Simulated S-parameter performance of the designed broadside coupler.

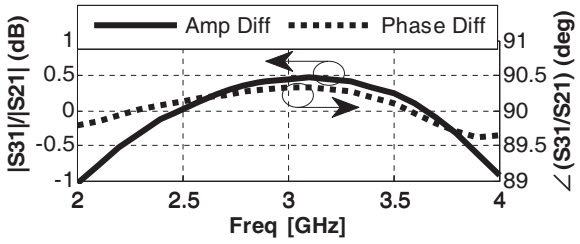


Figure 7. Amplitude difference and phase variation between the output ports of the designed broadside coupler.

The simulated S-parameters for the designed coupler are shown in Figure 6. The simulation results show that both return loss and isolation are better than 16 dB between 2 GHz and 4 GHz, and the coupling provided by this coupler is in the range of 3 dB $\pm$ 1 dB. Figure 7 indicates that the amplitude difference between the through and coupled ports (i.e., port 2 and port 3) is less than 1 dB, and the phase variation is $90° \pm 0.4°$ over the entire S-band.

2.3. Three-Section Coupled Line Quadrature Hybrid Design

The second needed QH for the FD is chosen to be a three-section quadrature hybrid having 3 dB coupling and 90° phase over the S-band. First, the dimensions of each coupling section are designed based on the even- and odd-mode impedances. Following the multi-section TEM coupler theory [4], the two outer sections (1 and 3) have $Z_e = 63.52\,\Omega$ and $Z_o = 39.36\,\Omega$ and are implemented by the conventional coupled microstrip lines. The central Section (2) has $Z_e = 183.28\,\Omega$, $Z_o = 13.64\,\Omega$ and has been realized by following the guidelines in [5] to have a tight coupler of type $\prod$ with structure shown in Figure 8.

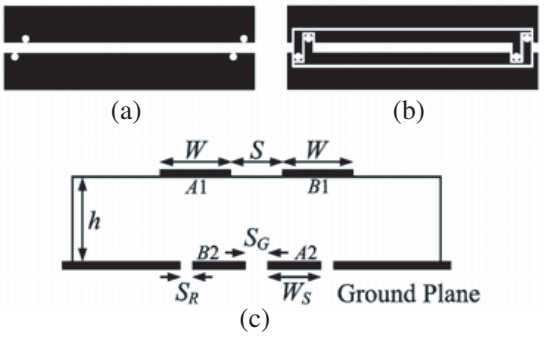


Figure 8. Coupled microstrip lines of type $\prod$. (a) Top view. (b) Bottom view. (c) Cross-section view (copied from [5]).

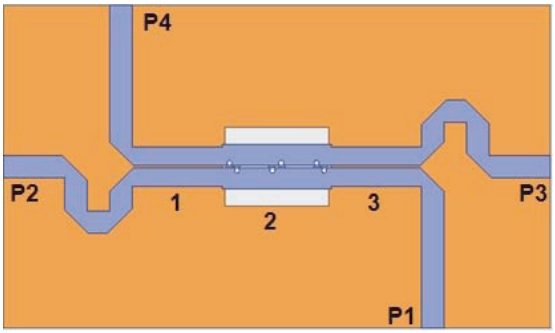


Figure 9. Top view of the three section quadrature hybrid.

The structure of the three-section coupler was edited by centralizing the ports P2 and P3 at the middle between ports P1 and P4 as shown in Figure 9, in order to validate the symmetry of the phase discriminator structure. The initial physical dimensions were optimized to compensate the discontinuities between coupling sections. The final dimensions of the quadrature hybrid are listed in Table 1, and the diameter of each hole in the structure is 0.4 mm.

Table 1. Dimensions (mm) of three-section quadrature hybrid.

Section	w	w_s	s	s_g	s_r	l
1 and 3	1.5	-	0.15	-	-	7
2	1.7	0.95	0.15	0.15	2.075	8.5

Figure 10 shows the simulated response of the designed coupler, in which the return loss at the input port P1 is better than 21 dB, the isolation $|S_{41}|$ better than 20 dB and the resulting coupling factor about 3 dB over the entire S-band. Figure 11 indicates that the amplitude difference is less than 1 dB, and the phase variation is $90° \pm 0.2°$ all over the entire S-band.

2.4. Frequency Discriminator Design

After designing different needed components, the frequency discriminator circuit was realized as shown in Figure 12. The cluster (Wil C1 C2 C3) is the phase discriminator, which is made frequency sensitive by replacing the input power divider by a broadside quadrature hybrid C4 and the delay line is connected between ports P2 and P3. Taking in consideration that there is a 90° shift between ports P1 and P2 of C4, the placement of C4 was optimized, and the feed lines to C1 and C2 are equal in length to ensure the tracking of the delay line phase at the output ports A to D. In the presence of the bottom substrate under the coupler C3, a slot is needed in the bottom middle layer ground and then the coupler dimensions must be optimized to ensure amplitude and phase balancing. Figure 13 displays the photograph of the fabricated frequency discriminator. The overall size of the circuit is 10 cm × 9 cm.

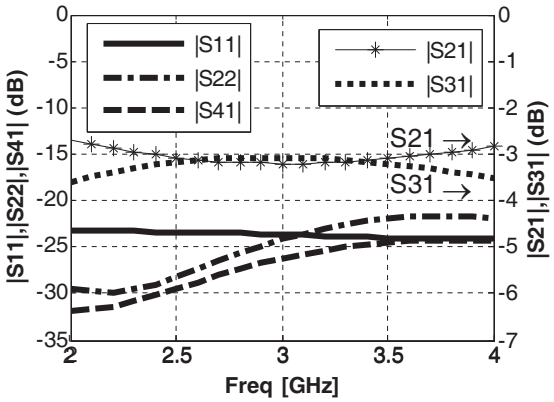


Figure 10. Simulated S-parameter performance of the designed three-section quadrature hybrid.

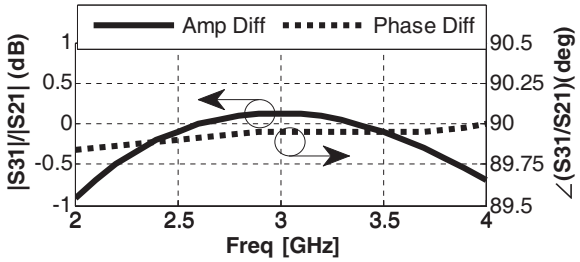


Figure 11. Amplitude difference and phase variation between the output ports of the designed three-section quadrature hybrid.

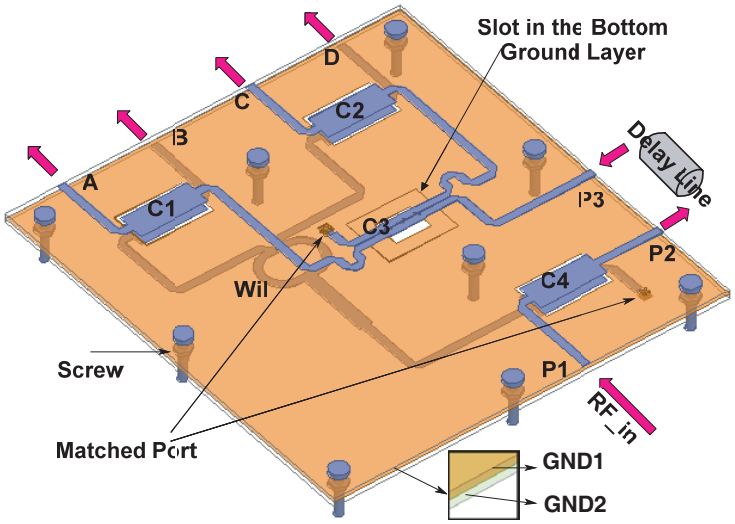


Figure 12. Top view of the designed frequency discriminator.

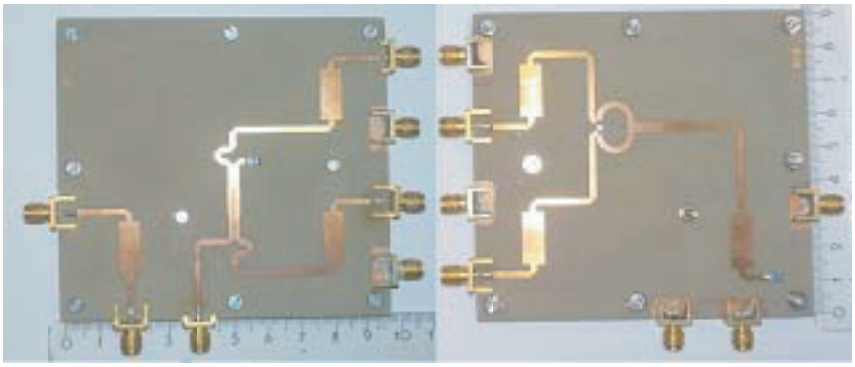
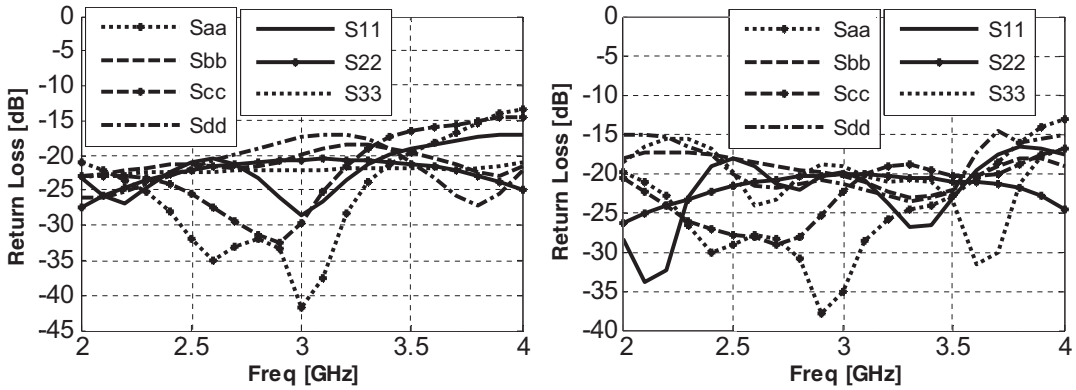


Figure 13. Top and bottom photographs of the fabricated frequency discriminator.



(a) Simulated Results (b) Measured Results

Figure 14. (a) Simulated and (b) measured RL of the FD.

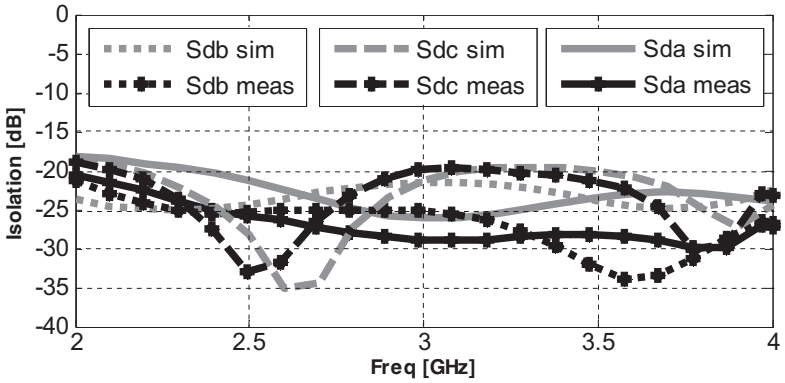


Figure 15. Simulated and measured isolation between output ports of the FD.

Figure 14 shows the simulated and measured return losses at ports P1, P2, P3, A, B, C and D, which are better than 14 dB. The simulated and measured isolations between output ports are shown in Figure 15, and they are better than 17 dB.

The simulated and measured insertion losses from P1 to P2 are 3 dB $\pm$ 0.8 dB all over the entire S-band, as shown in Figure 16(a). Theoretically, by assuming ideal components, the insertion loss from P1 to output ports is 9 dB and from P3 to output ports is 6 dB. The simulated and measured insertion losses are shown in Figures 16(b) and (c) respectively. These figures show that there is a 9 dB insertion loss when the FD is driven from P1 and 6 dB when the FD is driven from P3 with an amplitude difference between paired output ports (i.e., [A, B] and [C, D]).

Figure 17(a) shows that the simulated amplitude difference between paired output ports is in the range of $\pm$1 dB, and Figure 17(b) shows that the measured amplitude difference is in the range of $\pm$2 dB and specifically $\pm$1 dB for 90% of the observed bandwidth. Furthermore, the simulated phase variation between these paired ports is $90^\circ \pm 2^\circ$ as shown in Figure 18(a), and the measured phase variation is $90^\circ \pm 3^\circ$ as shown in Figure 18(b).

3. THREE-STAGE IFM RECEIVER

In order to achieve a frequency measurement accuracy less than 1 MHz (RMS) from 2 to 4 GHz, a multi-stage IFM receiver was established depending on the previous fabricated FD and using different delay time constant for each stage. The shortest delay line (smallest time constant) determines the operating bandwidth, while the longest delay line (largest time constant) determines the frequency measurement accuracy.

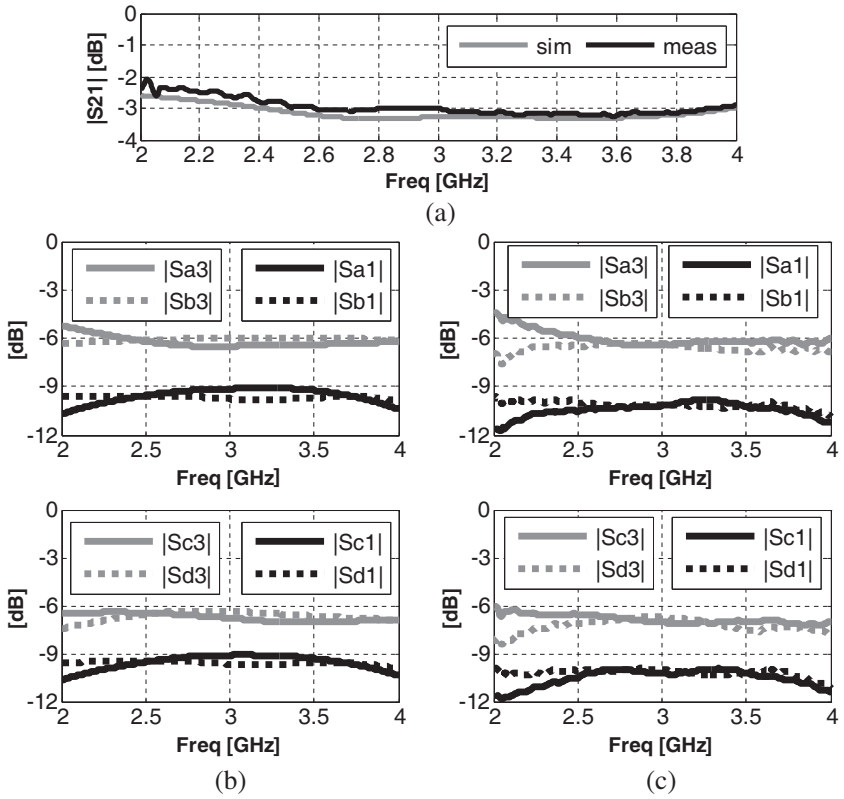


Figure 16. Simulated and measured response of the FD when it is driven from port 1 and 3. (a) S_{21}. (b) Simulation Results. (c) Measured Results.

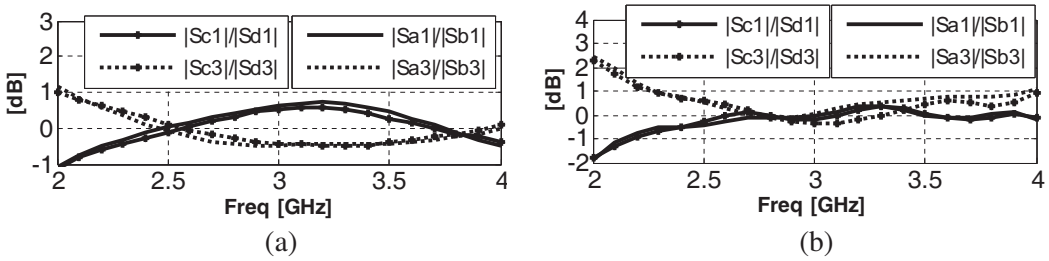


Figure 17. Simulated and measured amplitude difference between output ports when the FD is driven from port 1 and 3. (a) Simulation results. (b) Measured results.

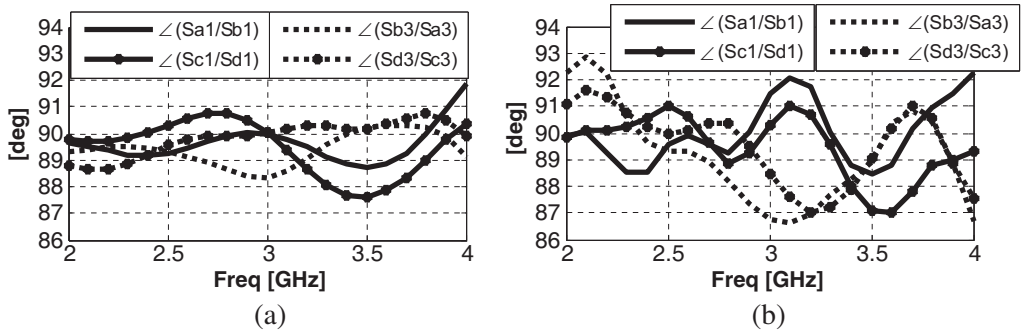


Figure 18. Phase variations between output ports when the FD is driven from port 1 and 3. (a) Simulated, (b) measured results.

In the absence of the video detection stage, the output video signals could be determined as follows:

$$V_A = |S_{A1}|^2 \tag{8}$$

$$V_B = |S_{B1}|^2 \tag{9}$$

$$V_C = |S_{C1}|^2 \tag{10}$$

$$V_D = |S_{D1}|^2 \tag{11}$$

The measurement procedure of these output video signals was done in two steps. In the first step, the vector network analyzer was used to measure and store the transmission parameters S_{A1}, S_{B1}, S_{C1} and S_{D1}. In the second step, using Matlab® and measured S parameters, the output video signals are calculated according to Equations (8) to (11), and then Equation (6) was used to calculate the phase θ.

3.1. First Stage

A delay line with time constant $\tau = 0.5$ ns was connected to the first FD in order to cover the bandwidth of 2 GHz. The measured phase θ and the frequency measurement error are shown in Figure 19 and Figure 20 respectively. The frequency measurement accuracy for this stage was about 16 MHz (RMS), so second stage with longer delay line was added to enhance the frequency measurement accuracy.

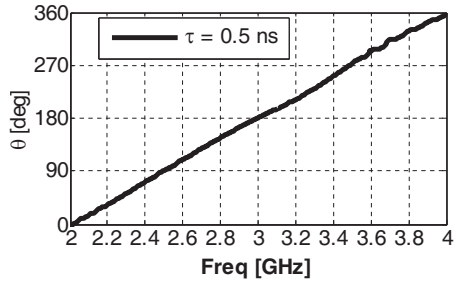


Figure 19. Measured phase θ of the first stage FD.

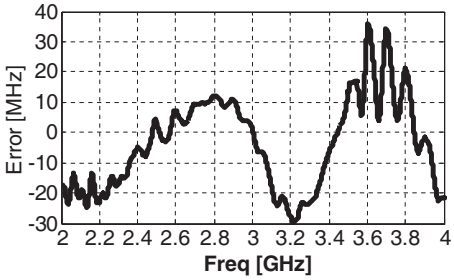


Figure 20. Frequency measurement error for one stage FD.

3.2. Second Stage

In the second stage, a delay line with time constant $\tau = 2.713$ ns was used, which corresponds to 368 MHz operating bandwidth. The measured phase θ of this stage and that of the first stage are shown in Figure 21. The ambiguity in measuring the frequency for this stage could be solved by the measured frequency in the first stage. The frequency measurement error is shown in Figure 22, where the ambiguity was resolved and the frequency measurement accuracy for this stage was about 2.3 MHz (RMS). In comparison with the first stage, the frequency measurement accuracy is improved, but still insufficient and a third stage is needed.

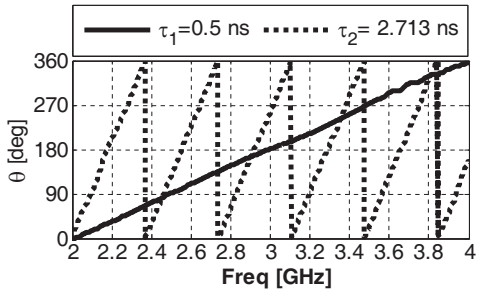


Figure 21. Measured phase θ of the first and second stages.

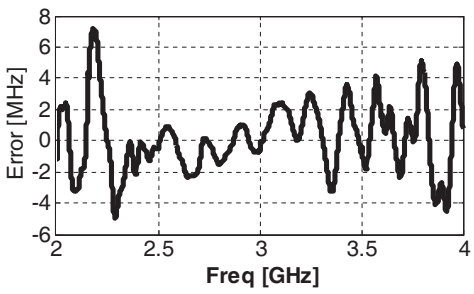


Figure 22. The frequency measurement error for two stages of FD.

3.3. Third Stage

In order to enhance the frequency measurement accuracy, a third stage of FD was used, with a delay line of time constant $\tau = 13.8$ ns, which corresponds to 72.5 MHz operating bandwidth.

Figure 23 shows the measured phase θ of the second and third stages. The ambiguity in frequency measurement could be solved by the measured frequency in the previous stages, and the frequency measurement error is shown in Figure 24. The frequency measurement accuracy, when three stages of FD were used, was about 0.8 MHz (RMS), so the desired accuracy was achieved by using three stages of FDs.

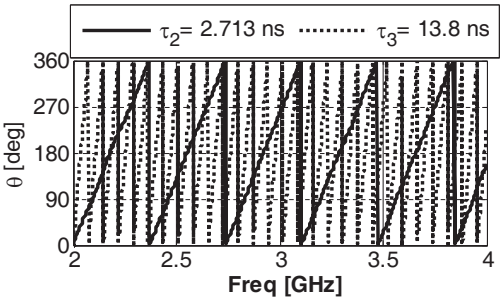


Figure 23. Measured phase θ of the second and third stages.

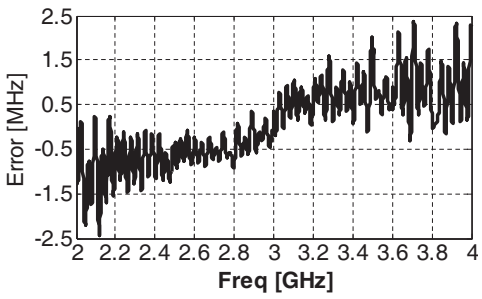


Figure 24. The frequency measurement error for three stages of FD.

4. CONCLUSION

An RF-FE IFM receiver is realized with frequency measurement accuracy less than 1 MHz (RMS). This accuracy is achieved by designing a receiver architecture consisting of three stages of RF frequency discriminator. The frequency discriminator is designed using simple microstrip components: a Wilkinson power divider, a broadside hybrid, and a three-section coupled-line hybrid. This designed RF frequency discriminator is implemented using conventional PCB fabrication process. The implemented frequency discriminator has a simple configuration and is easily fabricated on a multilayer substrate. It is compact, has low cost, and exhibits high performance over the frequency band of 2 GHz to 4 GHz.

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