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Design of Broadband, High-Efficiency, and High-Linearity GaN HEMT Class-J RF Power Amplifier

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Abstract—In this paper, the design of a broadband, high-efficiency, and high-linearity Class-J GaN HEMT RF power amplifier (PA) over 1.6–2.6 GHz is explained. The source impedance is conjugate-matched to the input impedance of the device resulted from small signal simulation to make a high-gain power amplifier. The load impedance related to the maximum power added efficiency (PAE) and maximum output power is obtained by pulling the only fundamental and second harmonic components over frequency bandwidth. Thus, not only a high-efficiency PA but also a high-linearity PA is formed. The input and output matching networks are implemented by microstrip transmission lines. The theoretical PA designed is optimized using computer-aided simulations. The fabricated PA provides output power in the range of 38–39.9 dBm with 60%–73% PAE and 15–16.3 dB power gain across the band. The worst measured ACLR1 as the PA is fed by the CDMA signal with 1.2288 MHz bandwidth is at a level of −38.6 dBc. A close agreement between the measured and simulation results is observed due to the use of high-order harmonic balance simulator and high-accuracy implementation procedure.

1. INTRODUCTION

Power amplifiers (PAs) are usually characterized by three main features; bandwidth, power efficiency, and linearity performance, which are often in conflict with one another and hence the need for optimal design tradeoffs by RF engineers. Such tradeoffs are better illustrated by comparing two major PA classes, linear and nonlinear classes. In linear classes, only fundamental harmonic component of drain voltage is considered while nonlinear classes investigate even higher harmonic components of drain voltage as well as drain current.

Several PA classes for applications with different requirements have emerged. Class-A PA topology demonstrates the best linearity performance, but it provides the lowest efficiency of 50% [1]. Class-B PA using an infinite number of high-order harmonics of current shows much better efficiency (78.5%) but lower linearity [2]. For a better compromise, Class-AB PA has been proposed with better linearity than Class-B and better efficiency than Class-A [3]. Higher efficiency, greater than 78.5% and theoretically close to 100%, is addressed using high nonlinear (switching) PA classes such as Class-E [4] and Class-F/F^{-1} [5]. These topologies rely on tuning at least third-order harmonic of the drain voltage and current signals. In these classes, using the further order of harmonics makes for higher efficiency but lower linearity.

Nowadays, Class-J PA [6] has received wide attention in numerous applications (e.g., new generation communication systems such as WiMAX and LTE/LTE-A), requiring both high efficiency and high linearity performance due to its good compromise between the two performance metrics. This class theoretically yields high efficiency, similar to Class-B (78.5%), but unlike Class-B, it is potentially more

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linear due to its tuning of only the second harmonic [7]. Therefore, the linearity is not much sacrificed for efficiency. It is also potentially able to demonstrate wide bandwidth since unlike other switching PAs, neither resonator circuits nor large input drive is required in its structure [8–10]. Another advantage of Class-J PA is that the drain-source capacitance is not accounted as a parasitic element but employed in the matching network as a beneficial element [11].

Figure 1 shows the generic circuit schematic of a Class-J PA based on a simplified model of a bare chip GaN HEMT including the input matching network (IMN) and output matching network (OMN). Typically, the transistor gain is sharply decreased as the frequency increases. This effect is known as the transistor gain roll-off and must be properly compensated for a broadband PA to achieve a flatter gain. For simplicity, it is better to first compensate the gain roll-off by a gain equalizer sub-network, as shown in Fig. 1, and then IMN and OMN are designed. Naturally, the gain roll-off is originated from the device parasitic capacitances. To compensate such a capacitive effect and gain roll-off, a simple inductance (or a transmission line) in series with the input device as a pre-matching network is usually used [12].

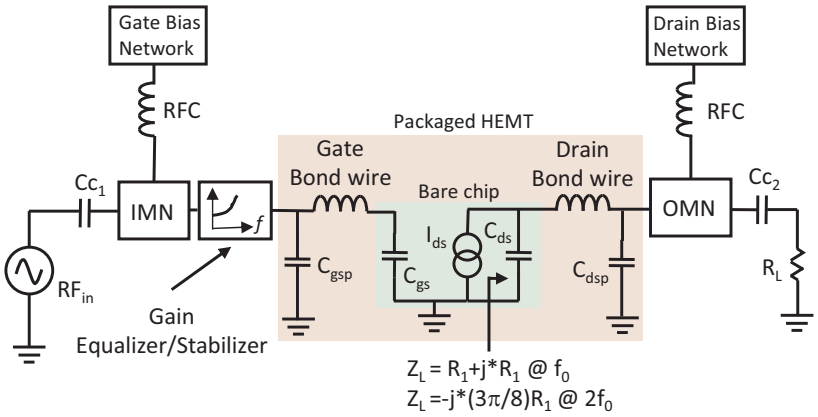

Figure 1. Generalized circuit schematic of a Class-J PA.

In this research, a broadband Class-J RF PA based on a 6-W Wolfspeed's CGH40006P GaN HEMT is designed to achieve high-efficiency and high-linearity performances over 1.6–2.6 GHz. The transistor gain variation is first balanced by a gain equalizer sub-network in series with the device input. Then, the source impedance is considered as the conjugate input impedance of the device seen from the generator toward the used equalizer, while the load impedance is obtained from pulling the fundamental and second harmonic impedances of the load. The input and output matching networks are designed and implemented by the microstrip transmission lines in such a way that a broadband Class-J PA is achieved. The PA in a slightly overdriven input power provides at least 6-W output power with a 16-dB minimum signal gain and almost 60% minimum power added efficiency across the entire bandwidth

This paper is organized as follows. In Section 2, the design theory of Class-J PA is briefly explained, while Section 3 presents the simulation methodology which shows how the appropriate gain equalizer circuit, load impedance, and source impedance are obtained and consequently, how the input and output matching networks are designed. Section 4 provides the simulation and measurement results of the fabricated PA, and finally the paper is concluded and compared with the other state-of-art designs in Section 4.

2. DESIGN THEORY

Class-B PA is realized when a half-sinusoidal waveform for the drain current and a full sinusoidal waveform for the drain voltage are formed by the device load network. For this reason, the gate is biased at the transistor pinch-off point. The input power level must not be large so that the drain voltage waveform is not clipped. The Fourier's series expansions of the drain current and voltage

signals become

$$i_{\mathrm{d,B}}(\omega t) = I_{\max}\left(\frac{1}{\pi} - \frac{1}{2}\sin(\omega t) - \frac{2}{\pi}\sum_{n=2,4,6,\ldots}^{\infty}\frac{\cos(n\omega t)}{n^2-1}\right) \tag{1}$$

$$v_{\mathrm{d,B}}(\omega t) = (V_{dd} - V_k)(1 + \beta\sin(\omega t)) \tag{2}$$

where $I_{\max}$, V_{dd}, V_k denote the maximum drain current, drain dc bias voltage, and device knee voltage, respectively. β is a constant coefficient related to input power level and limited in the range of $[0, 1]$. The fundamental output power and efficiency are simply obtained from Eqs. (1) and (2) as $P_{out,B} = \beta(V_{dd} - V_k)I_{\max}/4$ and $\eta_B = \beta(\pi/4)\%$, respectively. Thus, the maximum efficiency and optimum load impedance for the $\beta = 1$ (maximum input power level before signal clipping) are 78.5% and $R_{opt,B} = 2(V_{dd} - V_k)/I_{\max}$, respectively.

Class-J PA, which was first introduced by Crips [6], takes only two early harmonics of the Class-B drain current shown in Eq. (1) while the drain voltage is shifted as long as 45° as a result of a proper load network. Therefore, it potentially shows better linearity than Class-B. The drain current and voltage become

$$i_{\mathrm{d,J}}(\omega t) = I_{\max}\left(\frac{1}{\pi} - \frac{1}{2}\sin(\omega t) - \frac{2}{3\pi}\cos(2\omega t)\right) \tag{3}$$

$$v_{\mathrm{d,J}}(\omega t) = (V_{\mathrm{dd}} - V_{\mathrm{k}})(1 + \beta\sin(\omega t))\underbrace{(1 - \alpha\cos(\omega t))}_{\substack{\text{corresponding}\\ \text{term to shift}\\ \text{the voltage}\\ \text{waveform}}} \tag{4}$$

where α is the constant coefficient of Class-J operation bounded in $[-1, 1]$. The maximum output power and maximum efficiency are realized for $\beta = 1$. The fundamental output power and efficiency are simply obtained from Eqs. (3) and (4). The voltage and current waveforms for the Class-B and the groups of Class-J (the different values of α at $\beta = 1$) are shown in Fig. 2. In order to satisfy Eqs. (3) and (4), the load impedances at the fundamental and second harmonic must be as follows

$$Z_{\mathrm{f_0,J}} = \left.\frac{\bar{V}_{\mathrm{d}}}{\bar{I}_{\mathrm{L}}}\right|_{@f0} = \left.\frac{\bar{V}_{\mathrm{d}}}{-\bar{I}_{\mathrm{d}}}\right|_{@f0} = \frac{2(Vdd - Vk)}{I_{\max}}(\beta + j\alpha) = \beta R_{opt,B} + j\alpha R_{opt,B} \tag{5}$$

$$Z_{\mathrm{2f_0,J}} = \left.\frac{\bar{V}_{\mathrm{d}}}{\bar{I}_{\mathrm{L}}}\right|_{@2f0} = \left.\frac{\bar{V}_{\mathrm{d}}}{-\bar{I}_{\mathrm{d}}}\right|_{@2f0} = -j\frac{3\pi}{8}\frac{2(V_{dd} - V_k)}{I_{\max}}\alpha\beta = -j\frac{3\pi}{8}\alpha\beta R_{opt,B} \tag{6}$$

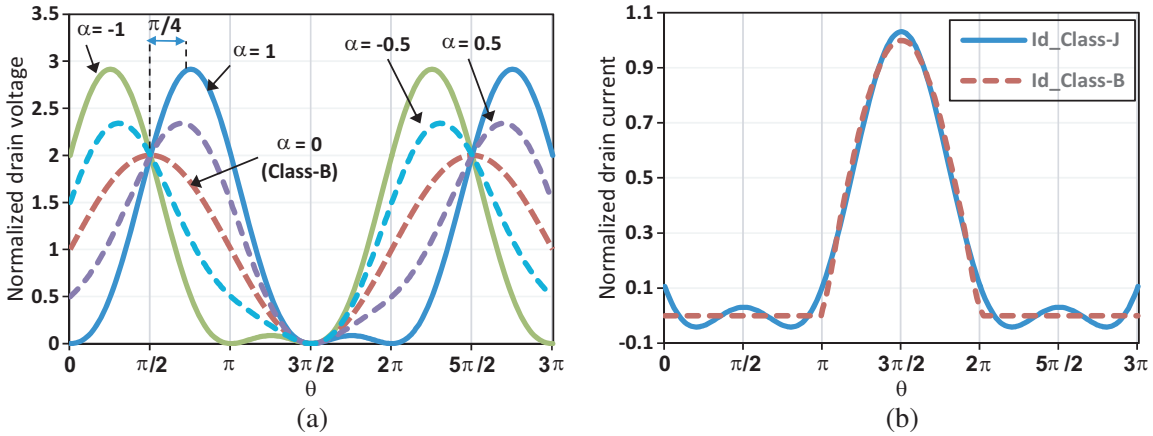

Figure 2. Normalized waveforms for Class-J PA with different values of α at $\beta = 1$ in comparison with Class-B PA waveforms, (a) normalized drain voltage waveforms and (b) normalized drain current waveforms.

The load impedance values for Class-J operation demonstrate that the drain device must see an inductive or capacitive load (depending on α) as much as $\beta R_{opt,B} + j\alpha R_{opt,B}$ at the fundamental frequency and a capacitive load as much as $\alpha\beta R_{opt,B}(3\alpha/8)$ at the second harmonic. There is a inherently capacitive load between the drain and source junctions which simplifies the design of the PA load network. The note which must be taken into account in this class is that the maximum voltage across the device drain-source can attain nearly three times of dc bias voltage, and therefore to avoid breakdown, the dc drain voltage must be under one-third of the transistor breakdown voltage.

3. SIMULATION METHODOLOGY

In this study, a general purpose CGH40006P GaN HEMT from Wolfspeed Company is employed as an active device to design a Class-J RF PA over 1.6–2.6 GHz. The bare chip used in this packaged transistor is CGH60008D GaN HEMT device which is used to de-embedding the device parasitic elements. For Class-J operation, as mentioned in the previous section, the optimum gate bias is the transistor pinch-off voltage (V_p) which is -2.9 V for the selected transistor. For reliable operation, it is compulsory to avoid breakdown region. According to the transistor datasheet, the breakdown occurs around 84 V, and therefore, the drain is biased at 27 V which is slightly less than its recommended bias point in the datasheet. The bias sequencer-controller MABC-001000-DP000L from Macom Company is employed to control the dc bias and protect the transistor from low-frequency instability.

Small signal simulation indicates the stability factor below one ($K < 1$), and therefore instability may occur. There are several approaches to improve stability level [13] such as using a resistor in series or parallel with the input or output of the device as recommended in the device's datasheet. A very high stability factor is also unacceptable because increasing stability factor leads to lower signal gain. On the other hand, gain variation is a common problem in broadband amplifiers due to the gain roll-off. Low gain variation is an important requirement in the modern signal modulations such as OFDM and LTE. Here, a 2.5 Ω resistor in series with a 0.3 nH inductor, as shown in Fig. 3, acts as a stabilizer and gain equalizer for compensating the gain roll-off effect. The simulation results for stability factor (k factor) and maximum available gain with and without the presence of stabilizer/equalizer circuit are shown in Fig. 4. Since, the k factor is less than one for the bottom half of the bandwidth, magnitudes of $S(1,1)$ and $S(2,2)$ are simulated to ensure that they are also less than one, and therefore, the PA works in a stable condition [14]. The resulting $S(1,1)$ and $S(2,2)$ are shown in Fig. 5, which entirely satisfy the stability criteria. This circuit not only improves stability level but also reduces the gain variation and facilitates the design of input matching network by increasing the source impedance value of PA.

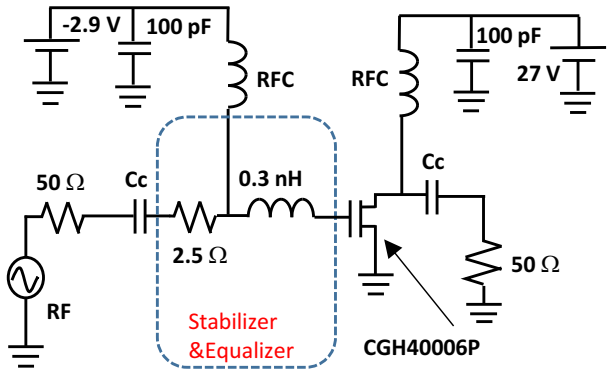

Figure 3. Configuration of stabilizer/equalizer circuit in PA structure.

The conjugated input impedance seen from the generator toward the device will be an optimum source impedance, since Class-J PA, similar to Class-B, avoids clipping signal and nonlinear region. It is hard to design a broadband matching network when the load impedance contains a large imaginary part implying a very highly loaded Q (Q_L) circuit. The PA input impedance in the presence of the stabilizer over 1.6–2.6 GHz is shown in Fig. 6(a). Fortunately, as can be seen from this figure and also as expected

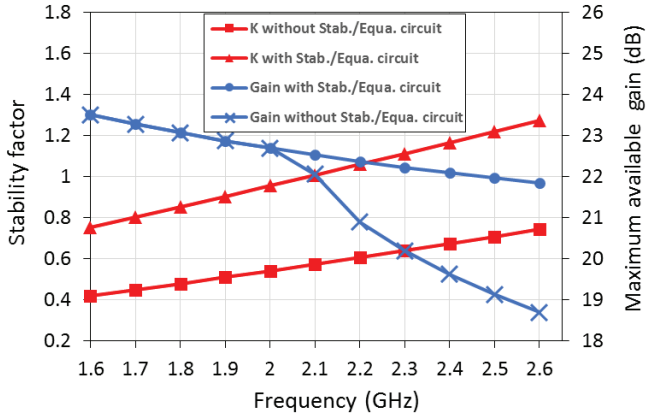

Figure 4. Small-signal simulation results for stability factor and maximum available gain versus frequency within and without presence of stabilizer/equalizer circuit.

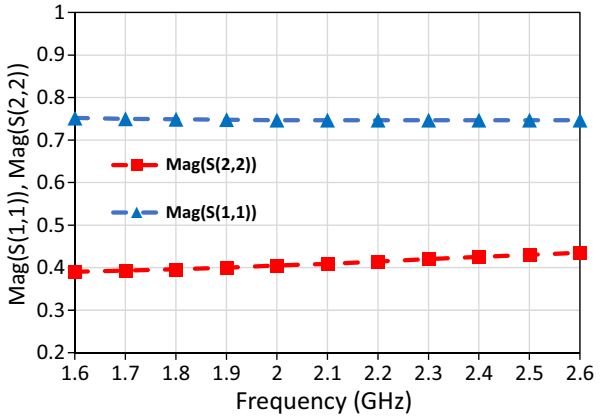

Figure 5. Magnitude of $S(1,1)$ and $S(2,2)$ versus frequency of PA in presence of stabilizer/equalizer circuit, ensuring stability criteria.

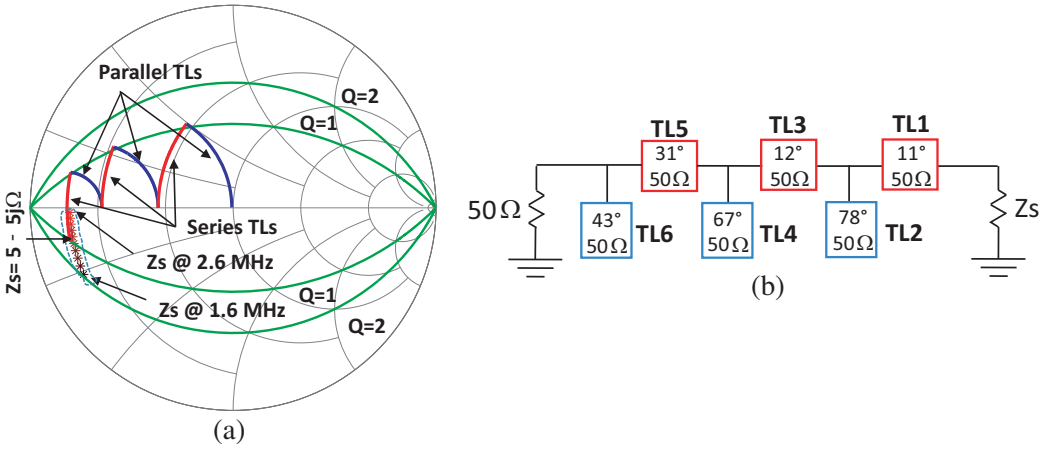

Figure 6. Conjugated input impedances swept over 1.6–2.6 GHz in steps of 100 MHz with showing input matching network loci at the center frequency and Q curves, (b) configuration of input matching network by 50 Ω microstrip lines.

from the operation of the used stabilizer, the imaginary parts of the input impedances are small enough and bounded within the $Q = 2$ curve with up to half of the impedances bounded within the $Q = 1$ curve. Although increasing inductance value will lead to all impedances bounded within the $Q = 1$ curve, it will also lead to lower bandwidth due to large Q_L provided by the inductance. In order to get a facility in the design of the broadband input matching network, a $5 - j5\,\Omega$ ($Q_L = 1$) is adopted for the source impedance. However, selecting this impedance might lead to a slight reduction in power gain at the whole frequency except 2 GHz. The ladder structure of series and parallel 50 Ω transmission lines (TLs) operates as a broadband low-pass filter so that when the TLs values are appropriately determined, an optimum low-loss broadband matching network is realized. This filter is graphically designed based on the method proposed in [15]. The low-pass filter structure for the input ($n = 6$) matching network using 50 Ω transmission lines is depicted in Fig. 6(b).

The optimum Class-J load impedance related to the maximum power added efficiency (PAE) and output power is obtained using pulling the load in such a way that the load impedance is maintained as the shape of $R_1 + j\alpha R_1$ at the fundamental frequency, $-j\alpha R_1(3\pi/8)$ at the second harmonic component, and opened circuit for all higher harmonics. The 7th order harmonic balance simulator provided in

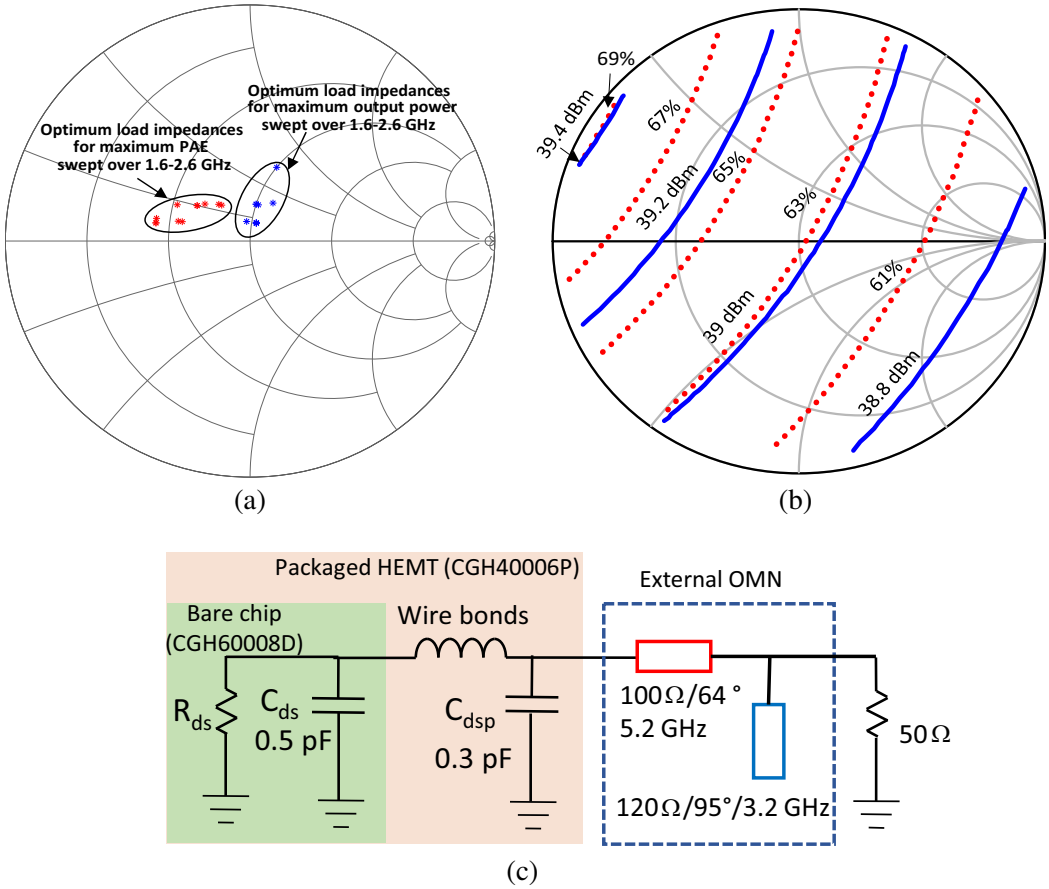

Figure 7. Optimum output fundamental load impedances for the maximum PAE and maximum output power swept over 1.6–2.6 GHz in steps of 100 MHz, (b) the second harmonic load pulling contours for the PAE (dashed lines) and the output power (solid lines) as the fundamental harmonic component of load impedance is kept fix at 2.1 GHz, (c) configuration of output matching network.

Keysight's Advanced Design System (ADS) software is used. The load-pull impedances obtained from simulation for the PAE and output power in steps of 100-MHz at the fundamental and second harmonics are shown in Figs. 7(a) and (b). Fortunately, the optimum impedances are near the center of Smith chart (50 Ω) which facilitates the design of output matching network. A simple low-pass filter structure of microstrip transmission lines proposed here, as shown in Fig. 7(c), appropriately matches the device by the network (50 Ω) at the fundamental harmonic and matches by a low-real value impedance at the second harmonic which is a Class-J requirement. Although the matching network seems as though it is unable to provide definite Class-J load condition, especially for the second harmonics of the early frequencies, it is optimized for output power and PAE parameters by computer-aided simulation as the power amplifier design is completed.

The prototype PA structure is shown in Fig. 8. The designed PA circuit is optimized by ADS for the PAE greater than 60% and the output power greater than 38 dBm (6.3 W) by varying the width and length of all transmission lines. Finally, the electromagnetic (EM) simulation is carried out to predict PA behavior in the real condition.

4. SIMULATION AND EXPERIMENTAL RESULTS

The power amplifier is biased at $V_{dd} = 27$ V, $V_{gs} = -2.9$ V and is fed by 23-dBm input power level over 1.6–2.6 GHz. The load-line simulation results in steps of 100-MHz at the intrinsic drain of the bare chip are shown in Fig. 9. It is demonstrated that the maximum voltage attains close to 75 V where the

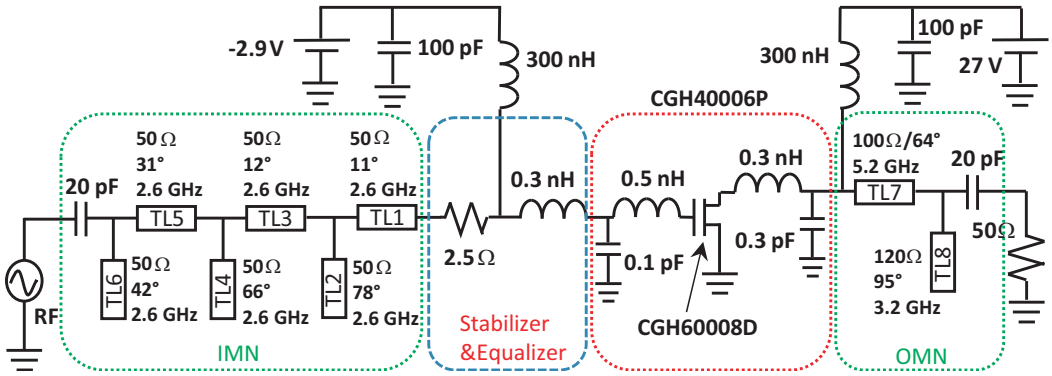

Figure 8. Prototype schematic of Class-J PA.

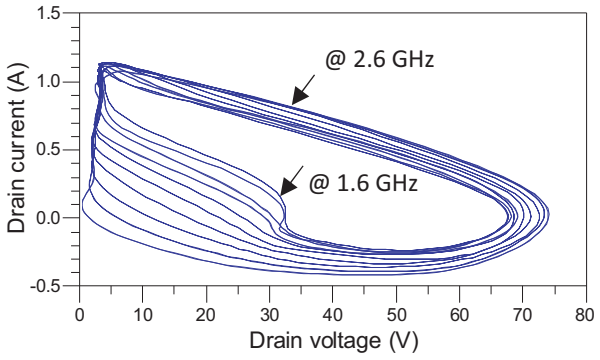

Figure 9. Load line of Class-J PA at the intrinsic drain of the bare chip.

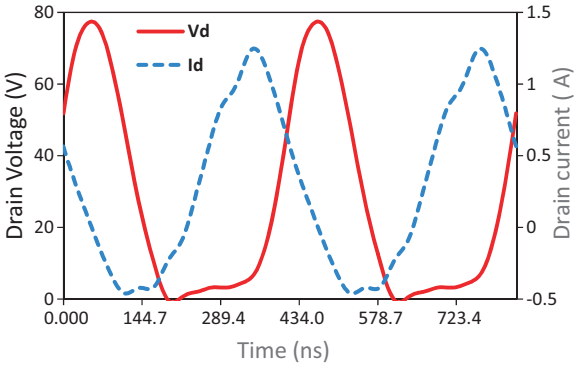

Figure 10. Time-domain simulation results for drain voltage and current waveforms of prototype Class-J PA at 2.4 GHz.

current lines are appropriately maintained low, around zero. The maximum current rises to near 1.3 A at 2.6 GHz, where the drain voltage is sufficiently small. It also shows that the PA for high-efficiency operation has not been saturated such as Class-F and Class-E PAs and therefore, a proper linearity performance will be expectable. The time-domain simulation results for the drain voltage and current waveforms of the prototype PA at 2.4 GHz are shown in Fig. 10.

The substrate used for fabrication has a 3-mm dielectric thickness, 17-µm copper cladding thickness, and $\epsilon_r = 4.2$. We used a thick substrate because the lead of packaged transistor CGH40006P is rather wide while the matching network requires small inductance (0.3 nH). The fabricated Class-J PA is shown in Fig. 11. The TL4 is drawn in opposite side with TL2 and TL6 to reduce the coupling effect between the stubs. TL4 and TL8 are also used for the gate and drain DC supply path, respectively. Two 300-nH inductors as RFCs isolate DC signals from RF signals. In order to block DC signals from the input and output ports, two low-ESR capacitors (20-pF) are employed. The PCB dimensions are 42 mm × 45 mm. The PCB was screwed on a suitable aluminum heat sink.

An Agilent's RF signal generator N9310A is used to sweep input signal over 1.6–2.6 GHz in steps of 50-MHz for characterizing the PA. The generated signal is boosted by a commercial pre-driver to provide sufficient input power level, since the single RF generator may not produce sufficient level. The PA output is connected to Agilent's spectrum analyzer E4440A equipped by a high-power attenuator in order to protect the instrument. The simulation and measurement results for the output power, power gain, and PAE as functions of frequency at $P_{in} = 23$ dBm are shown in Fig. 12. The PAE is greater than 60% throughout the band. It nearly attains 73% at 2.5 GHz while it drops to 60% at 1.6 GHz. The output power decreases from 39.9 dBm at 2 GHz to 39.3 and 38 dBm at 2.6 and 1.6 GHz, respectively, which indicates 1.9 dB output power variation across the band. The power gain is slowly compressed from 16.9 dB at 2 GHz to 16.3 dB and 15 dB at 1.6 GHz and 2.6 GHz, respectively. The output power

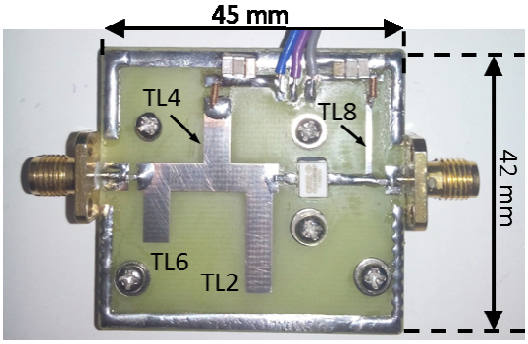

Figure 11. Fabricated Class-J PA within its dimensions.

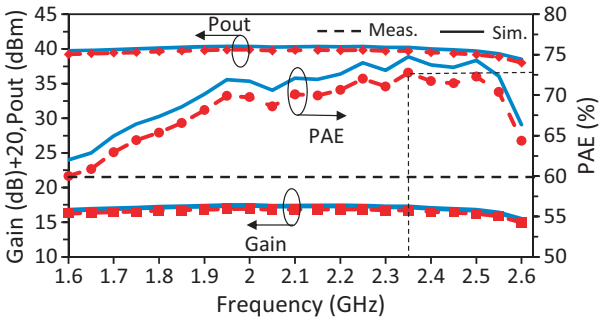

Figure 12. Simulation and measurement results for the output power, PAE, and signal gain in steps of 50-MHz.

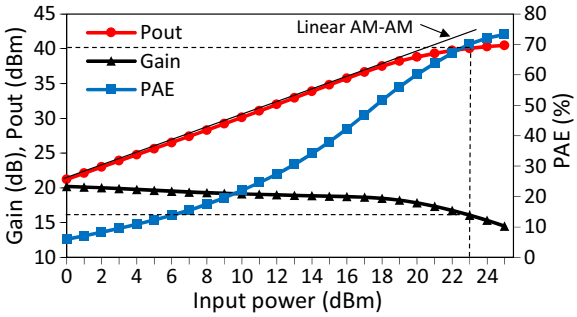

Figure 13. Measurement results in steps of 1-dB for output power, power gain, and PAE versus input power.

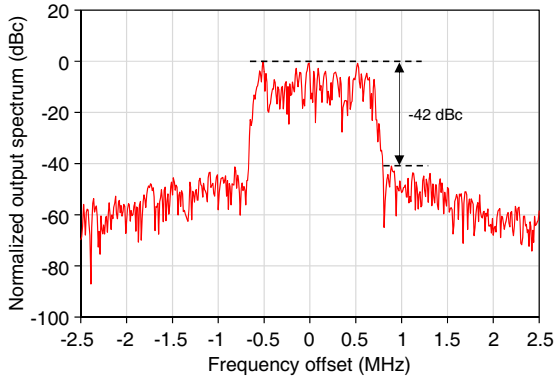

Figure 14. The normalized spectrum of output signal versus frequency offset of 2.1 GHz when the PA is driven by a CDMA modulated signal with 1.2288 MHz bandwidth.

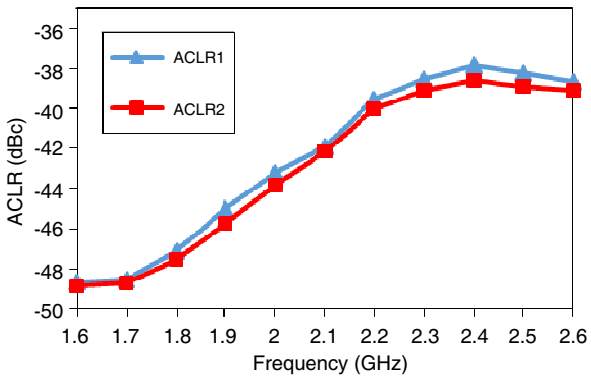

Figure 15. ACLR1 and ACLR2 at the 1.2288 MHz and 2.4576 MHz respectively versus frequency.

and power gain are sharply reduced in out of band as frequency is increased.

The power amplifier is characterized under different input powers in steps of 1-dBm over 0–25 dBm at 2.1 GHz. The measured results for the output power, power gain, and PAE are depicted in Fig. 13. The AM-AM (P_{out}-P_{in}) result in comparison with the linear AM-AM line shows that the PA will provide good linearity performance. The PAE attains close to 73% at 25-dBm input power (P3 dB). The output power at the 1-dB gain compression point (P_{in} = 23 dBm) is 40.4 dBm where PAE = 70.1% and gain = 16.1 dB.

Table 1. Performance comparison of reported PA with different classes.

Ref.	Class	$f_{\min}$–$f_{\max}$ (GHz)	BW (%)	P_{sat} (dBm)	$\text{PAE}^{\dagger\dagger}_{\min}$ (%)	$\text{ACPR}^{**}{}_{\min}$ (dBc)	Tech.
[7]	Class-J	1.4–2.6	60	39.2	60*	−25	GaN
[16]	Class-J	0.5–0.7	33	30	50	-	SiGe
[19]	Class-E	1.8–2.6	36	28.1	34.5	−28.5	CMOS
[17]	HT†	2–3.5	54	30	64	−30	GaN
[18]	Class-J	0.65–1.03	45	31	60	−30	CMOS
[20]	Class-AB	1.2–1.4	15	41	50%	−32	GaN
[21]	Class-AB	1.9–2.5	29	36.9	54.3	−40	GaN
This work	Class-J	1.6–2.6	47	39.9	60	−37.8	GaN

* Drain efficiency has been reported.
† Harmonic tuned.
†† Minimum PAE across the bandwidth.
** The worst ACLR without linearizer.

To investigate the PA linearity performance, the PA is driven by the CDMA signal with 1.2288 MHz bandwidth at the center frequency of 2.1 GHz. The measured signal is shown in Fig. 14. The adjacent channel leakage ratio (ACLR1) and ACLR2 at 1.2288 MHz and 2.4576 MHz frequency offset are slightly close to −41.9 dBc and −42.1 dBc respectively which indicates proper linearity for this class operation. The signal is symmetrical around center showing less memory effect, and therefore, the PA linearity can be further improved by a linearizer if required. Fig. 15 shows the ACLR1 and ACLR2 over frequency bandwidth in steps of 100 MHz. The worst ACRL1 and ACLR2 occur at 2.4 GHz and are −37.8 dBc and −38.6 dBc, respectively. Overall, they are good results for the linearity performance of the Class-J PA without any linearizer.

5. CONCLUSIONS

In this paper, the design of a broadband, high-efficiency, high linearity Class-J RF PA based on GaN HEMT CGH40006P over 1.6–2.6 GHz is explained in detail. The PA gain variation is controlled using an equalizer. The IMN is obtained from small-signal simulation and designed by a broadband low-pass matching network. The simple OMN is proposed to estimate the Class-J requirements. The designed power amplifier shows the PAE greater than 60% and ACLR1 better than −37.8 dBc throughout the band. The output power is bounded in the range of 39.9–38 dBm across the entire band. Table 1 shows the comparison of the designed power amplifier with other state-of-the-art PA designs, including linear and nonlinear classes. In comparison with [7] and [16], the designed PA shows better linearity performance and power efficiency. This PA shows better linearity than [17, 18] but lower $\text{PAE}_{\min}$ while in comparison with [19] and [20], it exhibits better $\text{PAE}_{\min}$ and linearity performances over higher fractional bandwidth percentage. This work in comparison with [21] which used Class-AB shows better $\text{PAE}_{\min}$ but slightly lower linearity.

ACKNOWLEDGMENT

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