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Nonlinear Characteristics of P-I-N Diode Circuits Analyzed by a Physically Based Simulation Method

Hao Wang[1, *], Guodong Wang[1], Xiaolian Liu[1], Ke Xu[2], and Xing Chen[2]

Abstract—Nonlinear characteristics of semiconductor devices play a key role in the performances of circuits, but their modelling is still a big challenge in circuit simulations nowadays. This paper explores modelling nonlinear characteristics of circuits containing semiconductor devices by presenting a modified physically based simulation method. A p-i-n diode microstrip circuit is taken as a sample, and its nonlinear characteristics, such as the power limiting, bistability, and forward recovery characteristics, are simulated and analysed. The applied method demonstrates its good capability and accuracy of modelling the nonlinear characteristics in the simulation, and moreover clarifies the underlying physical mechanisms. In contrast, the Advanced Design System (ADS) software, a popular circuit simulation program based on the equivalent circuit model, fails to reveal some of those nonlinear characteristics.

1. INTRODUCTION

Semiconductor devices are key components in modern electronic circuits [1, 2]. Their nonlinear characteristics are essential for circuit performances, and thus the accurate modelling of those nonlinear behaviours in circuits is fundamental to the circuit design and application. A number of simulation methods have been proposed, e.g., the equivalent-model based simulation method [3–7]; the analytical-model based simulation method [8], etc.. However, the aforementioned approaches suffer from limitations that may preclude their application in some cases. For example, the equivalent or analytical models may lose their accuracy in some special cases such as high-power or high-frequency applications, and moreover, most of them lack a direct physical interpretation for the physical phenomena. Therefore, nowadays, the simulation of nonlinear characteristics for distributed circuits containing semiconductor devices is still a great challenge.

Among the available techniques, the physically based simulation method attracts researchers' interest most particularly for the statistical significance and predictive ability [9–11]. It is based on semiconductor devices' physical models, and solves field equations such as the Maxwell's equations and semiconductor transport equations, to model the electromagnetic wave propagation and charge transport inside semiconductor devices. Hence it is naturally able to accurately simulate semiconductor devices under various conditions and convenient for predicting the physical effects.

In our previous works, a novel physically based simulation method was proposed for the first time [12, 13]. As an extension of previous studies, the proposed method is modified to be able to model distributed structures by introducing a circuit-field co-simulation model. This paper explores applying this modified physically based simulation method to model semiconductor devices' nonlinear characteristics in microstrip circuits and clarify the underlying physical mechanisms. Similar to that in our previous works, a commercial p-i-n diode with model number mot_bal99lt1 is taken as a sample, and a series of experiments are conducted to validate the simulation results.

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* Corresponding author: Hao Wang (skytager@163.com).

[1] School of Physics and Electronic Information Engineering, Henan Polytechnic University, Jiaozuo 454000, P. R. China. [2] College of Electronics and Information Engineering, Sichuan University, Chengdu 610064, P. R. China.

The remainder of this paper is organized as follows. The physically based simulation method is formulated in Section 2. Then, in Section 3, the simulation results of the nonlinear characteristics are presented and compared with measurement data. Finally, conclusions are drawn in Section 4.

2. THE PHYSICALLY BASED SIMULATION METHOD

In principle, the classical set of macroscopic equations for semiconductor devices involves a coupling equation system as follows [12, 14]:

$$\nabla^2\varphi = -\frac{q}{\varepsilon}(p - n + N_t) \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \overrightarrow{J}_n - R \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \overrightarrow{J}_p - R \tag{3}$$

$$\overrightarrow{J}_n = qD_n\nabla n + q\mu_n n\nabla\varphi \tag{4}$$

$$\overrightarrow{J}_p = qD_p\nabla p + q\mu_p p\nabla\varphi \tag{5}$$

$$I = A\left(\overrightarrow{J}_c + \overrightarrow{J}_d\right)\cdot\overrightarrow{\delta} = A\left(\overrightarrow{J}_n + \overrightarrow{J}_p + \varepsilon\frac{\partial\overrightarrow{E}}{\partial t}\right)\cdot\overrightarrow{\delta} \tag{6}$$

where ε is the permittivity; q is the electron charge, N_t is the net doping concentration; φ is the electrostatic potential; n and p are the electron and hole densities; $\overrightarrow{J}_n$ and $\overrightarrow{J}_p$ are the electron and hole current densities; D_n and D_p are the corresponding diffusion coefficients; μ_n and μ_p are the electron and hole mobilities; I is the branch current; A is the cross-sectional area; $\overrightarrow{\delta}$ is a unit vector normal to the cross-section.

The procedure of solving the above Equations (1)–(6) can be simplified to the solution of an increment equation

$$\mathbf{A}\Delta\mathbf{y}_{(k-1)} + \mathbf{B}\Delta\mathbf{y}_{(k)} + \mathbf{C}\Delta\mathbf{y}_{(k+1)} = \mathbf{H}_{(k)} \tag{7}$$

where $y = [\varphi\ n\ p]^T$, $\Delta y = [\Delta\varphi\ \Delta n\ \Delta p]^T$, $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ are 3×3 matrices, $\mathbf{H}$ is a 3×1 matrix. The deriving and solving of Equation (7) is well described in the Reference [12] and need not be detailed here.

For a two-terminal semiconductor device, the branch current is obtained by calculating Equation (7) for an applied voltage V by Newton's method. Thus the terminal current can be represented by $I(V(t))$.

For circuits working at high frequencies, they may contain not only lumped elements but also some distributed structures such as microstrip lines. In this paper, the coupling algorithm for semiconductor devices and distributed structures is realized by the circuit-field co-simulation model [15]. Figure 1 illustrates this model for the interaction between a diode and its external distributed part. As shown in the right side of the figure, the distributed part is described by the finite-difference time-domain (FDTD) technique with spatial domain discretized as Yee cell. Assuming a diode is located in the grid at nodes a and b, the external distributed structure can be modelled as an equivalent sub-circuit consisting of a resistor R_{grid} and a current source I_{EM}. After solving the lumped circuit at the centrepiece of the figure, the diode current, in return, is fed back to the field FDTD iteration formulation by I_S. The values of the equivalent resistor and current source are determined by Equations (8)–(12) [15].

$$\left(I_y^{n+1}\right)_{EM} = \sum_{\beta=j_a}^{\beta=j_b}\left(\delta\alpha_\beta\right)K_{yijk}^{n+1}/\left(R_y^{n+1}\right)_{grid} \tag{8}$$

$$\left(R_y^{n+1}\right)_{grid} = \sum_{\beta=j_a}^{\beta=j_b}\left(\delta\alpha_\beta\right)\Gamma_{yijk}^{n+1}/\left(\delta x\cdot\delta z\right) \tag{9}$$

$$K_{yijk}^{n+1} = \Gamma_{yijk}^{n+1}\cdot LHS_y^{n+1/2}/\left(\delta x\cdot\delta z\right) + \Gamma_{yijk}^{n+1}\left(\tilde{\varepsilon}_{ijk}/\delta t^{n+1} - \tilde{\sigma}_{ijk}/2\right)E_{yijk}^n \tag{10}$$

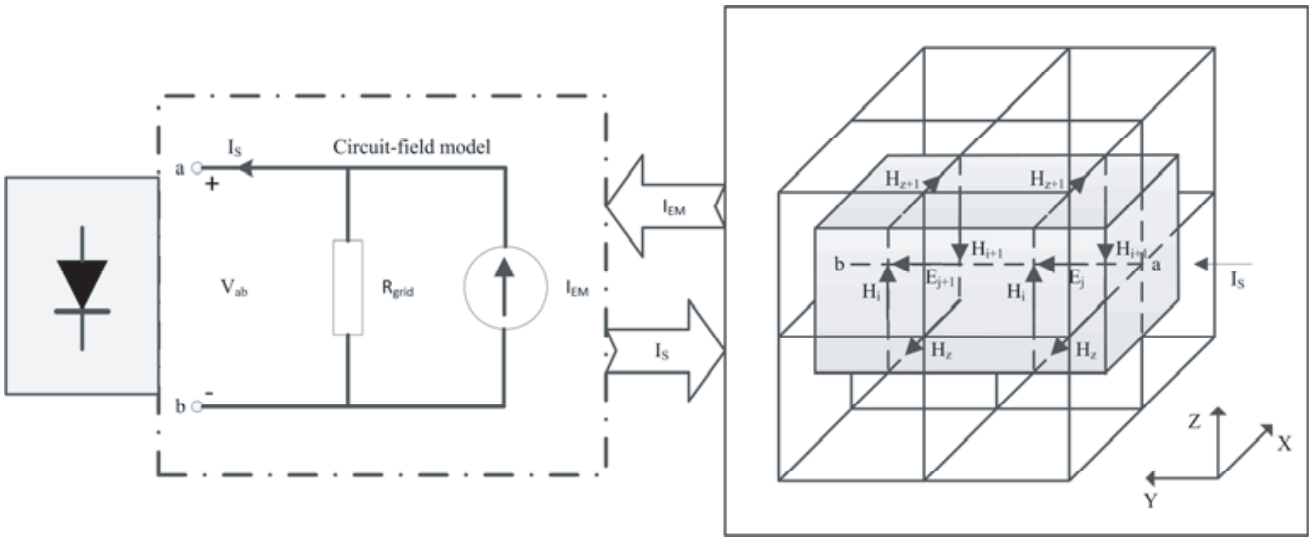


Figure 1. Illustration of the circuit-field model for coupling the external distributed structure with a diode.

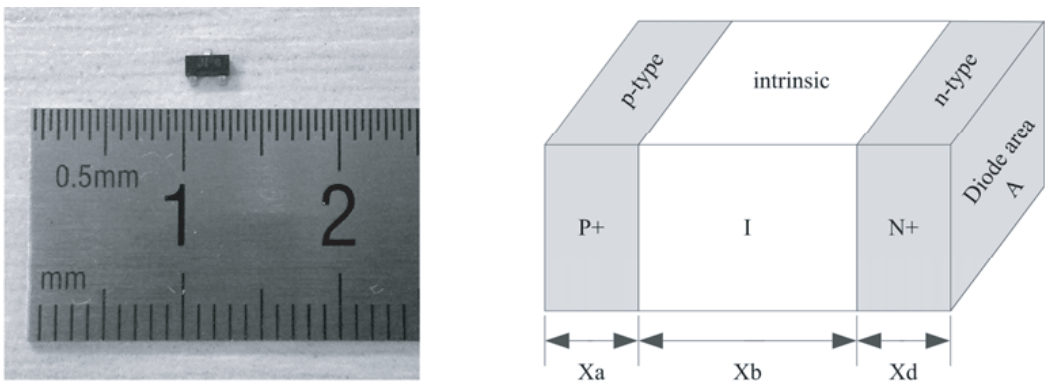
$$\Gamma_{yijk}^{n+1} = 1/\left(\tilde{\varepsilon}_{ijk}/\delta t^{n+1} + \tilde{\sigma}_{ijk}/2\right) \tag{11}$$

$$LHS_y^{n+1/2} = \left(H_{xijk}^{n+1/2} - H_{xijk-1}^{n+1/2}\right) \cdot \delta x_i - \left(H_{zijk}^{n+1/2} - H_{zi-1jk}^{n+1/2}\right) \cdot \delta z_k \tag{12}$$

3. THE SIMULATION OF NONLINEAR CHARACTERISTICS OF A MICROSTRIP P-I-N DIODE CIRCUIT AND DISCUSSION

In this section, some nonlinear characteristics of a microstrip p-i-n diode circuit will be analysed. The chosen mot_bal99lt1 diode and its physical model are illustrated in Figure 2. A Genetic Algorithm (GA) based curve-fitting approach, which is introduced in detail in our previous works [12, 13], is adopted for the extraction of the physical parameters. The extracted results are as follows: the donor and acceptor surface concentrations are $1.8 \times 10^{16}\,\mathrm{cm}^{-3}$ with a Gaussian doping profile to the interior of the diode; the doping level of i-layer is $0.5 \times 10^{10}\,\mathrm{cm}^{-3}$; the widths of the three layers are $Xa = 5\,\mu\mathrm{m}$, $Xb = 1.55\,\mu\mathrm{m}$ and $Xd = 0.5\,\mu\mathrm{m}$ respectively; the cross-sectional area of the diode is $A = 0.7 \times 10^{-4}\,\mathrm{cm}^2$.

A microstrip p-i-n diode circuit (see Figure 3) is fabricated. It consists of two microstrip lines connected together on Teflon substrate with relative dielectric constant $\varepsilon_r = 2.65$ and thickness



(a) (b)

Figure 2. (a) A p-i-n diode with model number mot_bal99lt1 and (b) its physical model.

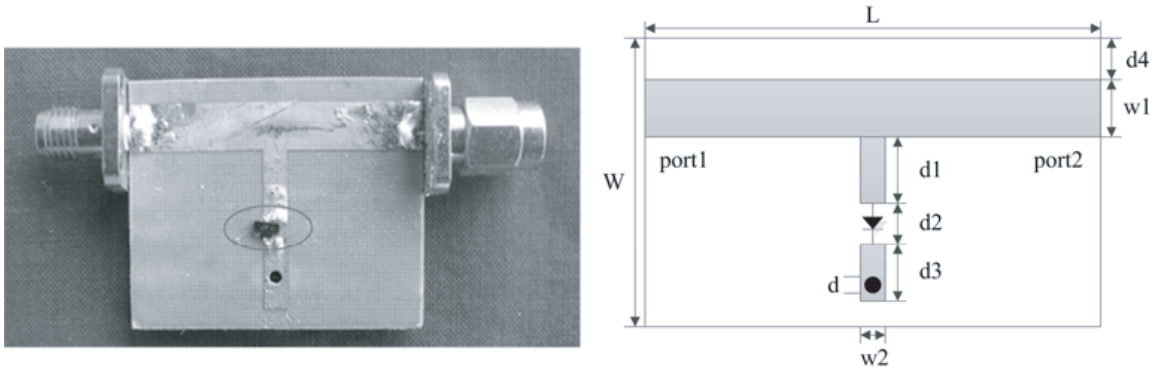


Figure 3. (a) Photo and (b) schematic plot of the microstrip diode circuit.

$h = 2\,\text{mm}$. One of the microstrip lines is connected to SMA connectors at both ends. The other microstrip line has a gap, d_2, of width 1.35 mm with one end grounded through via hole. A mot_bal99lt1 p-i-n diode is mounted across the gap. Other geometrical parameters are as follows (unit mm): $L = 32.4$, $W = 28.3$, $w_1 = 5.4$, $w_2 = 2.7$, $d = 1$, $d_1 = d_3 = 8.1$, and $d_4 = 2.7$.

3.1. The Power Limiting and Bistability Characteristics

The microstrip circuit, shown in Figure 3, functions as a simple diode limiter with a power limiting characteristic. It has two ports. Port 1 is the input port where power is applied, and port 2 is the output port. The output power versus input power for the microstrip circuit at frequencies of 250 and 600 MHz are simulated by the modified physically based simulation method and the ADS respectively, and then compared with that obtained from experiment, as shown in Figure 4. The measurement is performed by using a CETC power meter AV2432 with an Agilent vector signal generator E8267C. In general, the two modelling approaches both predict the power limiting characteristic, which indicates that the simulated output power is lower than the input power. Moreover, one can observe that the simulation results from both modelling approaches agree well with the measurement ones at frequency of 250 MHz. But for the frequency of 600 MHz, the modified simulation method is more accurate than ADS. In that case, an interesting nonlinear phenomenon, named bistability effect [16–18], occurs. As illustrated in Figure 4(b), the output power increases almost linearly with the input power. However, at the input power of about 16 dBm, there is a jump of the output power. This complicated nonlinear property is successfully predicted by the proposed physically based simulation. In contrast, ADS does not possess the capacity of simulating this physical effect.

3.2. The Forward Recovery Characteristics

The forward recovery characteristic of p-i-n diodes refers to the terminal voltage overshoot phenomenon when a diode turns on abruptly under the influence of the external circuit. This characteristic is very important to p-i-n diodes since it affects the diode switching speed significantly.

Figure 5 shows the forward recovery characteristic of the mot_bal99lt1 p-i-n diode. As can be seen in this figure, the measured terminal voltage (solid line) is a little larger than the clamping level at some phase of the forward voltage period, which is denoted by an ellipse. The measurement is conducted under the condition that a 15 dBm sine-wave signal with frequency 50 MHz is injected into the port 1 of the microstrip circuit (see Figure 3) while the port 2 is matched. And a Tektronix TDS1012 oscillograph is used for measurement of terminal voltage.

The modelling results from the presented simulation method (black dot) and ADS (white dot) are also shown in Figure 5. As illustrated in the figure, the proposed method clearly displays the forward recovery characteristics while ADS fails to reveal this nonlinear behaviour, which demonstrates the limitation of the equivalent-model based simulation.

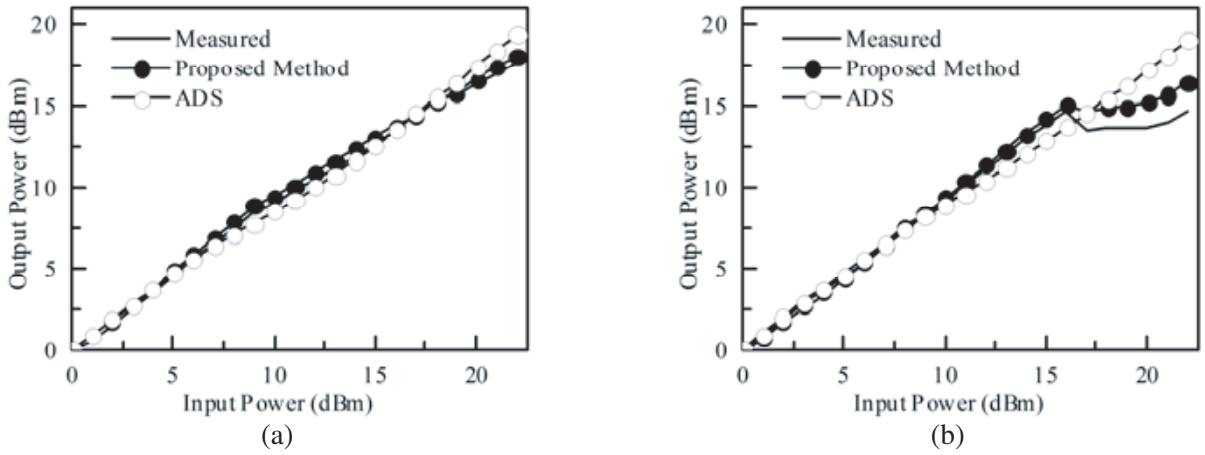


Figure 4. Output power vs. input power of the microstrip circuit for (a) 250 MHz and (b) 600 MHz.

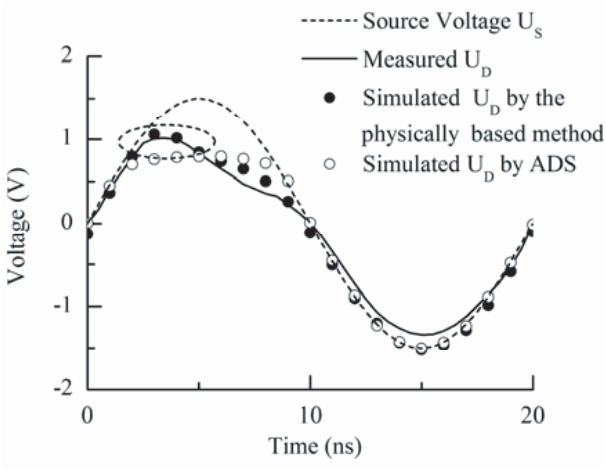


Figure 5. The measured and simulated terminal voltage waveforms of the chosen p-i-n diode.

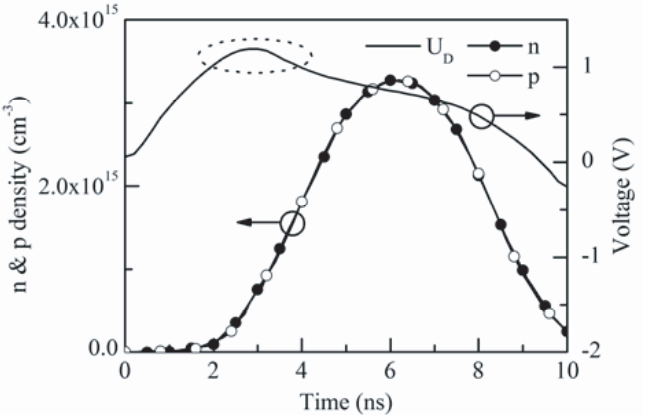


Figure 6. The simulated carrier densities at the center of i-layer during a forward voltage period.

Moreover, the forward recovery characteristic of the chosen p-i-n diode can be clearly and intuitively analysed by the physically based simulation. As illustrated in Figure 6, at the beginning of a forward voltage period, the carrier densities inside i-layer is still in low-level, which means that the diode has a high volume resistivity at this stage. Thus the p-i-n diode actually behaves like a capacitor. This makes the terminal voltage increase with the input voltage and finally results in the rise of the carrier densities. However, when the carrier densities inside i-layer increase to $1.0 \times 10^{15}\,\mathrm{cm}^{-3}$, the diode would have low impedance. And this makes the terminal voltage drop to the clamping level.

In this paper, the proposed algorithm is coded in MATLAB and implemented on a personal computer equipped with an Intel Q8200 processor of four cores and 8-GB memory. In the present implementation, a one-dimensional (1-D) discretization grid that is independent of the 3-D FDTD mesh is adopted for the physical model of the p-i-n diode. Hence, the central processing unit (CPU) time needed for the proposed algorithm mainly depends on the total number of FDTD cells. In this work, the FDTD problem space is $63 \times 60 \times 48$ cells, while the p-i-n diode's physical model employs a 50 point mesh. The FDTD grid is terminated with the convolutional perfect matched layer (CPML) absorbing boundary condition. The time-step size is determined by the Courant-Friedrichs-Lewy (CFL) condition, and the total time consuming in the forward recovery problem is 110 minutes for about 20 thousand of timesteps in one period. But it is worth noting that the alternating direction implicit finite-difference

time-domain (ADI-FDTD) method can be used for avoiding the CFL condition restraint, which will reduce the simulation time significantly. As a contrast, although the ADS simulation time is less than 10 seconds, it fails to reveal the nonlinear characteristics since it is based on the equivalent circuit model.

4. CONCLUSION

Nonlinear characteristics of semiconductor devices significantly affect circuits' performances, but some of them are difficult to, or even cannot be simulated by current available circuit simulation methods and corresponding software. This work explores simulating nonlinear characteristics of semiconductor devices in microstrip circuits by modifying a physically based simulation method. Nonlinear characteristics such as the power limiting, bistability and forward recovery characteristics of a pin diode distributed circuit are analysed as a sample. In the simulation examples, this physically based approach demonstrates a great capacity of accurately revealing devices' nonlinear properties, and moreover providing clear physical pictures for those properties. The capacity of accurate simulation and providing physical mechanism for the nonlinear characteristics of semiconductor devices in circuits makes this approach a powerful and effective tool for the semiconductor and distributed circuit analysis.

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