Capacitive Loaded U-Slot Defected Ground Structure for Bandstop Filter with Improvement Q Factor

Gang Liu, Zhuo-Ying Wang, Jia-Jia Wu, and Lin Li[1, *]

Abstract—A novel capacitive loaded U-slot defected ground structure (DGS) is presented in this letter to provide narrowband rejection property. The principles for the selective rejection and the strategies for size-reduction and external Q-factor improvement are detailed based on transmission line equivalent model and the lumped parallel RLC model developed from transmission line model at resonance frequency. The design concept is well validated by the design and measurement of an exemplary high Q BSF.

1. INTRODUCTION

Recently, defected ground structures (DGSs) have drawn much interest for BSFs construction since they have compact size and excellent band gap characteristics. However, conventional dumbbell-shaped DGSs are not satisfactory in narrowband and stiff rejection since they have low Q-factor.

To suppress unwanted signals closely located from the desired signal in the spectrum, many high-Q DGSs are proposed to develop narrow-band BSFs. In [1], a two-layer improvement Q DGS BSF with a parasitic stub is proposed. However, this multi-layer configuration increases both design complexity and fabrication cost. Changing the shape of the etched patch is another effective method to increase Q-factor. T-shape [2], U- and V-shape [3], E-shape DGS [4], open loop DGS [5], C-shape DGS [6] and double hairpin-shaped [7] are proposed by researchers to enhance Q-factor. Nevertheless, in these papers, Q improvement mechanism still requires further investigation, since all lumped elements of the equivalent models are extracted from EM simulation.

In this letter, a novel capacitive loaded U-slot DGS is presented. To gain a deep insight into the Q improvement mechanism, transmission line model is initially constructed, and lumped model is developed from transmission line model. Based on these two models, electrical parameters can be extracted from the physical dimensions directly, which facilitates design. Besides, equivalent circuit analysis reveals that both the size-miniaturization and Q-improvement mechanism are achieved by the incensement of capacitive element of the DGS. For demonstrative purpose, a high external Q-factor BSF is designed, fabricated, and measured using the proposed principles. Good agreement is obtained between the measured and the simulated performance.

2. MODELING AND THEORETICAL ANALYSIS

Figure 1 shows a geometrical diagram of the proposed U-slot DGS with microstrip line on its top. This U-slot DGS has the width W_S, arm length L_2, and arm distance d. Two lumped capacitors are soldered at quarter and three-fourths of the total slot, respectively. The distance between the lumped capacitor and edge of the U-slot is L_1. Obviously, $L_1 = L_2 - 0.5d$ is satisfied.
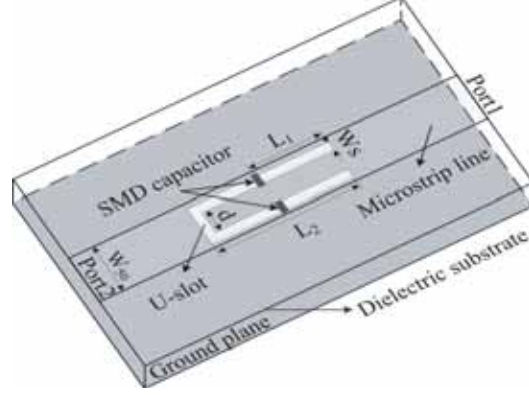
**Figure 1.** Three-dimensional view of the capacitive loaded U-slot DGS.

Similar to the methods presented in [9], the proposed U-slot DGS can be depicted by the equivalent model in Figure 2. In this model, the slots are characterized as transmission-line with the characteristics impedance of Z_S. The capacitor of C_P represents the capacitance of the lumped capacitor. The resistor of R_A refers to all of the resistive effects of the proposed U-slot DGS, i.e., metal ohmic loss, and dielectric loss. The transformer in the circuit depicts the electromagnetic (EM) couplings between the top microstrip line and the bottom DGS. The input admittance looking at the input port of the transform can be derived as:

$$Y_1 = \frac{1}{R_A} - j\frac{2}{Z_S}\frac{Z_S\omega C_P + \tan\theta_1 - \cot\theta_1}{Z_S\omega C_P \tan\theta_1 - 2} \tag{1}$$
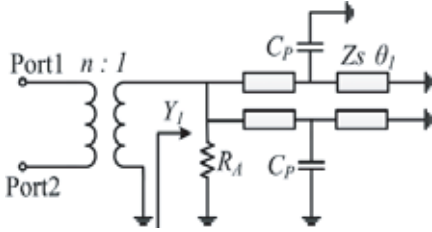
Figure 2. Transmission line equivalent circuit of model of the proposed DGS.
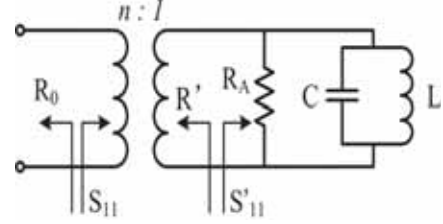
Figure 3. Lumped element circuit model of the proposed DGS.

It can be easily deduced that the signal through the microstrip line will be rejected around parallel resonance of the DGS. And the resonance condition should satisfy the following equation:

$$2\pi Z_S f_0 C_P + \tan\theta_1 - \cot\theta_1 = 0 \tag{2}$$

The model in Figure 2 can be transformed to the circuit in Figure 3 by expressing the capacitive loaded transmission structure in the resonating state as a parallel lumped RLC circuit. Now the input admittance looking at the input port of the transformer in the transmission-line topology in Figure 2 can be converted in the following form

$$Y_2 = \frac{1}{R_A} + j\frac{\omega^2 - \omega_0^2}{\omega}C \tag{3}$$

Let $Y_1 = Y_2$ and $\partial Y_1/\partial\omega = \partial Y_2/\partial\omega$, the parallel capacitance of the equivalent circuit, shown in Figure 3, can be obtained as:

$$C = -\frac{\left(Z_S^2\omega_0 C_P \tan\theta_1 - 2Z_S\right)\left(Z_S C_P + \sec^2\theta_1\frac{\theta_1}{\omega_0} + \csc^2\theta_1\frac{\theta_1}{\omega_0}\right)}{\left(Z_S^2\omega_0 C_P \tan\theta_1 - 2Z_S\right)^2} \tag{4}$$

$$\frac{- (Z_S\omega_0 C_P + \tan\theta_1 - \cot\theta_1)\left(Z_S^2 C_P \tan\theta_1 + Z_S^2\omega_0 C_P \sec^2\theta_1\frac{\theta_1}{\omega_0}\right)}{}$$

Additionally, the inductance L of the lumped RLC circuit can be expressed by

$$L = \frac{1}{\omega_0^2 C} \tag{5}$$

where ω_0 is the angular resonance frequency.

That is to say, for a set of predefined Z_S and ω_0, the values of lump elements in Figure 3 can be calculated using Equations (4) and (5).

Next, the turn ratio n in Figure 3 can be extracted by combining the full-wave EM simulations and the equivalent circuit. For a high external Q-factor DGS, it is feasible to assume that the resistance R_A is much larger than the port impedance R_0, so the external Q-factor of the RLC resonator circuit in Figure 3 is

$$Q = \omega_0 C R' = \frac{\omega_0 C R_0}{n^2} \tag{6}$$

And at resonance external Q-factor can also be expressed by

$$Q = \frac{\tau_{S_{11}}(\omega_0)\,\omega_0}{4} \tag{7}$$

where $\tau_{s11}(\omega_0)$ is the group delay at resonance.

The above relation is valid for any single resonant circuit [10], so n can be extracted from Eq. (6) once external Q-factor is obtained from Eq. (7) by using the EM simulated group delay. When the values of the inductor, capacitor, and turn ratio are determined, the value of R_A can be obtained by using curve-fitting method.
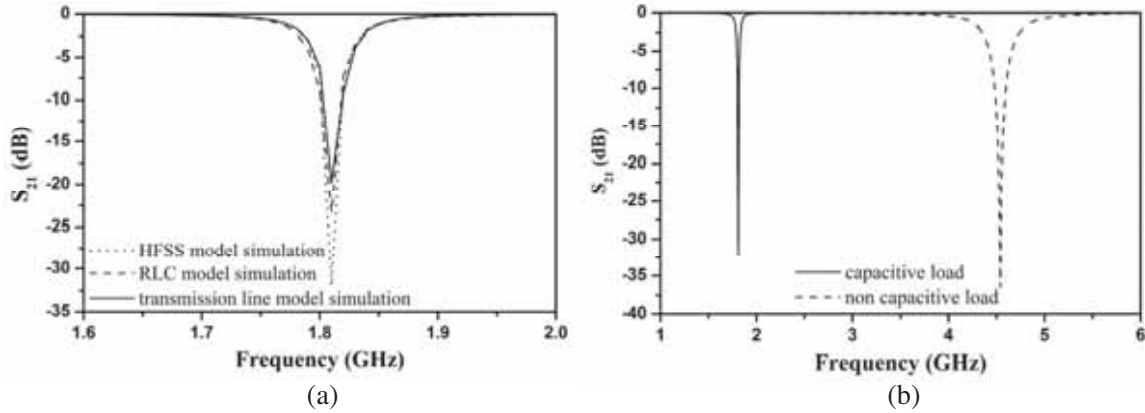
Figure 4. (a) The EM simulated S_{21} of different models with capacitive load. (b) The EM simulated S_{21} of U-slot with and without capacitive load.

To verify the feasibility of the equivalent circuit, Figure 4(a) shows the comparison of EM simulated S_{21} between the RLC circuit model, transmission line model, and HFSS model. Three models are designed to have the same resonant frequency 1.81 GHz, and the loaded capacitance $C_P = 2.2\,\text{pF}$. Parameters of HFSS model in Figure 1 are arranged as $W_S = 0.2\,\text{mm}$, $L_1 = 6\,\text{mm}$. Which corresponds to $Z_S = 105\,\Omega$, $\theta_1 = 18.5°$ of transmission line model in Figure 2. Lump elements of RLC circuit model in Figure 3 are $C = 4.35\,\text{pF}$, $L = 1.78\,\text{nH}$. Good agreements between the three circuit models can be observed in Figure 4(a), indicating that the proposed equivalent circuit is available for the description of the proposed DGS. In addition, the EM simulated S_{21} (HFSS model) of U-slot with and without capacitive load are compared in Figure 4(b), as shown in Figure 4(b), the proposed U-slot DGS has lower notch frequency and higher external Q-factor.

Let f_{r0} be the conventional U-slot's natural fundamental resonant frequency, then θ_1 will be about $\pi/4$ at f_{r0}, while $\theta_1 < \pi/4$ at the proposed DGS's resonant frequency f_{r1} can be derived from Eq. (2). That is to say, the proposed capacitive loaded U-slot works at a lower frequency than the U-slot's natural resonant frequency f_{r0}.
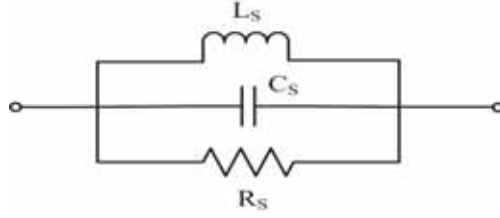
Figure 5. Simplified lumped element circuit model.

As to Q improving effects, this phenomenon can be explained by the simplified equivalent lumped circuit in Figure 5. This simplified model is developed from the circuit in Figure 3 by absorbing turn ratio into the value of the lumped elements. The following three equations relate the new equivalent circuit to the initial model in Figure 3.

$$C_S = \frac{C}{n^2} \tag{8}$$

$$L_S = n^2 L \tag{9}$$

$$R_S = n^2 R_A \tag{10}$$

Obviously, the model in Figure 5 has the same form as the model in [4], and thus deep insight can be gained by comparing the proposed DGS with conventional DGS.

Table 1 compares the proposed U-slot DGS with different capacitive loads and the unloaded U-slot DGS. All these exemplary DGSs in Table 1 have the same resonant frequency 1.8 GHz. As shown in Table 1, the capacitive element of the DGS increases largely with the increasement of the loaded capacitor. As a result, for a specified resonant frequency, the required slot length could thereby be reduced. Furthermore, it can be deduced from (6) that external Q-factor also increases since it is directly proportional to C_S. In short, both the size-miniaturization and Q-improvement effects are realized by adding capacitive load, which provides extra capacitance for proposed DGS.

Table 1. The circuit parameters value with different capacitance.

| C_P [pF]	θ [°]	external Q-factor	L_S [nH]	C_S [pF]
0	180	9.38	0.723	10.776
0.5	146	15.38	0.616	12.735
1	118.4	21.43	0.374	20.980
1.5	96.8	29.51	0.285	27.429
2	80	38.3	0.228	34.367

Table 2. Comparison with other reported DGS unit.

| Method	Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	Proposed
Size (λ_0^2)	0.005	0.001	0.001	0.007	0.001	0.002	0.008	0.001
external Q-factor	1.53	8.71	36.05	31.67	15	57	49.7	45

A comparison of the proposed DGS with other reported high external Q-factor DGSs is listed in Table 2. Compared with other DGS structure, proposed capacitive loaded U-slot DGS unit behaves compact size and high external Q-factor. In addition, it must be pointed out that the external Q-factor of the proposed U-slot can still be increased significantly if a larger capacitor is employed in the design.

3. FABRICATION AND MEASUREMENTS

Increasing DGS unit can improve the suppression degree; however, too many units will increase circuit area. So, choosing 3–4 units to carry on the design is the most appropriate. To confirm the proposed idea, a BSF using three cascaded proposed DGSs operating at 1.8 GHz is designed. Figure 6 illustrates the configuration of the proposed structure. Figure 7 shows the top and bottom views of the fabricated three cascaded U-slot DGSs. The dimensions for each U-slot are $L_2 = 11.2$ mm, $W_S = 0.2$ mm, $d = 1.6$ mm and the characteristic impedance of the microstrip line is $50\,\Omega$, embedded capacitor $C_P = 2.2$ pF is achieved by soldering standard ceramic capacitor, 0603 series from Murata Manufacturing Co., Ltd. The distance between each U-slot is fixed as $S = 16.8$ mm, that is about a quarter of a wavelength at the center frequency. Proposed prototype is implemented on a substrate with thickness of 1.0 mm, relative dielectric constant of 2.65, and the loss tangent of 0.02. The proposed capacitive loaded U-slot DGS unit has a simple structure as well as a quite compact size of merely 2.75 mm × 11.2 mm, corresponding to $0.001\lambda_0^2$ ($0.106\lambda_0 \times 0.067\lambda_0$), where λ_0 is the guided wavelength of free space at the central frequency. Moreover, the capacitive loaded U-slot DGS unit provides a high external Q-factor of 45.
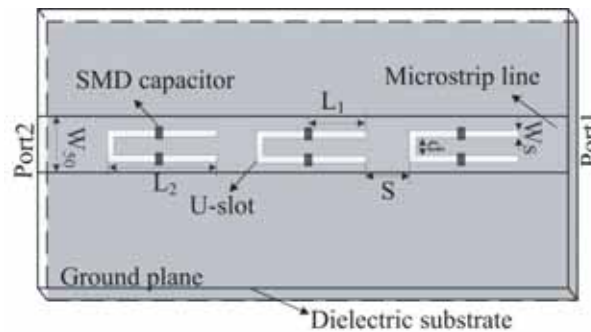

Figure 6. Three-dimensional view of the three cascaded capacitive loaded U-slot DGSs.
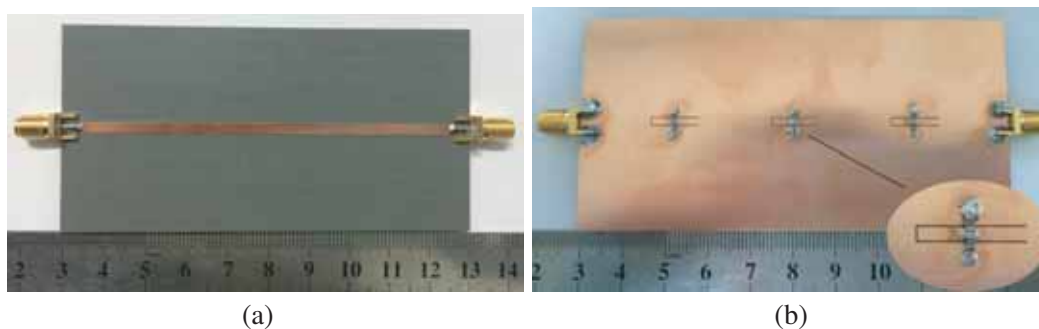
Figure 7. Photograph of proposed capacitive loaded U-slot DGSs. (a) Top view. (b) Bottom view.

The EM simulations using Ansoft HFSS and the measurements using Agilent 8510C vector network analyzer are displayed in Figure 8. Good agreement can be observed between the measured and simulated frequency responses. The slight difference between the simulated and measured bandwidths can be ascribed to fabrication tolerances as well as soldering lumped capacitors. As shown in Figure 8, the fabricated BSF with three cascaded U-slot DGSs rejects the signal at the central frequency 1.8 GHz with more than 20 dB suppression, and this 3 dB fractional bandwidth is about 5%. In addition, the proposed structure also show flat and low-loss properties in the passband characteristic.
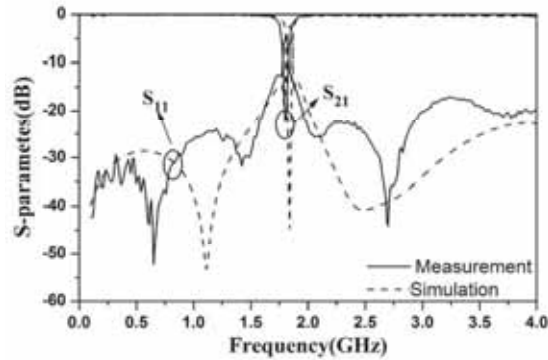
Figure 8. Simulation and measurement of fabricated DGS.

4. CONCLUSIONS

A novel capacitive loaded U-slot DGS is proposed in this paper. Equivalent circuit model and corresponding parameter extraction are developed to interpret the working mechanism of the proposed DGS. Theoretical analysis, simulation and measurement show that the proposed DGSs have lower resonant frequency, high external Q-factor and flexible regulatory mechanism. The fabricated BSF with three cascaded proposed U-slot DGSs provides very narrow $3\,\mathrm{dB}$ fractional bandwidth of about 5%.

ACKNOWLEDGMENT

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