Progress In Electromagnetics Research M, Vol. 52, 181–190, 2016

A New Diode-Clamped Multilevel Inverter for Capacitor Voltage Balancing

Shunji Shi[1], Xiangzhou Wang[1], Shuhua Zheng[1, *], and Fei Xia[2]

Abstract—In this paper, a new diode-clamped multilevel inverter for capacitor voltage with inserted inductors is proposed. The key is to solve the voltage unbalance of diode-clamped multilevel inverter (DCMLI), which utilizes fewer switches and adopts a simpler control strategy. In this way, the cost and volume of the DCMLI can be effectively reduced. Firstly, the new five-level inverter topology is analyzed in detail under different operation modes. Then, the proposed topology extended to $(2n+1)$ level inverter is introduced and discussed. Finally, both simulation and experiment results are demonstrated to verify the validity of the proposed topology.

1. INTRODUCTION

With the increase of output power density of power converters, multilevel converters become hot points [1, 2]. Compared with conventional two-level converters, multilevel converters show great advantages such as: high power quality of waveforms, low switching losses, high-voltage capability and low electromagnetic interference (EMI) [3–9]. In general, multilevel converters can be divided into three types: diode-clamped multilevel converters, flying capacitor multilevel converters and cascaded multilevel converters with separated DC sources [10–13].

The diode-clamped multilevel inverter (DCMLI) catches lots of attention due to its easily pre-charged DC capacitors, simple switch control and less complex protection circuit of inverter [14, 15]. However, DCMLI suffers from voltage unbalance if the voltage levels exceed three, then all the aforementioned advantages will disappear. Therefore, it is essential to keep the DC capacitor voltage balanced [16].

Different methodologies have been proposed to deal with the unbalance of DC capacitors voltage. One is changing the switching pattern and optimizing control methods of switches [17, 18], where complex control system is required. Another method is to install the parallel circuit on DC side of the inverter, such as conventional chopper circuit (Fig. 1(a)), flying capacitor based chopper circuit (FCBC) (Fig. 1(b)) [16], circuit based on RSCC (CBR) (Fig. 1(c)) [19–21], or parallel switch-based chopper circuit (PSBC) (Fig. 1(d)) [22]. All these methods need hardware reconfiguration. For instance, when being used in five-level inverter, conventional chopper needs four switches and two inductors, and the peak voltage of the extra switches is twice as much as main switches. Although FCBC can reduce the peak voltage, it requires double switches and two additional capacitors. Moreover, the control system of FCBC is also complicated. CBR has the same components of FCBC, but the volume of capacitors and inductors can be reduced. PSBC can reduce the number of extra switches to three, and simplify the control system. However, three additional diodes and one additional inductor are needed.

Given that all the aforementioned methods require more extra components or a complex control system, a new topology with inserted inductor is proposed in this paper to further reduce the extra

Received 6 October 2016, Accepted 29 November 2016, Scheduled 12 December 2016
* Corresponding author: Shuhua Zheng (zhengshuhua@bit.edu.cn).
[1] School of Automation, Beijing Institute of Technology, Beijing 100081, China. [2] Department of Information and Communication Division, State Grid Liaoyang Electric Power Supply Company, Liaoning 111000, China.

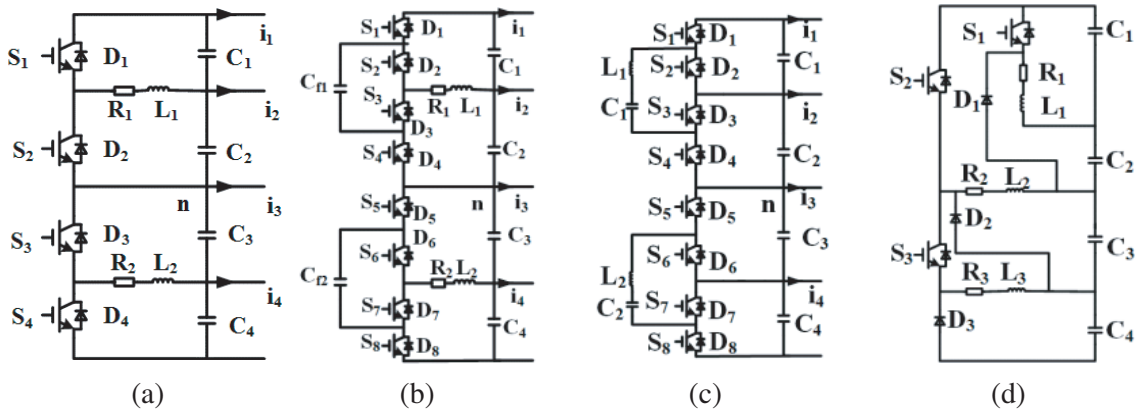


Figure 1. The method to install the parallel circuit on DC side of the inverter. (a) Conventional chopper. (b) Three-level flying capacitor based chopper. (c) Voltage-balancing circuit based on an RSCC. (d) Parallel switch-based chopper circuit.

components and simplify the control system. The proposed topology is analyzed in different modes in detail. Then, the proposed topology used in five-level inverter is verified by the simulation and experimentation.

2. PROPOSED TOPOLOGY

In this section, a new topology with an inserted inductor (TWII) for capacitor voltage balancing is presented. TWII is shown in Fig. 2. It can balance the voltages of capacitors with simple control system with only two inductors incorporated, which is an extraordinary advantage compared with the aforementioned methods in [16–22].

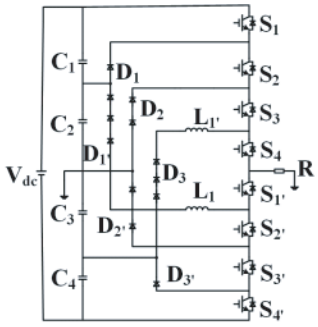


Figure 2. Proposed topology.

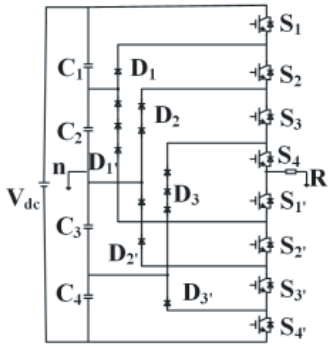


Figure 3. Conventional topology.

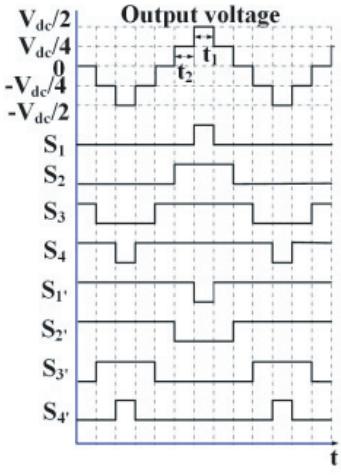


Figure 4. Modulation strategy.

2.1. Operation Principle of the Proposed Topology

A five-level inverter and modulation strategy of the inverter are shown in Fig. 3 and Fig. 4, respectively. Let's denote the point n as neutral reference, and the output voltage of the inverter has five levels. For the convenience of theoretical analysis, it is assumed that all the switches are ideal, $C_1 = C_2 = C_3 = C_4 = C$, and the load is a resistor R.

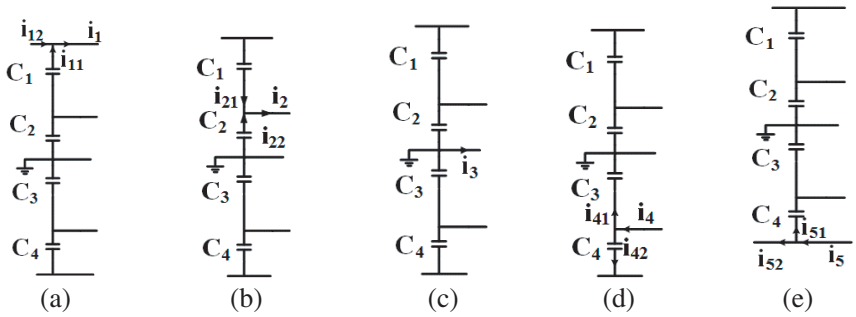


Figure 5. The five modes with different output current. (a) i_1. (b) i_2. (c) i_3. (d) i_4. (e) i_5.

The five modes with i_1–i_5 shown in Fig. 5 correspond to output voltage $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$, respectively. In mode (a), i_1 is divided into i_{11} and i_{12}. C_1 and C_2 are discharged by i_{11}. Correspondingly in mode (e), i_5 is divided into i_{51} and i_{52}. C_1 and C_2 are charged by i_{52}. As $i_{11} = i_{52} = V_{dc}/4R$, i_1 and i_5 do not cause voltage unbalance within one cycle. In mode (b), i_2 is divided into i_{21} and i_{22}. C_2 is discharged by i_{22}. Correspondingly in mode (d), i_4 is divided into i_{41} and i_{42}. C_2 is charged by i_{41}. As $i_{22} = 3V_{dc}/16R$ and $i_{41} = V_{dc}/16R$, the voltage of C_2 decreases within one cycle [22–25]. In mode (c), $i_3 = 0$ and does not cause voltage unbalance. In summary, the voltage change ΔU of one capacitor in one cycle is given by:

$$\Delta U = \frac{i_2 t_2}{C} \tag{1}$$

where t_2 is the duration of i_2, as shown in Fig. 4.

To balance the voltages, we turn on $S_{1'}$ for time t_b when output voltage is $V_{dc}/2$, and turn on S_4 for time t_b when output voltage is $-V_{dc}/2$ by using TWII shown in Fig. 2 with the modulation strategy shown in Fig. 7. Then the voltages of capacitors can be balanced. To simplify analysis, it is assumed that the compensating inductors L_1 and L_1' are ideal.

As the two modes are the same, only the mode shown in Fig. 6 is analyzed, where t_b is the compensating time and t_r the recession time. As for mode (a), when S_1' is turned on, the voltage on L_1 is $V_{dc}/4$. i_{L1} (the current of L_1) passes through S_1–S_4 and S_1', and increases linearly with slop $V_{dc}/4L_1$ from 0. When S_1' is turned off in mode (b), i_{L1} passes through the anti-parallel diodes of S_2'–S_4' and decreases from I_{mL1} linearly with slop $3V_{dc}/4L_1$. Fig. 9 shows the waveform of i_{L1}. i_{L1} can be divided into i_{L11} and i_{L12}, as shown in Fig. 6. i_{L11} discharges C_1. Meanwhile, i_{L12} charges C_2, C_3, and C_4. As $i_{L11} = 3i_{L1}/4$ and $i_{L12} = i_{L1}/4$, the compensating voltage ΔU_b of one capacitor in one cycle is given by:

$$\Delta U_b = \frac{V_{dc} t_b^2}{12 L_1 C} \tag{2}$$

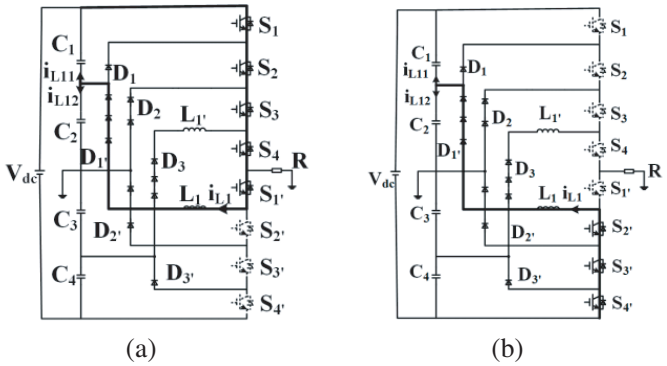


Figure 6. The compensating mode during different time. (a) t_b. (b) t_r.

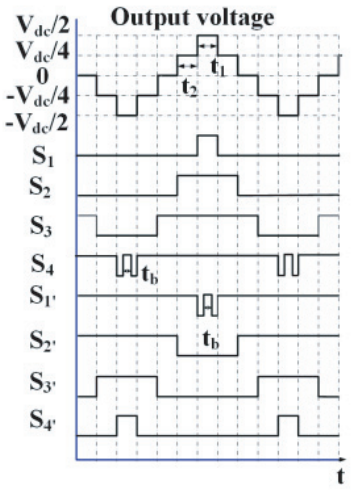


Figure 7. Modulation strategy of TWII.

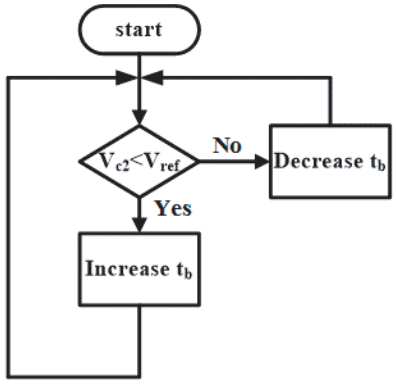


Figure 8. Control strategy of TWII.

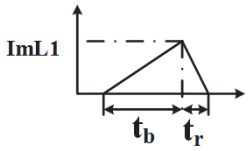


Figure 9. Waveform of i_{L1}.

When ΔU_b is equal to ΔU, the voltages of all capacitors can be balanced and what can be derived is:

$$L_1 = \frac{t_b^2 R}{3t_2} \tag{3}$$

It needs to be noted that there are some limitations:

$$t_b + t_r = \frac{4t_b}{3} \tag{4}$$

$$I_{mL1} + \frac{V_{dc}}{2R} < I_m \tag{5}$$

where I_m is the maximum allowable current of main switches, and I_{mL1} is the peak of i_{L1}:

$$I_{mL1} = \frac{V_{dc} t_b}{4L_1} \tag{6}$$

They not only help to define the volume of inserted inductors L_1 and L_1', but also estimate compensating time t_b.

The control strategy of upper capacitors C_1, C_2 and lower capacitors C_3, C_4 are the same, shown in Fig. 8. Since the sum of the voltage of C_1, C_2 is constant within one cycle, only one of them needs to be controlled. According to Fig. 8, when V_{C2} is less than V_{ref}, t_b should be increased. Correspondingly, t_b should be decreased when V_{C2} exceeds V_{ref}. Then the voltages are balanced. It can be seen that the control system is very simple.

2.2. Proposed Topology Extended to $(2n + 1)$ Level

The proposed topology extended to $(2n + 1)$-level is shown in Fig. 10(a). When the level of inverter increases two, the convention chopper needs to increase two switches and inductors. FCBC, as well as CBR, needs to increase four switches, two inductors and two capacitors. PSBC needs to increase two switches, diodes and inductors. However, TWII only needs to increase two inductors. Table 1 shows the required components of the five methods used in $(2n + 1)$ level. It can be seen that the reduction of extra components of TWII is more remarkable as the level of inverters increases.

When TWII is extended to $(2n + 1)$ level, the compensating method is similar to what is used in five-level. Fig. 10(b) shows the output voltage. When the output voltage is $mV_{dc}/2n$ $(0 < m < n)$, i_m between C_m and C_{m+1} occurs as shown in Fig. 10(c), and the voltage unbalance ΔU_m caused by i_m in one cycle is:

$$\Delta U_m = \frac{2mt_{m+1} i_m}{nC} \tag{7}$$

Table 1. Extra components of all methods when expended to $(2n+1)$ level.

Methodology	Inductor	Switch	Capacitor	Diode
TWII	$2(n-1)$	0	0	0
Conventional Chopper	$2(n-1)$	$2n$	0	0
FCBC and CBR	$2(n-1)$	$4n$	$2(n-1)$	0
PSBC	$2n-1$	$2n-1$	0	$2n-1$

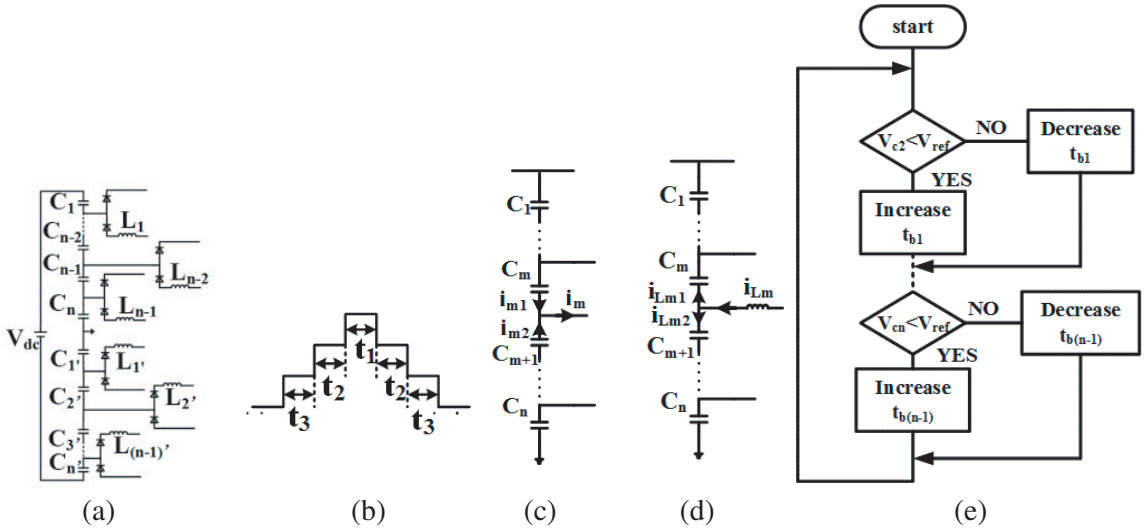


Figure 10. TWII used in $(2n+1)$ level inverter. (a) Topology of TWII. (b) Output voltage. (c) Mode with output current i_m. (d) Mode with compensating current i_{Lm}. (e) Control system.

where t_{m+1} is the duration of i_m, as shown in Fig. 10(b).

Figure 10(d) shows the corresponding compensating mode where the compensating voltage U_{bm} caused by i_{Lm} is:

$$U_{bm} = \frac{m^2 V_{dc} t_{bm}^2}{8\,(2n-m)\,CL_m} \tag{8}$$

It can be noted that there are two chances to compensate in one cycle when $m=1$. When $m>1$, there are four changes in one cycle. Therefore, what can be derived is:

$$L_m = \left\{ \begin{array}{ll} \dfrac{nRt_{b1}^2}{2\,(n-1)\,(2n-1)\,t_2} & m{=}1 \\ \dfrac{mnRt_{bm}^2}{(n-m)\,(2n-m)\,t_{m+1}} & m>1 \end{array} \right\} \tag{9}$$

Similarly, the limitations are:

$$t_{bm} + t_{rm} = t_{bm} + \frac{mt_{bm}}{2n-m} < t_m \tag{10}$$

$$I_{mLm} + \frac{(n-m)\,V_{dc}}{2nR} < I_m \tag{11}$$

which help to define the volume of L_m and estimate compensating time t_{bm}.

It should be noted that the maximum voltage of the anti-parallel diodes of switches $V_{\max d}$ is:

$$V_{\max d} = \frac{n+2}{2n\,(n+1)} V_{dc} \tag{12}$$

The current in inductors i_L passes through the diodes. Therefore, the maximum current of the diodes is I_{mL}, which is the maximum of i_L.

The control circuit of the upper n capacitors is shown in Fig. 10(e). It should be noted that i_{Lm} charges the capacitors $C_{(m+1)} - C_{n'}$. Hence the compensating time t_{b1} should be adjusted firstly. Then t_{b2} should be adjusted and so on.

It can be concluded that TWII can balance the capacitor voltages with two inductors and simplify control system. Furthermore, TWII can be easily extended to $(2n+1)$ level inverter where the reduction of extra components becomes more impressive. It should be noted that when the load is inductive, an auxiliary capacitor is needed to be inserted into the load to make it nearly resistive.

3. SIMULATION RESULTS

To show the performance of TWII, a simulation system shown in Fig. 2 is set up. Firstly, the parameters of the simulation system are determined as shown in Table 2 to verify the theoretical analysis.

Table 2. Parameters of simulation system.

Parameters	V_{dc}	C_1, C_2, C_3, C_4	L_1, L_2	f_{base}	R_{load}
Value	30 V	1 mf	1.1 mH	400 Hz	10 Ω

The simulation results are shown in Fig. 11. The output voltage is five-level without distortion, as shown in Fig. 11(a). According to Eq. (3), the theoretical value of compensating time t_b is 0.266 ms. The simulation result is 0.271 ms shown in Fig. 11(b), which agrees with the theoretical result within the allowable error range. According to Eq. (6), the theoretical value of I_{mL} is 1.84 A. The simulation result is 1.83 A, shown in Fig. 11(c), which is consistent with the theoretical result. Fig. 11(d) shows that the voltages of capacitors are balanced.

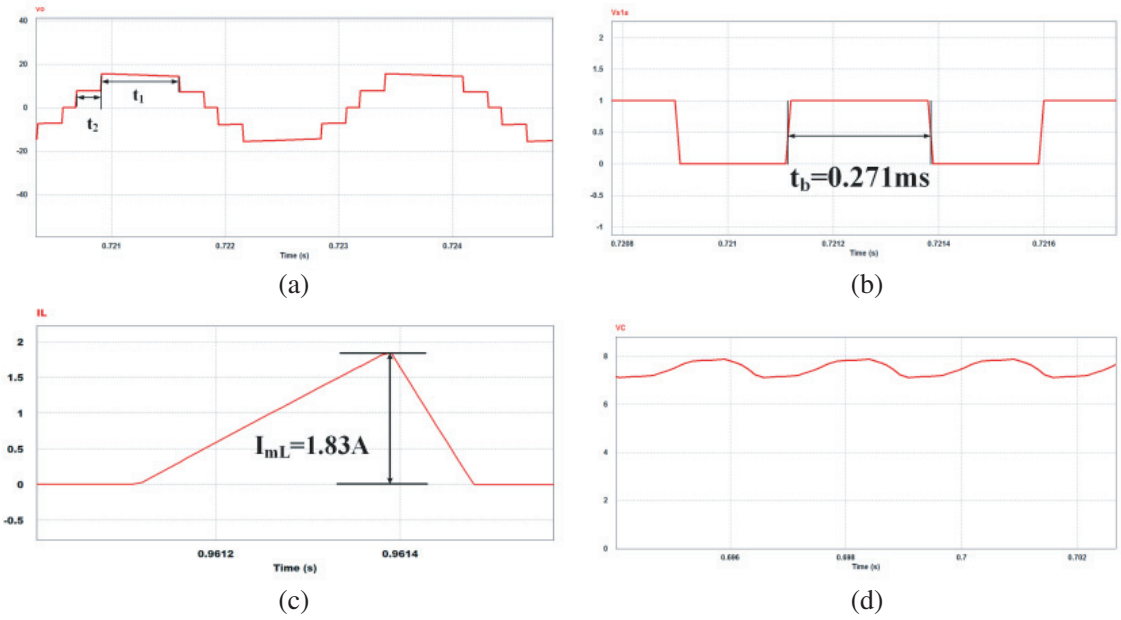


Figure 11. Simulation results. (a) Output five levels voltage. (b) Compensating time. (c) Compensating current. (d) Voltage of one capacitor.

Secondly, the inductive load is considered to show the load-carrying capacity of TWII. Now the parameters of the simulation system are redetermined in Table 3.

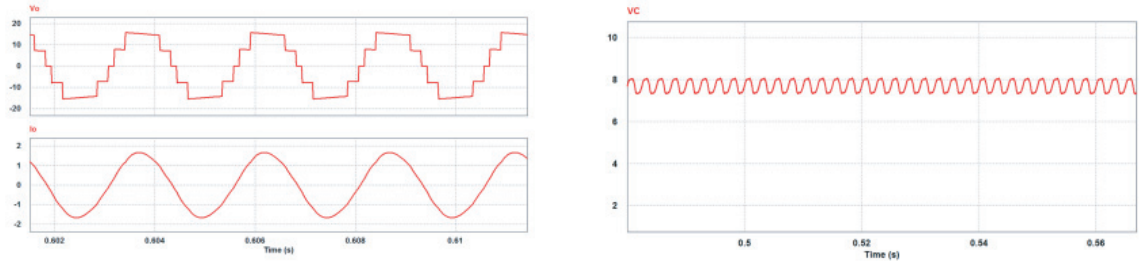
Figure 12(a) shows that the output voltage has five levels without distortion, and the load current is sinusoidal. Fig. 12(b) shows that the voltages of capacitors are balanced.

Table 3. Parameters of simulation system.

Parameters	V_{dc}	C_1, C_2, C_3, C_4	L_1, L_2	f_{base}	R_{load}	L_{load}	$C_{inserted}$
Value	30 V	1 mf	1.1 mH	400 Hz	10 Ω	5 mH	30 uf

Table 4. Parameters of simulation system.

Parameter	V_{dc}	C_1	C_2	C_3	C_4	L_1, L_2	f_{base}	R_{load}	L_{load}	$C_{inserted}$
Value	30 V	1.0 mf	1.3 mf	1.6 mf	2.0 mf	1.1 mH	400 Hz	10 Ω	5 mH	30 uf



(a) (b)

Figure 12. Simulation results. (a) Output voltage and load current. (b) Voltage of one capacitor.

Finally, in order to show the robustness of TWII, different DC-link capacitors are considered. Now the parameters of the simulation system are determined as in Table 4. Fig. 13 shows that the voltages of all capacitors are balanced even the volume and initial value are different.

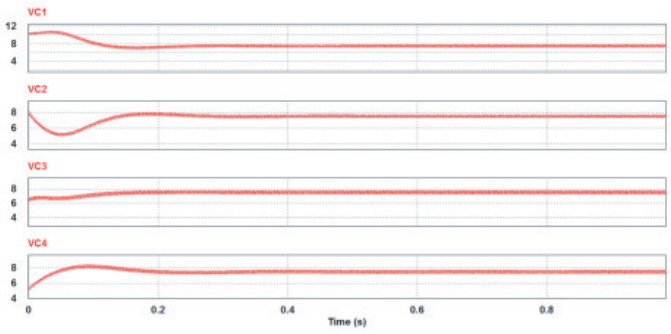


Figure 13. Voltage of four capacitors.

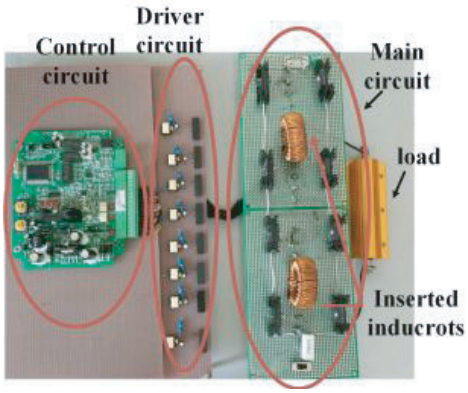


Figure 14. Photograph of prototype.

In summary, the simulation results verify that the theoretical analysis is valid, and TWII is robust enough to balance the voltage with any load, even when the capacitors are in different values.

4. EXPERIMENTAL RESULTS

To verify the effectiveness of TWII, the prototype of experimental system is built as shown in Fig. 14. To compare with the simulation results, the parameters of the system are determined as in Table 2. The experimental results are given as in Fig. 15.

The comparison of experimental and simulated results is shown in Table 5. It can be found that the experimental results are almost the same as that achieved by the simulation, which verifies the validity of TWII. The input voltage is $V_{dc} = 30$ V, and the RMS input current is $I_{in} = 0.38$ A. Correspondingly,

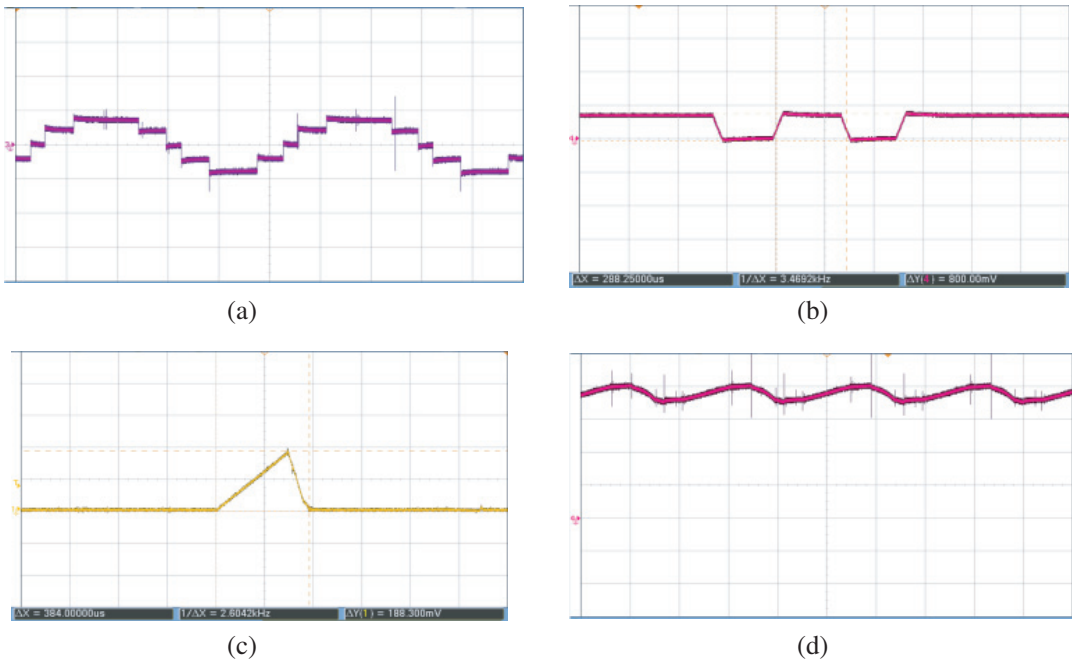


Figure 15. Experiment results. (a) Output five levels voltage of the inverter. (b) Compensating time. (c) Compensating current. (d) Voltage of one capacitor.

Table 5. Comparison of experiment and simulation results.

Parameter	Compensating time t_b	Peak of compensating current I_{mL}	Voltage fluctuation of DC-link capacitor
Simulation result	0.271 ms	1.83 A	0.4 V
Experimental result	0.288 ms	1.88 A	0.5 V

the RMS output voltage is $V_{out} = 10.2$ V, and the RMS output current is $I_{out} = 1.02$ A. As the load is a resistance, the efficiency is

$$\eta = \frac{V_{out} I_{out}}{V_{dc} I_{in}} = 91.26\% \tag{13}$$

The efficiency is not very high because of the small total power. But the efficiency will be improved as the total power increases.

5. CONCLUSIONS

In this paper, a new topology with inserted inductor for DC-link capacitor voltage balancing in the DCMLI is proposed. The topology used in five-level and $(2n + 1)$-level is introduced and compared with other methods to show its superiority. Besides, simulation and experimental test for TWII used in five-level inverter is presented. It can be seen that TWII can balance the voltage of capacitor with any load and that TWII is robust enough to sustain the difference of DC-link capacitors.

TWII needs an auxiliary capacitor when the load is inductive, but the extra components are greatly reduced. Compared with aforementioned methods, there are no extra drive circuits for extra switches. Therefore, the control circuit is efficiently simplified, and the electromagnetic interference is reduced. Of course, the efficiency is improved. On the other hand, the control strategy is just to adjust the duration of t_b. Therefore, the response of the topology is faster. With the inverter level increasing, these advantages become more extraordinary and have great commercial value.

ACKNOWLEDGMENT

This work is fully supported by the National Science and Technology Pillar Program During the 12th Five-Year Plan, project No. 2014BAF08B06.

REFERENCES

1. Franquelo, L. G., J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, Vol. 2, No. 2, 28–39, 2008.
2. Investigating R&D Committee of Current Statuses and Trends of General Purpose Inverter, "General purpose inverter: Current status of energy saving effect, performance improvement, and environmental harmonization," IEEJ Technical Report, No. 807, (in Japanese).
3. Sheng, L. J. and P. F. Zheng, "Multilevel converters a new breed of power converters," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 3, 509–517, 1996.
4. Yuan, X. M. and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Trans. Power Electron.*, Vol. 15, No. 4, 711–718, 2000.
5. Wang, H., J. Li, H. Li, K. Xiao, and H. Chen, "Experimental study and SPICE simulation of CMOS inverters latch-up effects due to high power microwave interference," *Progress In Electromagnetics Research*, Vol. 87, 313–330, 2008.
6. Hsu, C.-L. and J.-T. Kuo, "Microstrip realization of trisection synthesis with frequency-dependent admittance inverter," *Progress In Electromagnetics Research*, Vol. 113, 195–210, 2011.
7. Wu, Y.-D., C.-W. Kuo, S.-Y. Chen, and M.-H. Chen, "A general rule for designing multibranch high-order mode converter," *Progress In Electromagnetics Research*, Vol. 138, 327–336, 2013.
8. Guo, Y., L. Wang, and C. Liao, "Modeling and analysis of conducted electromagnetic interference in electric vehicle power supply system," *Progress In Electromagnetics Research*, Vol. 139, 193–209, 2013.
9. Guo, Y., L. Wang, and C. Liao, "Systematic analysis of conducted electromagnetic interferences for the electric drive system in electric vehicles," *Progress In Electromagnetics Research*, Vol. 134, 359–378, 2013.
10. Wang, H., M. Lu, Y. Deng, R. Zhao, and X. He, "Relationship between flying capacitor multilevel inverter PWM methods and switching loss minimized PWM method for flying capacitor multilevel inverter," *Proc. 2004 IEEE 35th Annual Power Electronics Specialists Conf., 2004 (PESC 04)*, Vol. 6, 4418–4422, June 2004.
11. Song, S. G., F. S. Kang, and S.-J. Park, "Cascaded multilevel inverter employing three-phase transformers and single DC input," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 6, 2005–2014, 2009.
12. Chen, A. and X. He, "Research on hybrid-clamped multilevel-inverter topologies," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 6, 1898–1907, 2006.
13. Rodriguez, J., J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, 724–738, 2002.
14. Han, Y., X. He, C. Tan, J. Cheng, and R. Zhao, "Multilevel circuit topologies based on the switched-capacitor converter and diode-clamped converter," *IEEE Trans. Power Electron.*, Vol. 26, No. 8, 2127–2136, 2011.
15. Peng, F. Z., J.-S. Lai, J. McKeever, and J. Van Coevering, "A multilevel voltage — source converter system with balanced DC voltages," *IEEE PESC Conf. Record*, 1144–1150, June 1995.
16. Shukla, A., A. Ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, 2249–2261, 2010.
17. Peng, F. Z., "A generalized multilevel inverter topology with self-voltage balancing," *IEEE Trans. Ind. Appl.*, Vol. 37, 611–618, 2001.
18. Gao, C., X. Jiang, Y. Li, Z. Chen, and J. Liu, "DC-link voltage self-balance method for a diode-clamped modular multilevel converter with minimum number of voltage sensors," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, 2125–2139, 2013.

19. Sano, K. and H. Fujita, "Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 6, 1768–1776, 2008.
20. Shoyama, M., T. Naka, and T. Ninomiya, "Resonant switched capacitor converter with high efficiency," *Proceedings of the 35th Annual IEEE Power Electronics Specialists Conference*, Vol. 5, 3780–3786, 2004.
21. Ito, T., M. Kamaga, and Y. Sato, "Operating characteristics of open-loop RSCC connected to diode-clamped multilevel inverter," *Proceedings of IEEJ Annual Meeting*, 4–043, 2009 (in Japanese).
22. Ajami, A., H. Shokri, and A. Mokhberdoran, "Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter," *IET Power Electron.*, Vol. 7, No. 3, 503–514, 2014.
23. Marchesoni, M. and P. Tenca, "Diode-clamped multilevel converters: A practical way to balance dc-link voltages," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, 752–765, 2002.
24. Lai, J. S. and F. Z. Peng, "Multilevel converters — A new breed of power converters," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 3, 509–517, 1996.
25. Newton, C. and M. Sumner, "Novel technique for maintaining balanced internal DC link voltages in diode clamped five-level inverters," *Proc. Institute of Electrical Engineering — Electric Power Applications*, Vol. 146, No. 3, 341–349, 1999.