Progress In Electromagnetics Research Letters, Vol. 64, 99–104, 2016

A Dual Band E-CRLH Frequency Multiplier with Two Multiplication Factors

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Abstract—A dual-band microstrip distributed multiplier with two multiplication factors based on the extended composite right- and left-handed (E-CRLH) transmission lines (TLs) is presented. Dual-band operation for distributed multiplier is achieved by three cells, and each cell consists of a transistor, microstrip TL and E-CRLH transmission line. The distributed multiplier exhibits two multiplication factors in two different frequencies: one multiplication factor in reverse direction and the other multiplication factor in forward direction. The excellent agreement between the proposed technique and measurement results confirms the accuracy and efficiency of the method.

1. INTRODUCTION

A nonlinear device is typically used for generating the desired frequency multiplier [1]. The nonlinear elements are Schottky varactor diode (passive frequency multiplier) or a transistor (active frequency multiplier). In low input levels, the distributed multiplier is a very good case for realizing active frequency multiplier, for the reason that the distributed multiplier exhibits wide frequency bandwidth [1]. In the last decade, several metamaterial (MTM) components have been introduced, and based on the unusual properties of the composite right/left-handed (CRLH) structures, many microwave circuits are presented [2].

In this contribution, we propose a dual-band distributed multiplier (DM) based on extended composite right/left-handed (E-CRLH) transmission lines. The concept of E-CRLH TL, introduced in [3] and extensively developed later, has proven particularly powerful for deep insight into and efficient design of metamaterial devices. In [4], the equations for designing quad-band E-CRLH TL are presented.

In this paper, we derive dual-band distributed multiplier (DM) with two multiplication factors based on E-CRLH transmission lines. The proposed DM can generate two different frequency multiplied signals at two different output ports, simultaneously.

2. DISTRIBUTED MULTIPLIER PRINCIPLES

In traditional distributed multiplier, the transistors as active devices are series (Fig. 1(a)). Also, gate and drain of the transistors are connected to the gate and drain microstrip lines, respectively. An input signal with frequency f_1 is applied to the input (port #1 in the gate line), and as the input signal travels down the gate line, each transistor is excited and transfers the signal with kf_1 frequency to the drain line. While the phase delays on the gate and drain lines are synchronized ($|k\beta_g l_g| = |\beta_d l_d|$, k is the multiplication factor), the drain current of each transistor will be added in phase [5].

Received 4 October 2016, Accepted 22 November 2016, Scheduled 12 December 2016

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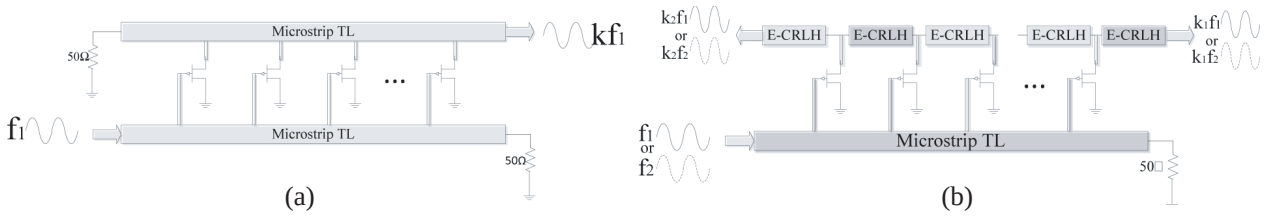


Figure 1. (a) Conventional distributed multiplier using MS TLs. (b) Proposed distributed multiplier using E-CRLH and MS TLs.

3. DUAL-BAND DISTRIBUTED MULTIPLIER DESIGN WITH E-CRLH TL

In our proposed dual-band DM, E-CRLH TLs and conventional microstrip TLs are used as drain and gate lines, respectively (Fig. 1(b)). In this dual-band DM, one side of the gate line is input port; two sides of the drain line are output ports; the other side of the gate line is isolated port (#4). This structure operates in two frequencies (f_1, f_2). If one tone signal with frequency f_1 (or f_2) is incoming to the input port, the signals with frequencies $3f_1(3f_2)$ and $4f_1(4f_2)$ are generated and come out from ports #2 and #3, respectively.

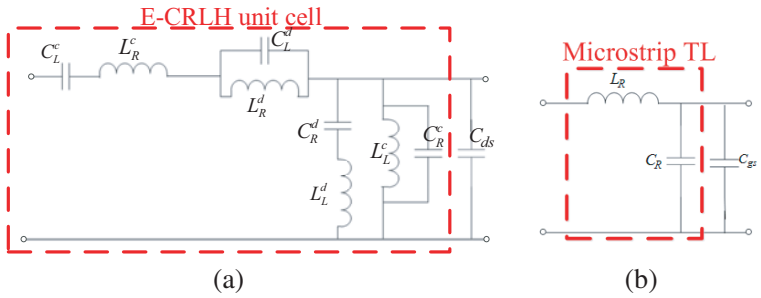


Figure 2. (a) E-CRLH unit cell and its equivalent circuit model. (b) Conventional microstrip TL equivalent circuit model.

Figure 2 shows the proposed unit cell of the E-CRLH in and its equivalent circuit model. In this figure, the capacitance (C_L^d) and inductance (L_R^d) of the series parallel resonance tank depend on the number of interdigital fingers and their gap widths, as well as its closed stub size, respectively. The capacitance (C_R^d) and inductance (L_L^d) of the shunt series resonance tank depend on the dimension of the rectangular patch and the conjoint stub, respectively. The inductance (L_L^c) depends on the stub with metallic via hole. The series inductance (L_R^c) and shunt capacitance (C_R^c) attribute to the inherent parasitic RH effect. Furthermore, C_L^c is the series capacitance of the interdigital capacitor. In Fig. 2, a parallel capacitance (C_{ds}) is added to the E-CRLH TL equivalent circuit model which is drain-source capacitance of transistor. Also, the gate-source capacitance is added to microstrip TL equivalent circuit model (Fig. 2). From Fig. 2, series impedance and parallel admittance of an E-CRLH unit cell can be derived as the following:

$$Z = j\omega L_R^c \left(1 - \frac{\omega_{cs}}{\omega^2}\right) - \frac{j}{\omega C_L^d \left(1 - \left(\frac{\omega_{dp}}{\omega^2}\right)\right)} \tag{1}$$

$$Y = j\omega (C_R^c + C_{ds}) \left(1 - \frac{\omega_{cp}}{\omega^2}\right) - \frac{j}{\omega L_L^d \left(1 - \left(\frac{\omega_{ds}}{\omega^2}\right)\right)} \tag{2}$$

where

$$\omega_{cs} = \frac{1}{\sqrt{L_R^c C_L^c}}, \quad \omega_{cp} = \frac{1}{\sqrt{L_L^c (C_R^c + C_{ds})}} \tag{3}$$

$$\omega_{dp} = \frac{1}{\sqrt{L_R^d C_L^d}}, \quad \omega_{ds} = \frac{1}{\sqrt{L_L^d C_R^d}} \tag{4}$$

and

$$\omega_{dscp} = \frac{1}{\sqrt{L_L^d C_R^c}}, \quad \omega_{csdp} = \frac{1}{\sqrt{L_R^c C_L^d}} \tag{5}$$

$$\omega_{dp} = \omega_{ds} = \omega_r, \quad \omega_{cp} = \omega_{cs}(balance\ conditions) \tag{6}$$

An E-CRLH TL is a periodic structure and can be constructed by cascading unit cells of Fig. 2. So, the Bloch propagation constant of the E-CRLH TL is equal to [6]:

$$\cos(\beta p) = 1 + ZY/2 \tag{7}$$

where p is the physical length of the unit cell. Such a component is therefore constituted of TL sections inducing equivalent phase shifts:

$$\phi_E(\omega) = \beta_E(\omega)\, p \tag{8}$$

where p is length of the E-CRLH cell. For designing a dual-band distributed multiplier with two multiplication factors according to the synchronization condition, we have:

$$\begin{cases} k_1\beta_g p = abs(\phi_E|_{k_1 f_1}) \\ k_2\beta_g p = abs(\phi_E|_{k_2 f_1} \\ k_1\beta_g p = abs(\phi_E|_{k_1 f_2}) \\ k_2\beta_g p = abs(\phi_E|_{k_2 f_2}) \end{cases} \tag{9}$$

where k_1 and k_2 are multiplication factors ($k_1 = 3$, $k_2 = 4$).

So, we must design a quad-band E-CRLH TL with conditions declared in Eq. (10). The E-CRLH TL can exhibit as a quad-band structure and eight equations for synthesis quad-band transmission line with E-CRLH cells are derived [4]. From these equations, lumped elements of Fig. 2 can be determined.

4. MEASUREMENT AND SIMULATION RESULTS

The proposed structure of the dual-band DM in this paper is fabricated on an RO4003 substrate with thickness 0.813 mm, loss tangent 0.01 and dielectric constant 3.38, as shown in Fig. 3. For simulating the proposed multiplier, Agilent Technologies Advanced Design System (ADS) is used, and full-wave simulation results are presented. Also, ATF36163 is used as an active device. The proposed dual-band distributed multiplier is biased at $V_{drain} = 0.6\,\mathrm{V}$ and $V_{gate} = V_{source} = 0\,\mathrm{V}$. The total drain current

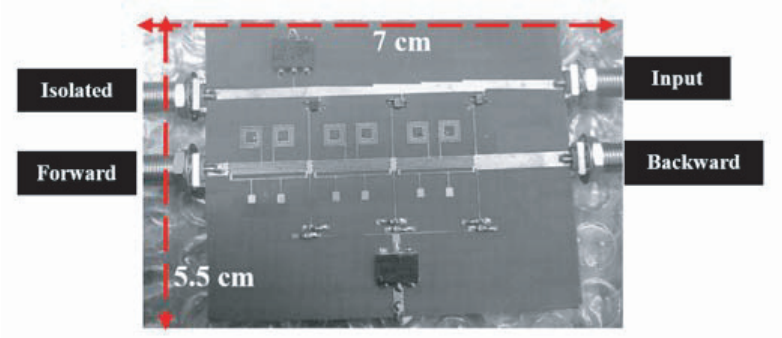


Figure 3. Fabricated prototype, of the proposed dual-band DM.

for three transistors is 45 mA. For DC bias, three lumped discrete capacitors (10 nF, 100 nF, 10 pF) for DC blocks in several points on board. Also, an RF chock chip (ADCH-80+) for RF blocks is utilized (Fig. 3).

The proposed DM is derived for below parameters:

$$\begin{cases} k_1 = 3 \\ k_2 = 4 \end{cases}, \quad \begin{cases} f_1 = 700 \sim 760\,\text{MHz} \\ f_2 = 1110 \sim 1160\,\text{MHz} \end{cases}$$

Now according to [4], we can derive eight lumped elements of the E-CRLH unit cell in Fig. 2 for above frequencies and multiplication factors.

C_R^c	L_L^c	L_L^d	C_R^d	L_R^c	C_L^c	C_L^d	L_R^d
4.1 pF	0.7 nH	5.3 nH	1.1 pF	10.3 nH	0.3 pF	2.1 pF	2.6 nH

Depending on the desired frequency bands, it is necessary to design the unit cell in consideration of HEMT gate capacitance (C_{gs}) and drain capacitance (C_{ds}). However, the values of these capacitances are very low (C_{gs} = 0.13 pF, C_{ds} = 0.05 pF), and for simplicity we can neglect them in design procedure. The absolute value of the dispersion curves of the proposed E-CRLH unit cell (theoretical and simulation) and conventional microstrip line is presented in Fig. 4. These two curves intersect each other at four points ($k_1 f_1$, $k_2 f_1$, $k_1 f_2$, $k_2 f_2$), and at these four points, synchronization condition is satisfied. At $k_1 f_1$ and $k_1 f_2$, the propagation constants of the E-CRLH TL are negative, and these signals come out from port #2 (backward direction). Also, at $k_2 f_1$ and $k_2 f_2$ the propagation constants of the E-CRLH TL are positive, and these signals come out from port #3 (forward direction). The

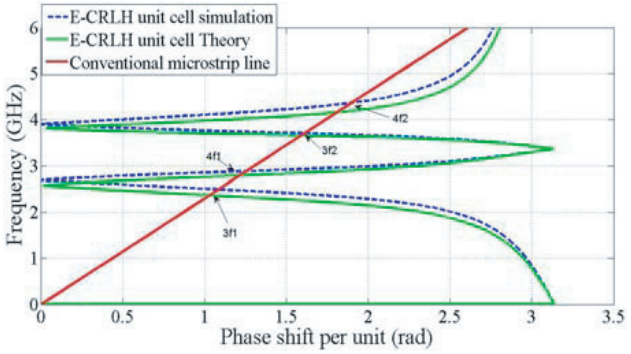


Figure 4. Dispersion curve of the E-CRLH unit cell (theory and full-wave simulation results) and conventional microstrip line.

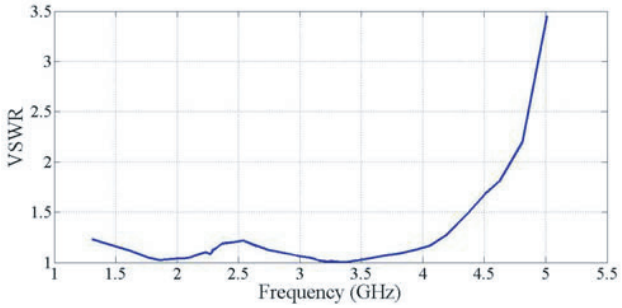
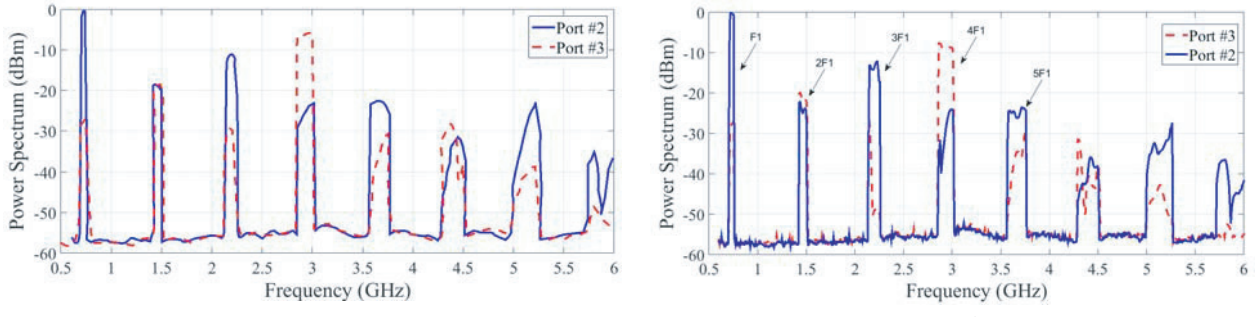


Figure 5. The measurement VSWR of the proposed DM.



(a) (b)

Figure 6. Output power spectrum of the proposed dual-band distributed multiplier shown in Fig. 2 at input frequency $f_1 = 700 \sim 760$ MHz. (a) Full-wave simulation results. (b) Measurement results.

measurement VSWR of the proposed DM is presented in Fig. 5. In the measurement procedure, first a signal generator is connected to the input port (port #1) and a spectrum analyzer to port #2, and we measure the spectrum of the output signal for two input frequency bands (f_1 and f_2). In this measurement process, the other ports (port #3 and port#4) are connected to a 50 Ω load. Then, we connect the spectrum analyzer to port #3 and measure the spectrum of the output signal while port #2 and port #4 are loaded with 50 Ω terminations.

The level of the input signals in two operation frequency bands is 0 dBm, and the measurement results show that the proposed dual-band distributed multiplier exhibits nearly 11 dB insertion loss in

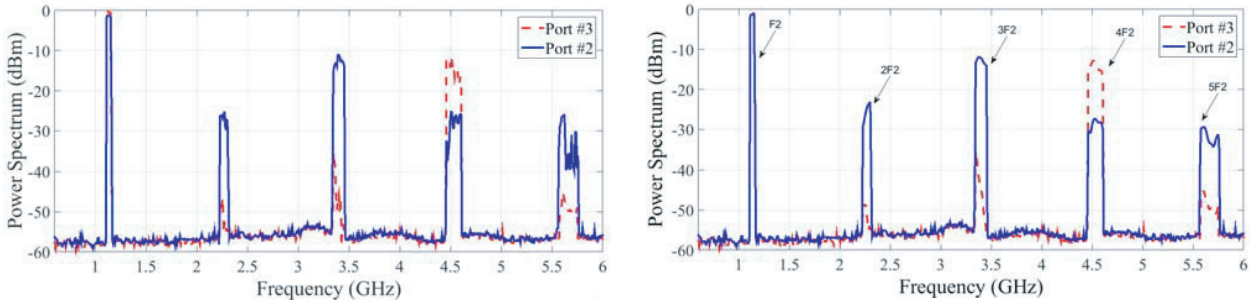


Figure 7. Output power spectrum of the proposed dual-band distributed multiplier shown in Fig. 2 at input frequency $f_2 = 1110 \sim 1160$ MHz. (a) full-wave simulation results. (b) Measurement results.

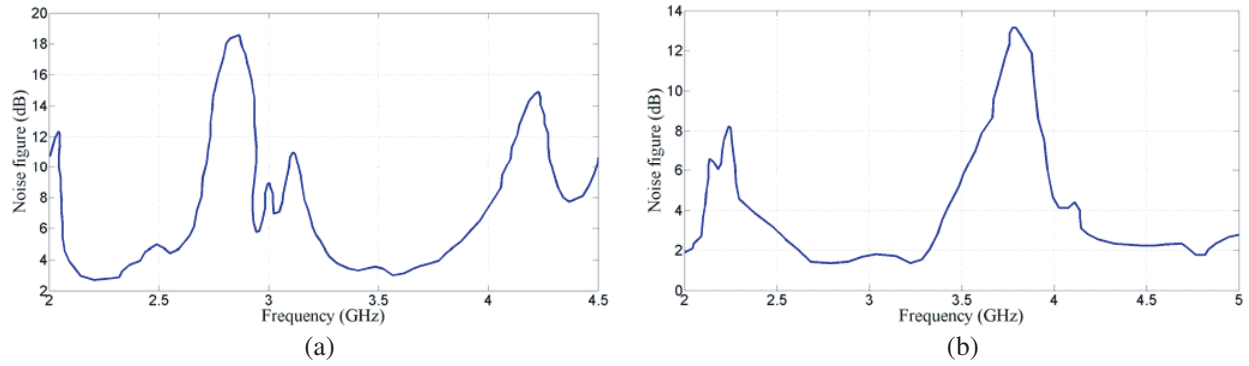


Figure 8. Measured noise figure versus output frequency in, (a) backward(port #2) and (b) forward (port #3), direction of the proposed dual-band DM.

Table 1. Comparison of the proposed dual-band multiplier with other works.

work	Design topology	Multiplication factor	Input frequency (GHz)	Input power (dBm)	Harmonic output (dBm)				
					F1	F2	F3	F4	F5
[7]	CRLH	3	1	0	−68	−59	−6	−67	---
[8]	Nonlinear CRLH	2	8 ∼ 21.5	20	7	7	−25	---	---
[9]	Diplexer based on CRLH	2	2	10	−41	−17	−47	−48	---
This work	E-CRLH	3 (port #2)	0.7 ∼ 0.76 and 1.11 ∼ 1.16	0	−1	−23	−12	−25	−26
		4 (port #3)			−2	−48	−36	−12	−47

the operation bands for each external port (Fig. 6 and Fig. 7). Because the proposed DM has two simultaneous outputs, the real value of the insertion loss is nearly 3 dB smaller than 11 dB and equal to 8 dB. The measured noise figure is also demonstrated in Fig. 8. It is less than 3.5 dB over output frequency bands 2100 $\sim$ 2280 MHz and 3330 $\sim$ 3480 MHz in backward direction (port #2), also less than 2.5 dB over output frequency bands 2800 $\sim$ 3040 MHz and 4440 $\sim$ 4640 MHz in forward direction (port #3). Table 1 lists the comparison of the proposed dual-band multiplier with other works.

5. CONCLUSION

A new compact dual-band distributed multiplier with two multiplication factors based on E-CRLH TLs isn presented in this paper. The proposed dual-band distributed multiplier is well suitable for microwave and millimeter-wave integrated circuits, local oscillator circuits and multi-band communication systems.

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