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A 2–4 GHz Octave Bandwidth GaN HEMT Power Amplifier with High Efficiency

Hao Guo, Chun-Qing Chen, Hao-Quan Wang, and Ming-Li Hao*

Abstract—In this paper, a broadband power amplifier with high efficiency and output power based on GaN HEMT is presented. The design of broadband matching network and transistor package modeling is presented, and a simulation strategy is proposed to increase the simulation accuracy. According to measured results, the PA module shows a linear gain of 10∼13 dB during 1.9–4 GHz. The efficiency can reach 74.5%, and the maximum output power reaches 33.2 Watt. For a 5-MHz WCDMA signal, the designed power amplifier achieves an average output power above 20 W when ACLR = −30 dBc over the entire working band.

1. INTRODUCTION

The number of frequency bands is increasing with the development of communication protocols. A broadband power amplifier which can cover different frequency bands is required to cut down hardware cost and make a communication system smaller. For some applications such as communication base stations and radar applications [1], the requirements of output power and efficiency are also very critical. GaN device is very suitable for these applications because of its high breakdown field, high electron saturation velocity, as well as high carrier density and mobility.

To achieve wide bandwidth, the traveling-wave amplifiers approach is a very popular technique [2–4], but too many devices used in circuit result in high cost, large size and low efficiency. For a single-device power amplifier, Class E [5], continuous Class F [6, 7], Class J [8] can achieve high efficiency over a wide band, while mostly the circuits design begins from packaged GaN HEMTs.

On the other hand, bare die is much cheaper and more flexible to use, which make it possible to put internal matching network and load more than one transistor in the package [9–11], while the package parasitics need to be taken into account in order to predict the performance at microwave frequencies. It is difficult to determine the package model from measurements because the internal ports are difficult to be accessed with probe tips. Therefore, the package model is extracted from 3-Delectromagnetic (EM) simulation [12]. The method to get the model of the transistor package from internal port to the outer edge can be found in [13], but they do not present the whole process for how to use the extracted model to design the power amplifier.

In this paper, a complete procedure to design a broadband power amplifier is presented, including the design of broadband matching network and transistor package modeling. Furthermore, a simulation strategy is proposed to increase the simulation accuracy

This paper is organized as follows. In Section 2, the design of a broadband matching network and PA topology is presented. The modeling of transistor package and the proposed simulation strategy are presented in Section 3, while the experimental results are shown in Section 4. Conclusions are then given in Section 5.

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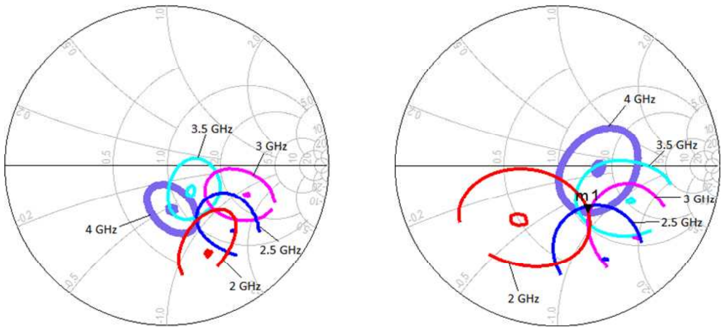
* Corresponding author: Ming-Li Hao (haomingli@ime.ac.cn).
The authors are with the Institute of Microelectronics of Chinese Academy of Sciences, Beijing Key Laboratory of Radio Frequency IC Technology for Next Generation Communications, Beijing 100029, China.

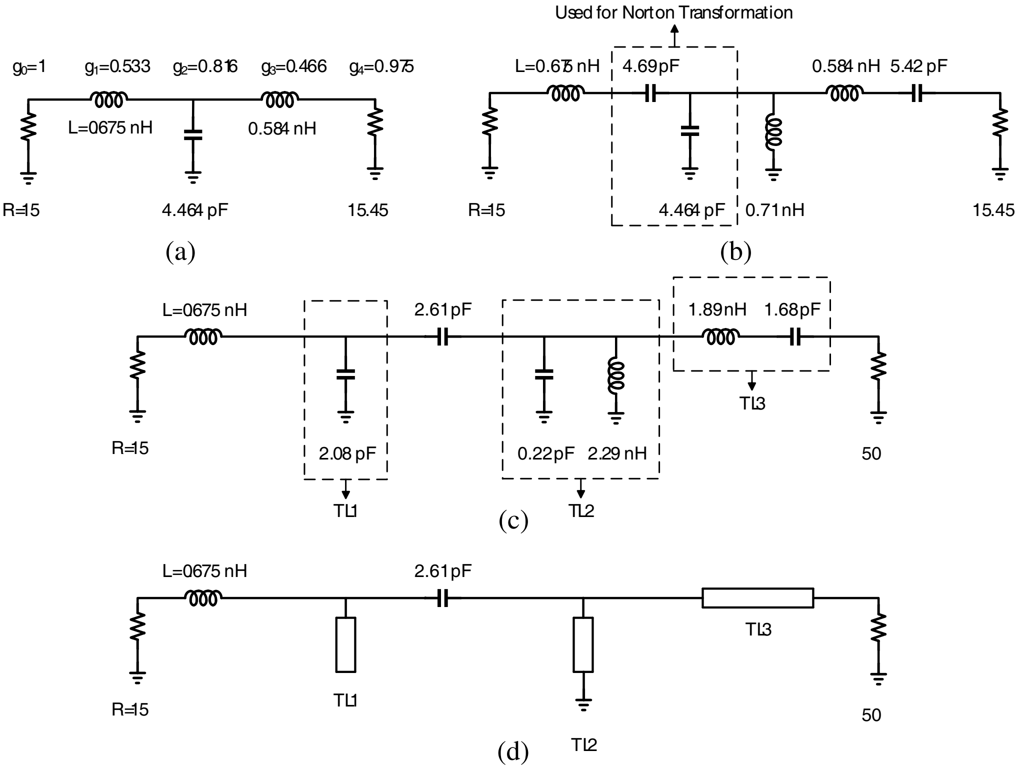
2. BROADBAND MATCHING NETWORK DESIGN

To design the broadband matching network, the first step is to find the optimum source and load impedances to make the transistor perform best in the working band. Load-pull/Source-pull simulation schematics are set up in ADS (Advanced Design System) while the large signal simulation model of the transistor is given by the factory, and the S-parameter of the package is obtained from HFSS (High Frequency Structure Simulator) which will be discussed in the next section. The simulation result is given in Figure 1.



(a) (b)

Figure 1. PAE and power contours at 2, 2.5, 3, 3.5 and 4 GHz, the characteristic impedance of the smith chart is 10 Ω. (a) Power contours of 44 dBm for load impedances. (b) PAE contours of 55% for load impedances.



(a) (b)

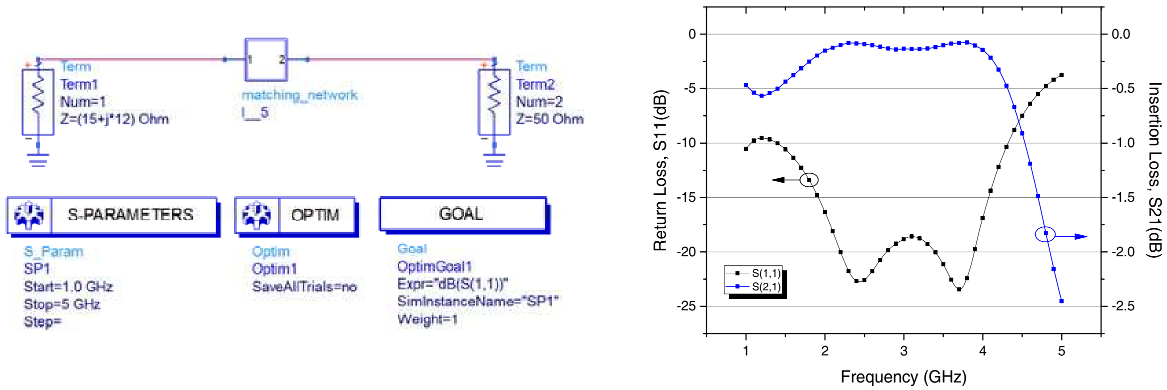
(c)

(d)

Figure 2. Design process of the broadband matching network. (a) Low-pass network. (b) Band-pass network. (c) Norton transformation is used to raise the load resistance to 50 Ω. (d) Corresponding distributed network.

Based on the simulation results, we have to choose the optimum impedance to design the broadband matching network. Taking the output power and efficiency during the whole working band into consideration, 15−j*12 is chosen as the optimum load impedance. The conjugate value of the optimum load impedance can be estimated by a resistance $R = 15\,\Omega$ in series with an inductor $L = 0.675\,\mathrm{nH}$. Therefore, the matching network should be designed to match R and L to $50\,\Omega$ across the 2–4 GHz working bandwidth. According to [14], a low-pass filter is first designed as shown in Figure 2(a). Then the low-pass network is transformed into a band-pass version by resonating each series or shunt element at the frequency of w_0, where $w_0 = \sqrt{w_1 * w_2}$, while w_1 and w_2 are the lower and upper band edge angular frequencies respectively as shown in Figure 2(b). After that, we have to scale the terminating resistor upwards to $50\,\Omega$, which is realized by a Norton transformation, as shown in Figure 2(c). Finally, the lumped LC network is transformed to distributed network shown in Figure 2(d), while the method can be found in [15].

However, the impedance of the R-L series cannot maintain 15+j*12 in the whole working bandwidth, so further optimization is needed. As shown in Figure 3(a), an automatic optimization is carried out in ADS to improve the matching between two ports, while the impedances of port1 and port2 are 15+j*12 and $50\,\Omega$, respectively. Figure 3(b) presents the final results of insertion loss and return loss.



Term1
Num=1
Z=(15+j*12) Ohm

matching_network
I__5

Term2
Num=2
Z=50 Ohm

S_Param
SP1
Start=1.0 GHz
Stop=5 GHz
Step=

Optim
Optim1
SaveAllTrials=no

Goal
OptimGoal1
Expr="dB(S(1,1))"
SimInstanceName="SP1"
Weight=1

(a) (b)

Figure 3. (a) Automatic optimization in ADS. (b) Insertion loss and return loss for the output matching network. The simulations use port1 and port2 impedances of 15+j*12 and $50\,\Omega$, respectively.

3. PACKAGE MODELING AND COMBINED SIMULATION STRATEGY

The final module looks like the model shown in Figure 4. The die is attached to the middle of the package, and bonding wires are employed to connect them. The PCB is fixed on the heat sink made in brass on both sides by screws first. Then the package is fixed on the groove in the middle of the heat sink by screws too, while the package leads fall on the pads on PCB.

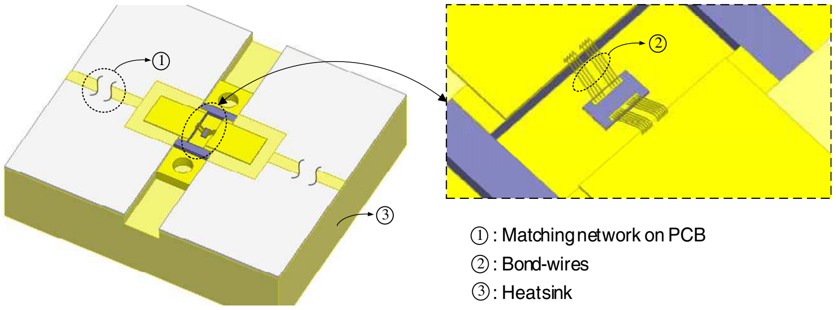


Figure 4. Model of the final module.

Figure 5 shows the overlook of the module. Region 3 means the matching network designed on PCB. Region 2 represents the pads on the PCB which connect the PCB with the transistor package leads. Region 1 represents the transistor package away from the PCB.

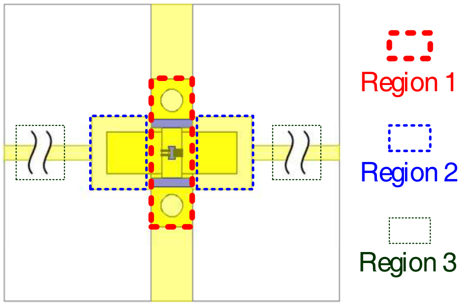


Figure 5. Overlook of the module.

Another model which just contains region 1 and the heat sink is set up in High Frequency Structure Simulator (HFSS) to extract the S-parameter from the inner port to the edge of the package. The method is given in [13]. Together with transistor large signal model, the S-parameter is then used for the source-pull and load-pull simulation, to get the optimum source and load impedance. This impedance is used for the broadband matching network design. Region 2 and region 3 are simulated in ADS, because they are both on the PCB. The final PA topology is shown in Figure 6.

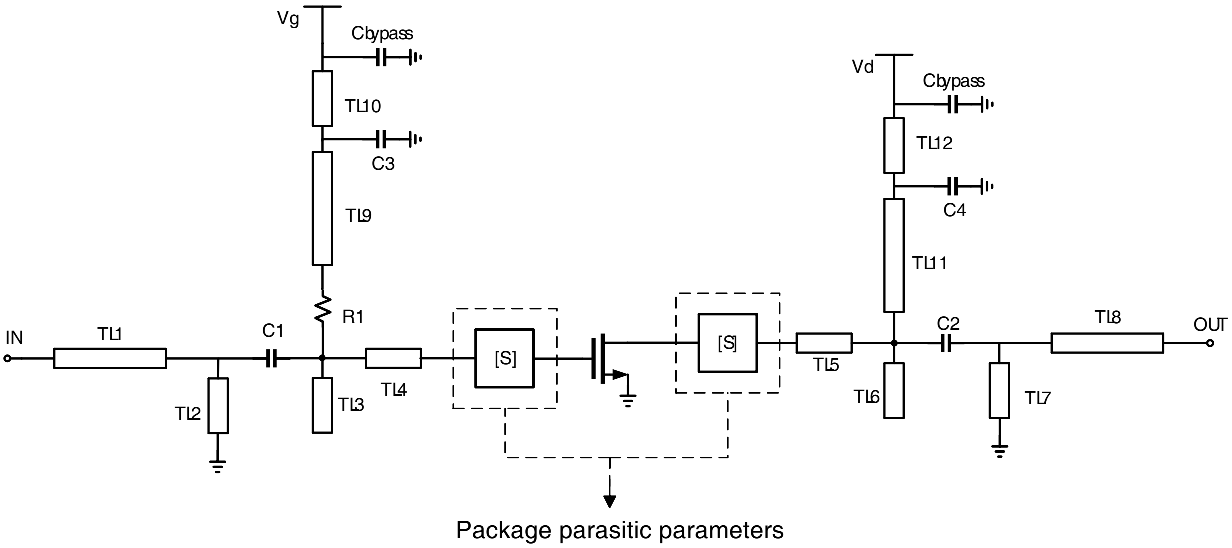
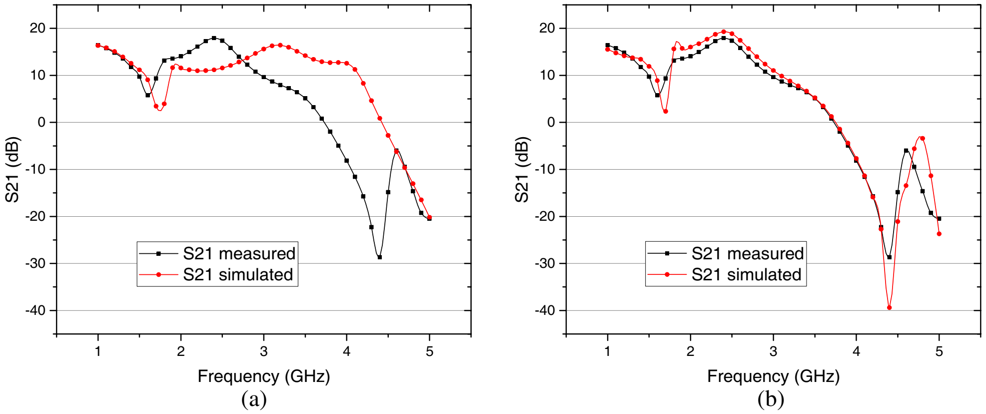


Figure 6. The topology of the designed PA.

The test result is shown in Figure 7(a), and it is not consistent with simulated results very well. It means that we have to adjust the original simulation strategy to increase the accuracy. The wrong management of region 2 is suspected to be the reason for the final inaccuracy. Though region 2 is on the PCB, it is at the edge, while the discontinuity and the complex electromagnetic field at the edge may introduce error.

A new simulation is taken, and region 2 is simulated in HFSS together with region 1 this time. As shown in Figure 7(b), new result shows that simulated result is consistent with the measured result very well, proving that the new simulation strategy is very effective. Then a new PA was designed and fabricated based on the proposed simulation strategy.



(a) (b)

Figure 7. (a) Comparison between measured and simulated results when region 2 is simulated in ADS. (b) Comparison between measured and simulated results when region 2 is simulated in HFSS.

4. MEASUREMENT RESULTS

The PA was implemented on a Rogers 4350 substrate with $\varepsilon_r = 3.66$ and thickness of 20 mil. Its size is $80 \times 60\,\text{mm}^2$. Figure 8 shows a photograph of the fabricated PA module using GaN HEMT device.

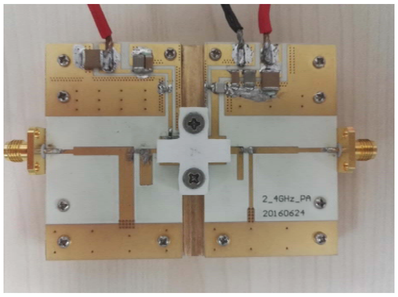
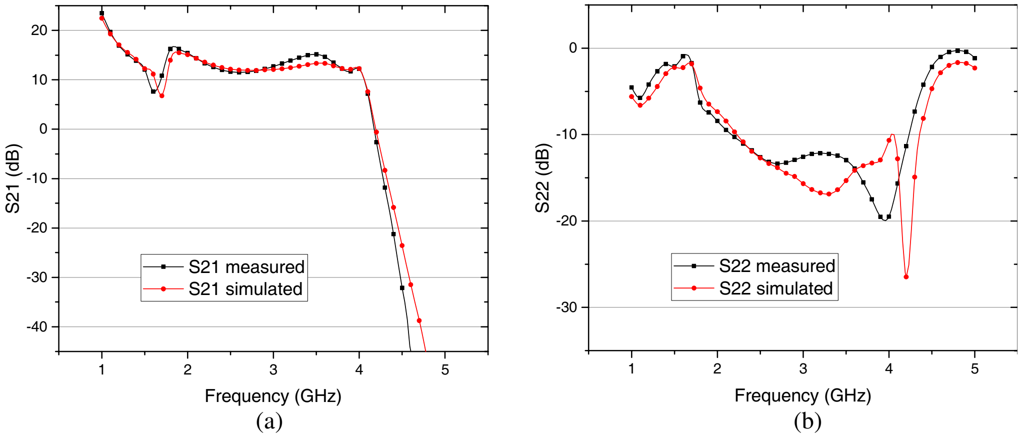


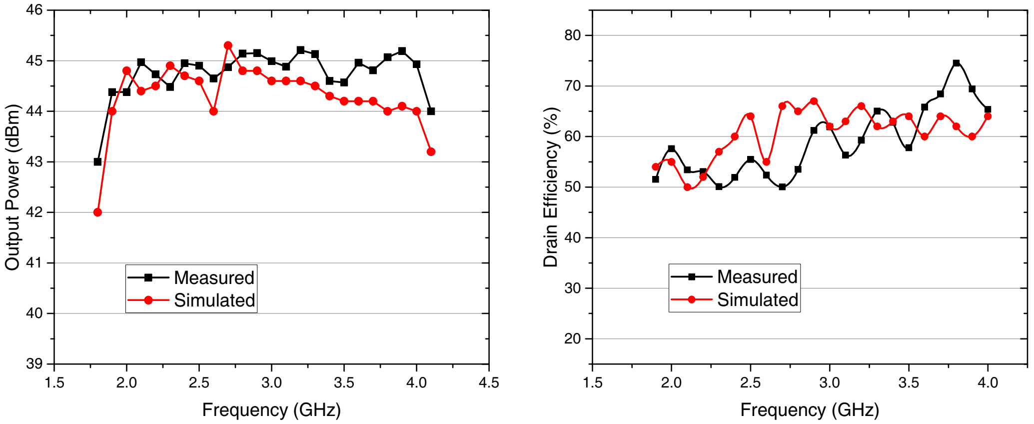
Figure 8. Photograph of the entire PA module.

Measurements were made using a continuous wave input signal generated by a microwave synthesized source (E4438C). A driver amplifier was used to boost the signal. The S-parameters were measured with an input power of -30 dBm and shown in Figure 9.



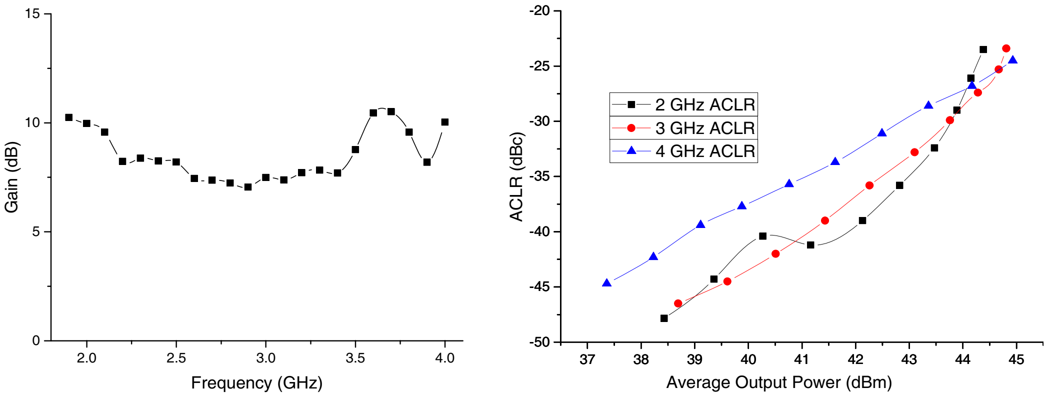
(a) (b)

Figure 9. Measured and simulated S-parameter.



(a) (b)

Figure 10. Measured and simulated output power and efficiency.



(a) (b)

Figure 11. Measured gain at maximum output power and ACLR at different frequencies with a 5-MHz WCDMA signal.

Table 1. State-of-the-art broadband PAs.

Reference	Bandwidth, GHz	Pout, W	Gain, dB	Drain Efficiency, %
2010 [16]	1.9–4.3	10–15	9–11	57–72
2012 [7]	1.3–3.3	10–11	10-13	63–89
2014 [17]	1.0–2.9	>8.5	10–13	>56.8
2015 [18]	0.9–2.8	>9.1	10–14	52–85
This work	1.9–4	27–33	7–10.5*	50–75

* Measured gain at maximum output power

In Figure 10, a reasonable agreement between simulation and measurement results is noted up to 3.5 GHz. At higher frequencies, a similar trend between measured and simulated results and the maximum disagreement, which is no more than 1 dB, can be seen.

Figure 11(a) presents the measured gain at maximum output power and shows a 3 dB compression compared to the small-signal gain. A single-carrier 5-MHz WCDMA signal with 6 dB peak-to-average ratio (PAR) was used to test the linearity performance of the power amplifier. Measurements were performed at three different frequencies of 2, 3 and 4 GHz, respectively. Figure 11(b) shows the measured adjacent channel leakage ratio (ACLR) results versus average output power, and the output power is still above 20 W when ACLR $= -30$ dBc.

A comparison of the recently published state-of-the-art broadband PA performances is shown in Table 1. The proposed PA presents excellent broadband characteristic while its efficiency performance is comparable with other state-of-the-art broadband PAs.

5. CONCLUSION

A complete procedure to design a broadband power amplifier is presented in this paper. It includes the design of broadband matching network, transistor package modeling and the proposed simulation strategy of ADS and HFSS combined simulation. A broadband power amplifier with high efficiency and output power based on GaN-HEMT is fabricated to demonstrate the proposed procedure. According to measured results, the small-signal gain is between 10–13 dB across 1.9–4 GHz. The output power is between 27.4 and 33.2 Watt with a drain efficiency of 50–74.5% while power gain is between 7–10.5 dB at maximum output power. Furthermore, the results show great agreement of simulated and measured results, which means that the approach is suitable for the design of wideband PAs, especially when the design starts from bare die.

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