Progress In Electromagnetics Research Letters, Vol. 63, 1–6, 2016

Fast Design Technique for Lumped-Element Multilayered Bandpass Filters

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Abstract—A fast design technique for lumped-element multilayered bandpass filters is proposed. With this technique, the difference between multilayered component values and theoretical component values can be quickly estimated and tuned. The design procedure for filters can be obviously simplified, and the efficiency can be improved. This technique is discussed in detail, and mathematic explanation is given. An example is used to show the entire design procedure. The measurement result agrees well with the desired result, which shows the effectiveness of proposed technique.

1. INTRODUCTION

Multilayered Bandpass Filters (BPFs) are widely used in wireless communication systems for its high performance, low cost and tiny size. However, the design procedure for lumped-element multilayer filter is always complicated because of the complicated structure, parasitic effects, and multiple tuning variables. To simplify the design procedure for filters, many techniques have been proposed. The space mapping technique proposed in [1] uses the efficient coarse model to simplify the design procedure for fine model. Based on this technique, many improvements were made, such as aggressive space mapping technique [2] and explicit knowledge embedded space mapping technique [3]. In [4], a design method based on hybrid electromagnetic (EM) model is proposed, which does not require formulas or equivalent models. The hybrid EM model is composed of multilayered components and ideal components. By introducing the ideal components, the efficiency of EM simulations can be improved obviously.

In this paper, a design technique for lumped-element multilayered BPFs is proposed to simplify the design procedures for filter. This technique is discussed in detail, and mathematic explanation is given. The proposed technique is based on the relationship between multilayered component values and port impedance. With this technique, the difference between multilayered component values and theoretical component values can be quickly estimated. Then multilayered components can be tuned with a clear target. The entire design procedure for filter is exhibited with an example. The measured result of experimental prototype agrees well with the circuit result, which shows the effectiveness of proposed technique.

2. DESIGN TECHNIQUE

The proposed technique is based on the relationship between multilayered component values and port impedance. It can be used to design single multilayered component and multilayered networks composed of capacitors and inductors in series. To show the proposed technique, an ideal filter [5] and a corresponding multilayered filter are taken as the examples (Fig. 1). The ideal filter is a third-order elliptic-function filter.

Received 29 July 2016, Accepted 19 September 2016, Scheduled 29 September 2016
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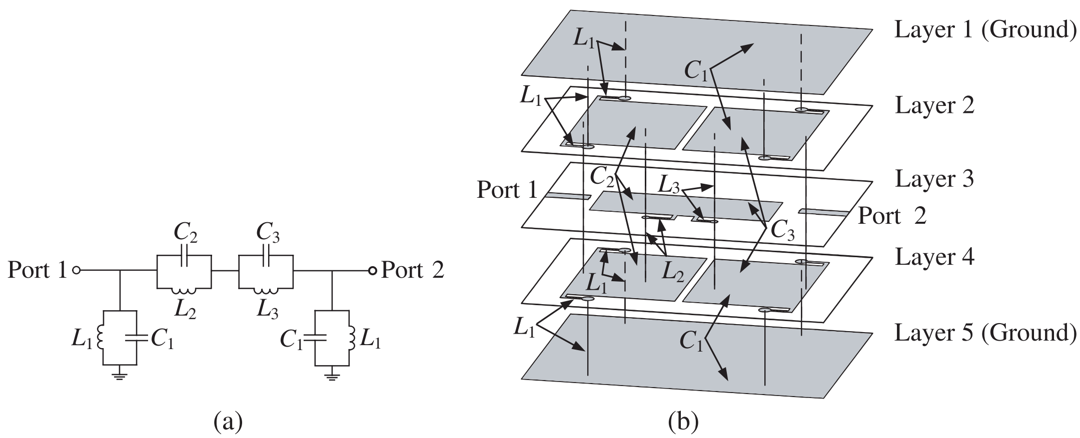


Figure 1. Example to show the proposed technique. (a) Ideal filter. (b) Multilayered filter layout.

According to the knowledge of microwave network [6], the $ABCD$ parameters of the ideal filter shown in Fig. 1(a) are

$$A_C = \frac{Y_1+Y_2}{Y_3+Y_4} + \frac{Y_1+Y_2}{Y_5+Y_6} + 1 \tag{1}$$

$$B_C = \frac{1}{Y_3+Y_4} + \frac{1}{Y_5+Y_6} \tag{2}$$

$$C_C = (Y_1+Y_2)\left(\frac{Y_1+Y_2}{Y_3+Y_4} + \frac{Y_1+Y_2}{Y_5+Y_6} + 2\right) \tag{3}$$

$$D_C = A_C \tag{4}$$

where Y_1 to Y_6 represent the admittance of L_1, C_1, L_2, C_2, L_3, and C_3, respectively. The S_{21} of this ideal filter is given by

$$S_{21C} = \frac{2}{A_C + B_C/Z_0 + C_C Z_0 + D_C} \tag{5}$$

where Z_0 is the port impedance, and its value is 50Ω.

Based on this ideal filter, a multilayered filter layout is designed and shown in Fig. 1(b). There are eight components in this multilayered filter, which makes the design and fine tunings very complex. To simplify the design procedure, we first define a factor k as

$$k = \frac{\text{admittance of multilayered component}}{\text{admittance of ideal component}} \tag{6}$$

Namely

$$\text{Multilayered capacitor value} = k \times \text{theoretical capacitor value} \tag{7}$$

$$\text{Multilayered inductor value} = \text{theoretical inductor value} \;/\; k \tag{8}$$

In this multilayered filter, we design all components with the same k. Because the multilayered component values are unknown, k is unknown. But it is possible to design them with the same k, which will be explained later. As a result, eight design variables degenerate to one, and the $ABCD$ parameters of this multilayered filter can be simplified as

$$A_M = A_C \tag{9}$$

$$B_M = B_C/k \tag{10}$$

$$C_M = kC_C \tag{11}$$

$$D_M = D_C \tag{12}$$

So the S_{21} of multilayered filter can be written as

$$S_{21M} = \frac{2}{A_M + B_M/Z_1 + C_M Z_1 + D_M} = \frac{2}{A_C + B_C/(kZ_1) + C_C(kZ_1) + D_C} \tag{13}$$

where Z_1 is the tuneable port impedance. A_C, B_C, C_C, and D_C are independent from multilayered components. They depend on filter circuit topology and theoretical component values.

According to Eq. (13), S_{21} of multilayered filter depends on the product of k and port impedance Z_1. Tuning k or Z_1 has the same influences on S_{21M}. This feature provides an easy way to design multilayered filter. k is difficult to tune because it is related to all multilayered component dimensions. But Z_1 is very easy to tune with EM simulation software, as the Ansys High Frequency Structure Simulator (HFSS). According to Eqs. (5) and (13), as long as we find a port impedance (noted as Z_{1b}) that makes

$$kZ_{1b} = Z_0 = 50\Omega \tag{14}$$

the value of k can be estimated by

$$k = \frac{Z_0}{Z_{1b}} = \frac{50\Omega}{Z_{1b}} \tag{15}$$

The desired Z_{1b} should make the response of multilayered filter agrees well with desired response, so we can try different port impedances with EM simulation software and choose the best one.

With the value of k, multilayered components can be tuned with a clear target. For example, if $Z_{1b} = 100\Omega$, we have $k = 0.5$. According to Eqs. (7) and (8), $k = 0.5$ means that every multilayered capacitor value is 50% of its theoretical value while every multilayered inductor value is 200% of its theoretical value. So we should double every multilayered capacitors and halve every multilayered inductor to get the desired response.

About the proposed technique, there are a few points worth mentioning.

To apply the proposed technique, it is necessary to keep the same k for every component in multilayered filter. Otherwise, the expression of S_{21} will be very complex, and the proposed technique fails. For multilayered capacitors, according to

$$C = \frac{\epsilon_0 \epsilon_r S}{d} \tag{16}$$

the ratio of multilayered capacitor values equals the ratio of their areas. As long as the ratio of their areas equals the ratio of their theoretical values, we may believe that they have the same k. According to Eqs. (6)–(8), k does not influence the resonant frequency of LC resonator. Therefore, for multilayered inductor that is part of LC resonator, we can tune it for desired resonant frequency. For inductor that is not part of LC resonator, we can design it with the proposed technique or with the method in [4].

In the previous discussion, we take S_{21} as the example to show the proposed technique. However, this technique is also valid for S_{11}. For example, the S_{11} of multilayered filter shown in Fig. 1(b) can be written as

$$S_{11M} = \frac{A_M + B_M/Z_1 - C_M Z_1 - D_M}{A_M + B_M/Z_1 + C_M Z_1 + D_M} = \frac{A_C + B_C/(kZ_1) - C_C(kZ_1) - D_C}{A_C + B_C/(kZ_1) + C_C(kZ_1) + D_C} \tag{17}$$

It can be observed that S_{11M} depends on the product of k and Z_1, too.

With the mathematical induction, it can be proved that the proposed technique can be used to design multilayered filters composed of reactance components in series, as the filter in [4, 7, 8]. With additional circuit transformation or steps, it can be used for more filters, as the filters in [9–12].

Figure 2 shows a flowchart of proposed technique. Because the port impedance is very easy to tune with EM simulation software, the design procedure can be significantly simplified. The complex tunings are not necessary. EM simulation software takes care of the parasitic effects, so the port impedance that we chose is the best for overall response.

3. DESIGN EXAMPLE AND DISCUSSION

An elliptic filter based on the circuit shown in Fig. 1(a) is designed, which operates at 800 MHz with 60 MHz 3 dB bandwidth. With the method given in [5], the theoretical component values are calculated. They are $C_1 = 48.1\,\text{pF}$, $C_2 = 22.85\,\text{pF}$, $C_3 = 19.67\,\text{pF}$, $L_1 = 0.823\,\text{nH}$, $L_2 = 2.01\,\text{nH}$, and $L_3 = 1.73\,\text{nH}$.

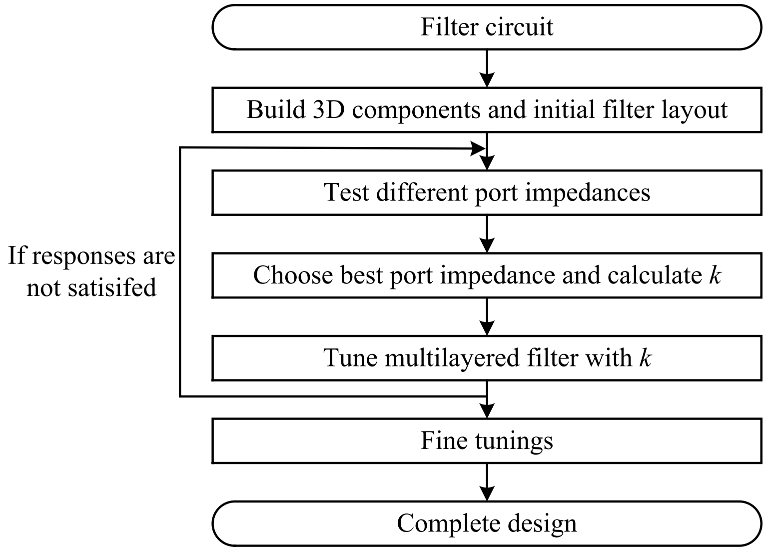
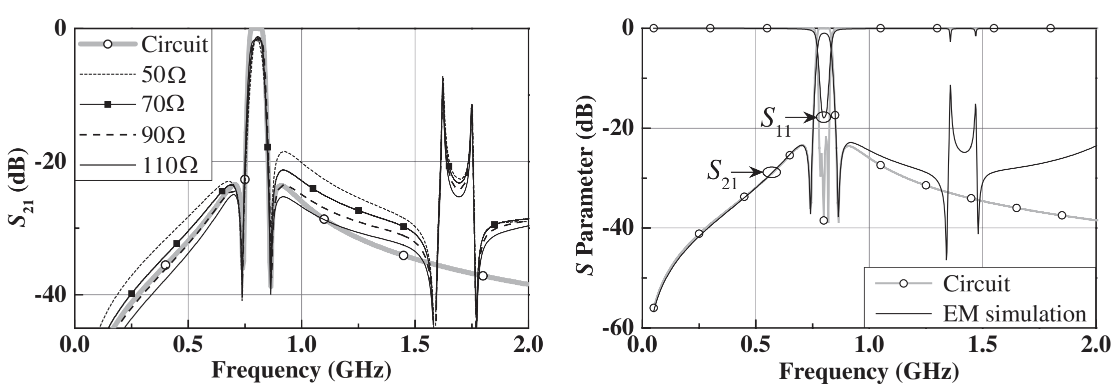


Figure 2. Flowchart of proposed technique.

Figure 1(b) shows the proposed physical layout. Due to the limitation of experimental conditions, we choose PCB technology for fabrication. The selected substrate is 1 mm-thickness Rogers 5880, of which the dielectric constant is 2.2. In the proposed layout, C_2 (C_3) is designed as a 3-metal-layer vertically-interdigitated-capacitor and placed at layers 2 to 4. C_1 is divided into two shunt capacitors and placed on the top and bottom of the layout, respectively. A via-hole is used to connect them. Inductors are composed of metal strips and via-holes. For L_2 (L_3), its metal strip is placed on layer 3. Its via-hole connects the metal strip and the electrode on layers 2 and 4. For L_1, because its value is relatively small, it is designed as four shunt sub-inductors. To keep the total inductance unchanged, the size of each sub-inductor has to be increased, which is good for fabrication.

According to the flowchart shown in Fig. 2, the first step is to build 3D components and initial layout. The initial area of C_1 is designed first with the method given in [4]. Based on the initial area of C_1, C_2 and C_3 are designed with the method in the last section to keep the same k. The initial area of C_1, C_2, and C_3 are $1000\,\text{mm}^2$, $475\,\text{mm}^2$, and $409\,\text{mm}^2$, respectively. Inductors are designed for the desired resonant frequencies. The EM simulation result of this initial filter is shown in Fig. 3(a) (terminated with 50Ω ports). Because the initial dimensions are not accurate, EM simulation result does not agree well with circuit result. The parasitic resonances at about 1.7 GHz are caused by the self-resonant of parallel resonant circuits.



(a) (b)

Figure 3. EM simulation results. (a) Different port impedances. (b) Final result.

The second step is to test different port impedances. Fig. 3(a) shows the EM simulation results when port impedances are 70Ω, 90Ω, and 110Ω.

The third step is to choose the best port impedance and calculate k. According to Fig. 3(a), when port impedance is 90Ω, the EM simulation result agrees well with the circuit result. Therefore, we choose 90Ω as the best port impedance and $k = 50/90 = 0.556$. This result means that every multilayered capacitor value is only about 55.6% of the theoretical value while every multilayered inductor value is about 180% of the theoretical value.

The fourth step is to tune the filter with k. The areas of C_1, C_2, and C_3 are increased to $1800\,\mathrm{mm}^2$, $854\,\mathrm{mm}^2$, and $735\,\mathrm{mm}^2$, respectively. Inductors are decreased to keep the resonant frequencies unchanged. No more tunings are performed. As shown in Fig. 3(b), the EM simulation result agrees well with the circuit result. Because C_1 is increased, the parasitic resonances decrease to about 1.4 GHz.

The last step is fine tunings. In this step, we fine tune the filter to meet the fabrication requirements.

In this example, only a few EM simulations are performed, and most of them are minor tunings. The target of each step is very clear. With the help of k, capacitors are directly tuned without EM simulations. As a result, almost half of the EM simulations are saved in component designs. In the tunings of filter, we treat all components as a whole rather than tuning them one by one. The complex tunings are obviously simplified. Compared to the space mapping technique [1–3], no equivalent circuits are used. Compared to the hybrid EM model in [4], the port impedance that we chose is the best for overall response.

4. EXPERIMENTAL RESULT

A prototype is fabricated using PCB technology. Its core size is about $4.3\,\mathrm{cm} \times 5.8\,\mathrm{cm} \times 0.4\,\mathrm{cm}$ or $5.86 \times 10^{-4}\lambda_g^3$. Fig. 4 shows the measurement and EM simulation results, which agree well with each other. The frequency shift may be caused by the stack error because all layers are manually stacked. The measured central frequency and 3 dB bandwidth are 822 MHz and 63 MHz, respectively. The designed central frequency and 3 dB bandwidth are 800 MHz and 60 MHz, respectively. The designed out-of-band suppression is about 24 dB while the measured result is about 23 dB. The very good agreement between desired response and measured response show the effectiveness of the proposed technique.

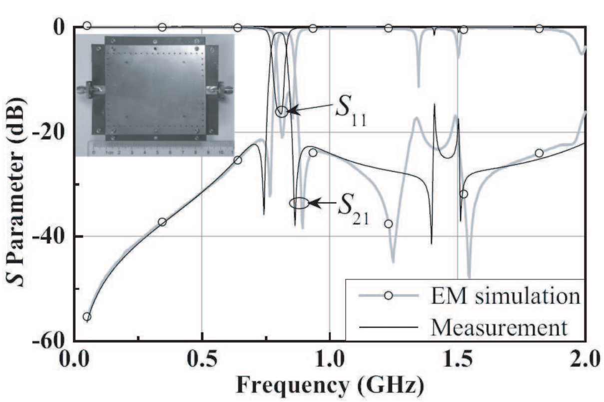


Figure 4. Measurement result and simulation result of the prototype.

5. CONCLUSION

A design technique for multilayered lumped-element BPFs is proposed. This technique is based on the relationship between multilayered component values and port impedance. By taking advantage of EM simulation software, the design procedure for this kind of filter can be simplified obviously with the proposed technique. Compared to previous technique, the proposed technique does not require equivalent model or hybrid model. These features make this technique easy to practice. A design example is used to demonstrate the whole design procedure. The measurement result agrees very well with the desired result, which verifies the effectiveness of the proposed technique.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China (NSFC) under Grant 61071020.

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