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Power-Combined Multipliers at 60 GHz Based on Fundamental Frequency Vector Modulation

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Abstract—High output power multiplier is necessary for local oscillator (LO) source of millimeter-wave and terahertz applications. However, single multiplier chip power-handling capability is limited by understandably low efficiency level and other technical constraints. Conventional in-phase power-combined structures are sensitive to the fabrication and assembly errors. In order to circumvent these limits, we propose a power-combined multiplier architecture at 60 GHz based on fundamental frequency vector modulation at 30 GHz. The fundamental vector modulator adjustment can compensate the phase deviation at the two doubler output ports despite fabrication and assembly tolerances. We can increase the output power by approximately 3 dB compared with single multiplier without sacrificing the bandwidth.

1. INTRODUCTION

High-power source plays an important role in millimeter and sub-millimeter and terahertz applications such as communication, imaging and radar systems. The recent advance in monolithic microwave integrated circuit (MMIC) amplifiers based on GaN transistors can provide several watts at W-band, one order of magnitude higher than the previous GaAs [1]. In order to increase the single-chip power handling capabilities, increasing the transistor areas, optimizing doping levels, employing high thermal conductivity substrates like diamond, and moving to GaN-based devices are adopted [2–5]. However, the output power of single-chip is ultimately constrained by physical size limit, thermal issues and substrate losses. Moreover, it is unrealistic to improve the capabilities in many applications that adopt the commercially available transistor or chip. The power-combined technology by combining multiple chips will be essential for further improving the power-handling capabilities without sacrificing the bandwidth and efficiency.

A variety of power-combined techniques have been reported at millimeter-wave(MMW) and terahertz frequencies [6–16]. Conventional binary networks based on planar transmission line suffer from high loss at very high frequency and are not suitable for MMW and terahertz. Spatial or Quasi-optical power-combined technique is another attractive approach, but relatively bulky systems are not suitable for a compact design [7, 8]. Since waveguide offers a low loss for signal conduction and simple configuration, many power-combined structures based on waveguide have been reported. Compact branch-line couplers or Y-junctions are used at both input and output of the single waveguide combiner block for power splitting and combining respectively and achieve excellent performance [9–11]. Dual-chip single-waveguide scheme can double the power-handling capabilities of multipliers without the necessity of duplicating the input and output matching networks [12, 13]. Compact waveguide-to-microstrip probe-array or waveguide-to-SIW transition structures are adopted to minimize the circuit size and provide the frequency coverage performance [14–16].

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However, the above power-combined topologies which are designed symmetrically are sensitive to fabrication and assembly errors which are unavoidable. The devices need to be electrically identical, and the alignment of the manually assembled device needs to be very accurate. Once fabrication and assembly errors occur, the power-combined efficiency will decrease, and it is impossible to repair. On-chip power-combined F-band frequency tripler using the superior accuracy of lithographic fabrication allows excellent power handling compared with traditional approaches without the need for combining several discrete chips [17]. However, such a method is highly dependent on the current lithographic fabrication technical level and is infeasible for the commercially available chip. In order to circumvent these limits, we present a power-combined multiplier architecture based on input fundamental frequency vector modulation despite fabrication and assembly tolerances. The adopted fundamental vector modulator can achieve a low-loss typical 12 dB and 360° phase shift at Ka-band [18, 19]. A novel five-port waveguide power combiner can obtain excellent consistence between two output ports [20]. The phase deviation of the doubler output ports can be compensated by the input vector modulation phase shift adjustment. To verify our scheme, we design, fabricate, measure a power-combined doubler at 60 GHz based on fundamental frequency vector modulation at 30 GHz. Results show that the proposed scheme can enhance the power-handling capabilities by approximately a factor of two compared with single doubler despite fabrication and assembly tolerances. Since the adopted doubler is MMIC utilizing GaAs pseudomorphic high electron mobility transistor (pHEMT) technology designed by our lab, the proposed power-combined multipliers cannot achieve the state-of-the-art output power and is mainly used to prove the feasibility of the concept.

2. POWER-COMBINED DOUBLER BASED ON FUNDAMENTAL FREQUENCY VECTOR MODULATION

The proposed power-combined scheme is depicted in Fig. 1. It consists of two mirror fundamental frequency vector modulators (VM), followed by Ka-band driver amplifiers (DA) and V-band doublers symmetrically placed along the center line, and a novel five-port waveguide power combiner to combine the doubler output. Φ_{VM1} and Φ_{VM2} mean the phase after $VM1$ and $VM2$ modulation, which are controlled by the bias control voltages V_I and V_Q. $\Delta\Phi_{VM}$ is the phase difference between Φ_{VM1} and Φ_{VM2}. Φ_{D1} and Φ_{D2} are the phases at the two doublers output ports. $\Delta\Phi_D$ is the phase difference between the two doublers output ports. P_{D1} and P_{D2} are the output powers of the two doublers. Ideally, ignoring the loss of the combiner block and phase deviation, the power-combined output power should be $P_{D1} + P_{D2}$. However, amplitude and phase consistency errors at two symmetrical doubler modules caused by electrical asymmetries such as the inherent difference of the discrete chip, the inconformity of gold wire bonding area, length, height will lead to that $\Delta\Phi_D$ deviates from 0°. A 1 mm electrical length difference between the two doublers will lead to 72° phase difference at 60 GHz and obviously decrease the power-handling capabilities. By adjusting the bias voltage V_I and V_Q of the input fundamental VM, we can finally correct the doubler output signals $\Delta\Phi_D$ deviation error, thus maximize the power-handling capabilities. Notably, the fundamental frequency Ka-band VM and DA design and implementation are easier and more efficient than the V-band counterparts. In addition, the fundamental vector modulation can be used to feed into other multiplier and extended to higher frequency.

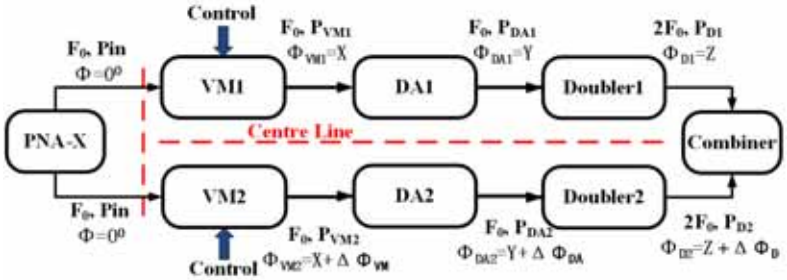

Figure 1. The scheme of proposed power-combined multipliers based on fundamental frequency vector modulation.

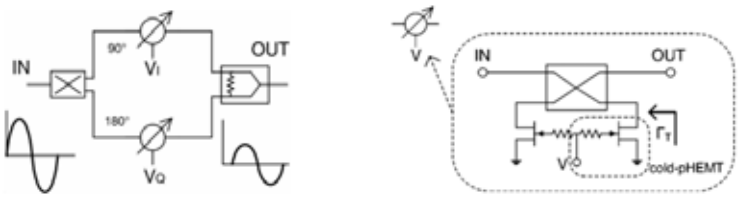

Figure 2. The schematic diagram of the vector modulator.

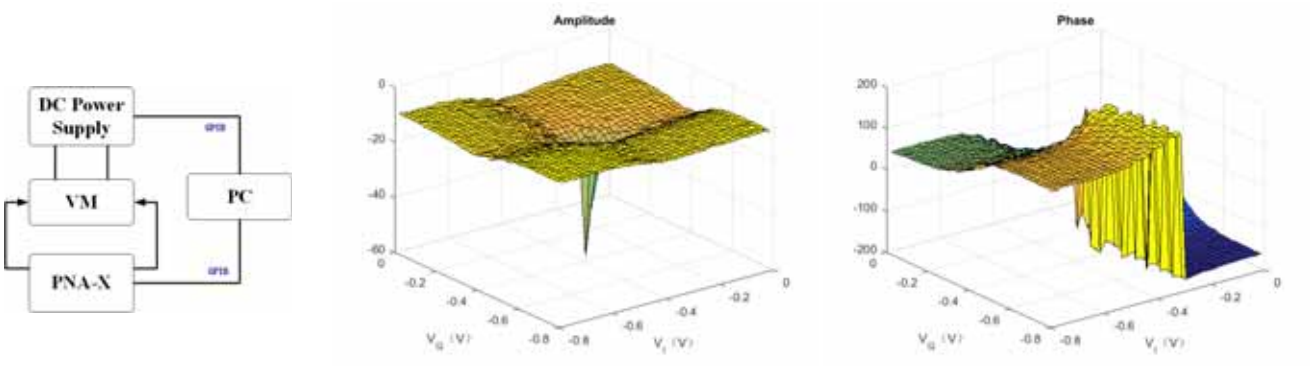

Figure 3. The measured setup and measured amplitude and phase versus V_Q and V_I of the vector modulator at 30 GHz.

2.1. Vector Modulator

Figure 2 shows the schematic and principles of the vector modulator presented. The input signal is split into two orthogonal portions: in-phase and quadrature-phase. These two portions are attenuated by two bi-phase amplitude modulators, which are controlled by two bias voltages V_I and V_Q. Combining these two modulated portions with a Wilkinson coupler completes the modulating function. The bi-phase amplitude modulator of the VM is based on a reflection type topology. This topology employs a 3-dB Lange coupler and a pair of cold-pHEMT terminations. The Lange coupler splits the input signal equally between direct and coupled ports with 90-degree phase shift. When two orthogonal portions are reflected back to the coupler, they are canceled at the input port and reduplicated at the isolated port. As the resistance of the termination controlled by bias voltage varies from low to high, signals are reflected with different attenuations. Γ_T is the reflection coefficient of the cold-pHEMT termination. Assume that the input is amplitude normalized signal with the frequency of f, the output voltage A_{com} can be derived as

$$A_{com} = \frac{1}{\sqrt{2}} \times \frac{1}{\sqrt{2}} \left(S_{I21} + jS_{Q21}\right) e^{j(2\pi ft+\varphi)} \tag{1}$$

where $1/\sqrt{2}$ is the constant coefficient induced by the Lange coupler; S_{I21} and S_{Q21} are the transmission coefficients of the bi-phase amplitude modulators, respectively; φ is the additional constant phase shift. The insertion loss IL and phase shift θ of the vector modulator can be obtained as follows

$$IL = -6 + 20\log\left|\sqrt{|S_{I21}|^2 + |S_{Q21}|^2}\right| \tag{2}$$

$$\theta = \varphi + \arctan\frac{S_{Q21}}{S_{I21}} \tag{3}$$

The adopted Ka-band VM MMIC is designed by our lab utilizing the GaAs pHEMT technology. The block diagram of the automatic measurement system for the VM and the measured results are shown in Fig. 3. The DC power supply provides the bias voltages V_I and V_Q of VM sweep from -0.8 to 0 V, in a step of 20 mV. PNA-X N5245A synchronously acquires the amplitude and phase of the VM module.

The DC power supply and PNA-X are controlled by PC automatic measurement software using the GPIB cables. Accurate S-parameters calibration is implemented before the automatic measurement and guarantees the reliability of the measurement results. The measured results show that the presented VM module can achieve a low-loss typical 12 dB, about 20 dB dynamic amplitude attenuation and 360° phase shift at 30 GHz. The performance of the proposed VM shows that it is adequate for our fundamental frequency amplitude and phase modulation. We can achieve the corresponding amplitude attenuation and phase shift characteristics simultaneously at bias voltage V_I and V_Q over 28–32 GHz.

2.2. Five-Port Waveguide Power Divider/Combiner

The configuration of the novel five-port power divider/combiner is shown in Fig. 4 and Fig. 5. The whole structure is composed of three sections along the propagation axis: Region I-input terminal, region II-coupling region and region III-output terminal. At the input terminal, there are three adjacent waveguides: one is used to input power, and the others are used to improve the isolation between two output ports. There are two adjacent waveguides to output power at the output terminal. In the coupling region, only one waveguide with H-plane steps is needed. The proposed five-port power dividier/combiner can realize high isolation, low Voltage StandingWave Ratio (VSWR), excellent insertion loss, small amplitude and phase error between two output ports without adding the cost and difficulty of fabrication, extra assembly elements or any other craft. Conventional dividers/combiners such as E-plane bifurcated waveguide, Magic-T, T-junction, Riblet coupler and substrate integrated waveguide have their disadvantages in different aspects in the practical application. The E-plane bifurcated waveguide must need a resistive film placed inside the bifurcated waveguide to realize the isolation between two output ports, which increases the cost of the product and the complexity of the assembly. Magic-T is a three-dimensional structure, which increases the difficulty of fabrication, especially when more than one such devices are integrated into a network. The T-junction has no isolation between two output ports. Although the Riblet coupler can provide a high isolation between two output ports in a certain bandwidth, it has intrinsically 90 degrees out-of-phase between two output ports. It is difficult to be compensated in a relatively wide bandwidth and the compensating circuits add to the overall size of the device. The power capacity of the substrate integrated waveguide power divider cannot be compared with the waveguide power divider, and its insertion loss is higher than the waveguide power divider.

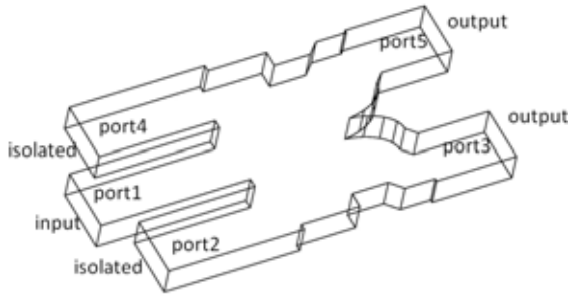

Figure 4. The simulation model of proposed power divider/combiner.

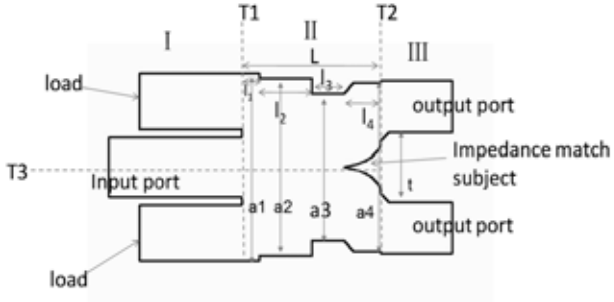

Figure 5. The flat-screen graphic of proposed power divider/combiner.

The structure of this power divider/combiner shows a full-height slot in the common narrow-wall between adjacent waveguides in region II. To achieve high isolation, low VSWR, excellent insertion loss and broad bandwidth, H-plane steps and bifurcation impedance match subject in region II are applied to achieve impedance match. The number of steps and the parameters of every step and bifurcation are analyzed and optimized by commercial software-CST's Microwave Studio.

A four-step power divider/combiner at V-band is designed, and the presented novel five-port waveguide divider/combiner shows that simulated insertion loss is lower than 0.1 dB and reflection of input port better than 20 dB from 55 to 65 GHz in Fig. 6. Amplitude imbalance and phase difference

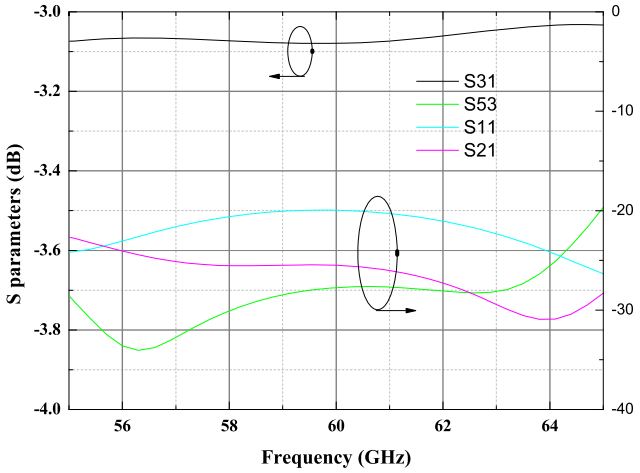

Figure 6. The simulated S-parameters of proposed power divider/combiner.

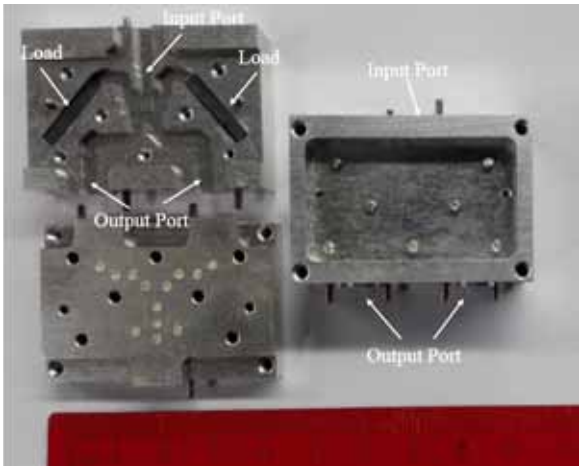

Figure 7. The presented novel five-port waveguide power divider/combiner photograph.

between two output ports is zero due to the symmetry of the proposed structure design. Fig. 7 shows the split portion on the left and the overview on the right of the waveguide power divider/combiner.

2.3. Fabrication and Assembly

The single multiplier module fabricates the GaAs pHMET MMIC doubler at V-band designed by lab which provides 0 dBm typical output power when driven by a +10 dBm signal. Fig. 8 shows the simulated model and S-parameters of the low-loss bent waveguide-to-microstrip probe transition based on 0.127 mm quartz substrate at the doubler output waveguide port. A high impedance line is used to achieve the broadband matching of the probe impedance to 50-ohm microstrip line. The optimized simulated insertion loss is less than 0.2 dB, and the return loss is better than 17 dB over 50–75 GHz.

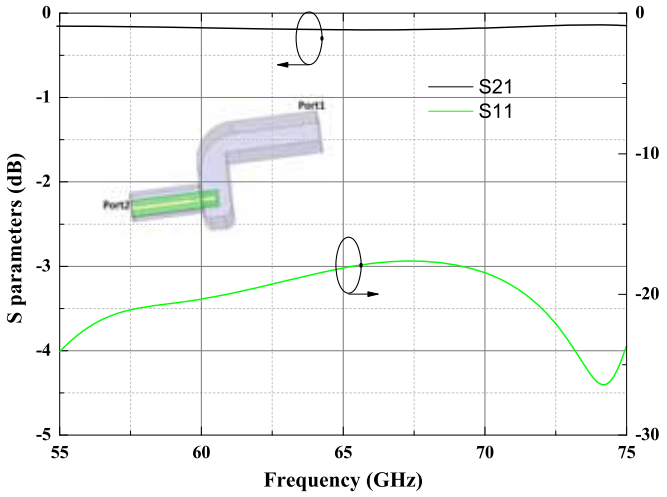

Figure 8. The simulated model and S-parameters of proposed V-band probe transition structure.

The two VM, DA and doubler modules are assembled symmetrically along the center line of the novel five-port waveguide power combiner as shown in Fig. 9. The VMs provide controlled amplitude attenuation and phase shift at the fundamental frequency. The modulated fundamental signal is amplified by DA and fed into the V-band doubler, and the doubler output signals are finally combined at the five-port waveguide combiner block.

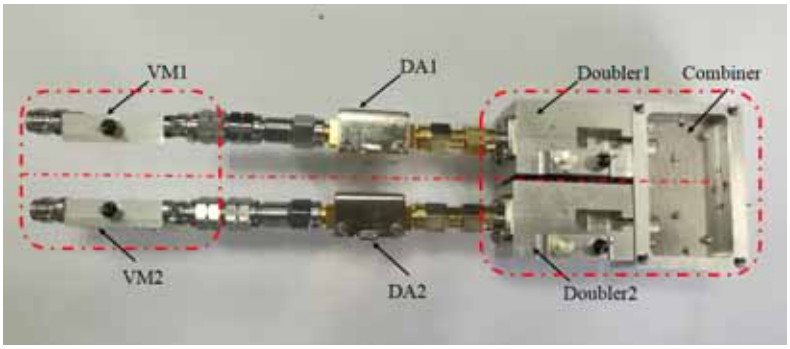

Figure 9. The assembly photograph consisting of two VMs, DAs and doublers symmetrically placed along the novel waveguide power combiner, coaxial connectors.

3. MEASUREMENTS

The two in-phase input fundamental frequency signals provided by the Keysight PNA-X are modulated by two VMs, amplified by the following two Ka-band DAs. The proposed VM has a maximum input power less than +15 dBm and a typical 12 dB, about 20 dB dynamic amplitude attenuation. The driver amplifier employs a commercially available MMIC chip CHA3396-QDG which produces 22 dB gain for +19 dBm output power at 1 dB compression, fabricated by UMS, Inc. Fig. 10(a) shows the setup of the input modulated and amplified signal output power calibration (red arrows) and phase difference test (black arrows). A constant +10 dBm P_{DA1} and P_{DA2} for doubler input is achieved by the adjustment of the bias voltages V_I and V_Q at the VM1 and VM2, and monitored using Keysight 8487A power sensor and N1912A power meter at P_{in} = 10 dBm. The corresponding phase difference $\Delta\Phi_{DA}$ between the DAs is tested and recorded by the Keysight Oscillator DSO-X 93204A whose sampling rate is up to 80 GSa/s.

The modulated and amplified fundamental signals are fed into the V-band doublers. The fundamental and 3rd isolations of the adopted doubler MMIC are 15 dBc and 25 dBc, respectively, with respect to the desired 2nd output signal level from 56 to 62 GHz. Moreover, the fundamental frequency is below the cut-off frequency of WR-15 waveguide. High suppression of undesired harmonics can be achieved, and the desired 2nd output power of the single doubler can be measured using the Keysight WR-15 V8486A power sensor and N1912A power meter (red arrows). The output power of the waveguide combiner block is also measured using the same method mentioned above (black arrows) as shown in Fig. 10(b).

Figure 11 shows the power-combined output power at 60 GHz versus the phase difference $\Delta\Phi_{DA}$ of the modulated and amplified input fundamental signal between the DAs at 30 GHz. The corresponding two doublers output power is −1.27 dBm and −0.97 dBm, respectively. Ideally when the phase difference is 0°, the maximum output power 1.94 dBm is achieved without consideration of the power-combined loss. However, the corresponding measured output power is only −2.1 dBm due to the phase deviation at the power-combined input port caused by fabrication and assembly errors. When the phase difference $\Delta\Phi_{DA}$ is 38° or 218°, we can achieve the maximum output power 1.45 dBm. The power-combined loss is 0.44 dB, which corresponds to a power combining efficiency higher than 91%. When the phase difference $\Delta\Phi_{DA}$ deviates from above optimum values, the output power decreases obviously. When the phase difference is 128° or 308°, the minimum output power means that the phases at the two doublers output ports are contrary, and the power cancels out. Notably, the optimum and worst power-combined points occur every 90° and have a 180° period due to the adopted doubler structure.

Similarly, Fig. 12 shows the power-combined output power at 62 GHz versus the phase difference $\Delta\Phi_{DA}$ between the DAs at 31 GHz. The maximum output power 3.5 dBm is achieved when the phase difference is 36° or 216°, and the phase difference 126° or 306° results in the minimum power output. In comparison, the two doublers can only achieve 0.69 dBm and 0.81 dBm output power respectively at 62 GHz, and the power combining efficiency is higher than 94%.

Frequency sweep from 56 to 62 GHz has been performed with the measured maximum output power

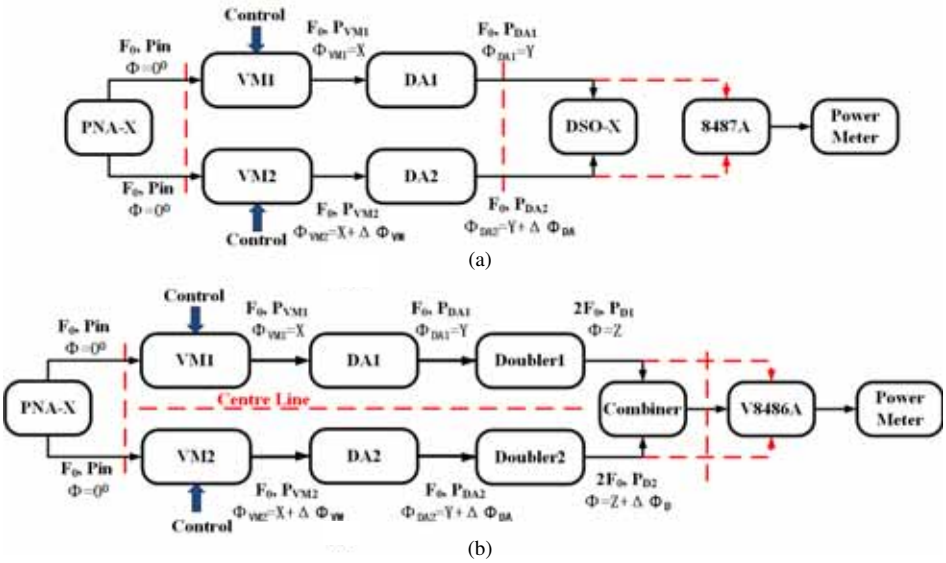

Figure 10. (a) The fundamental signal power calibration and phase difference test setup. (b) The single doubler and power-combined block output power test setup.

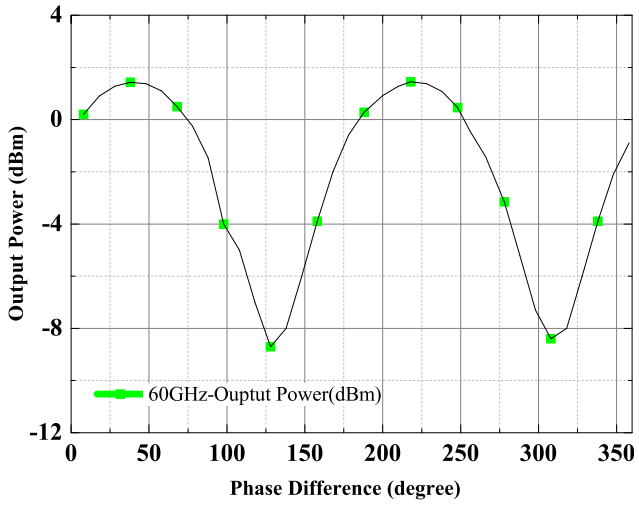

Figure 11. Power-combined output power at 60 GHz versus phase difference at 30 GHz.

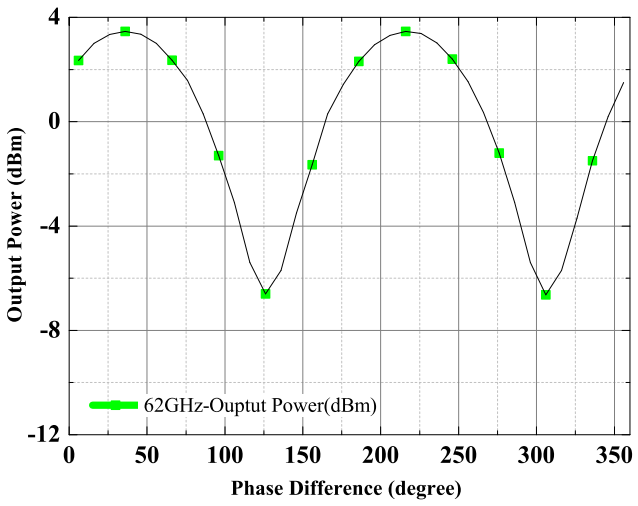

Figure 12. Power-combined output power at 62 GHz versus phase difference at 31 GHz.

of the power-combined block. A comparison between the two doublers and the power-combined block is provided in Fig. 13 and Fig. 14. Table 1 demonstrates the comparison of the proposed power-combined block with the single doubler at four typical frequency points. SM1 and SM2 mean the output powers of two doublers respectively. Ideal Com curve serves as a reference of ideal power-combining. When the phase difference $\Delta\Phi_{DA}$ is 0°, the combining output power is at least 1 dB lower than Ideal Com, and the combining efficiency (CE) is below 75% over the 56–62 GHz. Utilizing the fundamental frequency vector modulation technology to correct the phase deviation caused by fabrication and assembly errors, we can get the corresponding optimum power-combined loss between 0.45–0.25 dB and combining efficiency higher than 90%. The measured results clearly indicate that the proposed power-combining scheme based on fundamental frequency vector modulation can produce approximately twice as much power compared with the single doubler without sacrificing the bandwidth despite the fabrication and assembly errors.

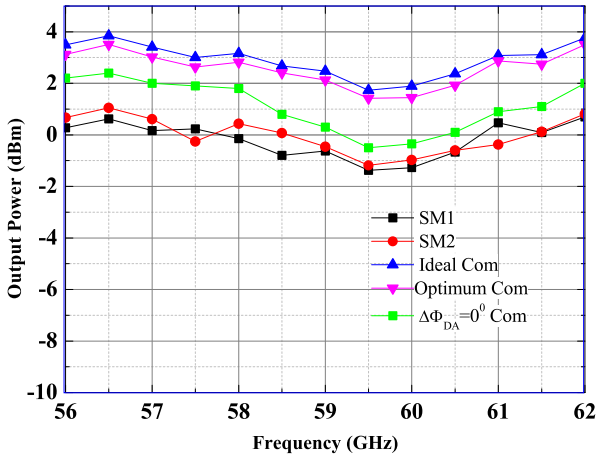

Figure 13. Comparison of the output power of the power-combined block with the single multiplier.

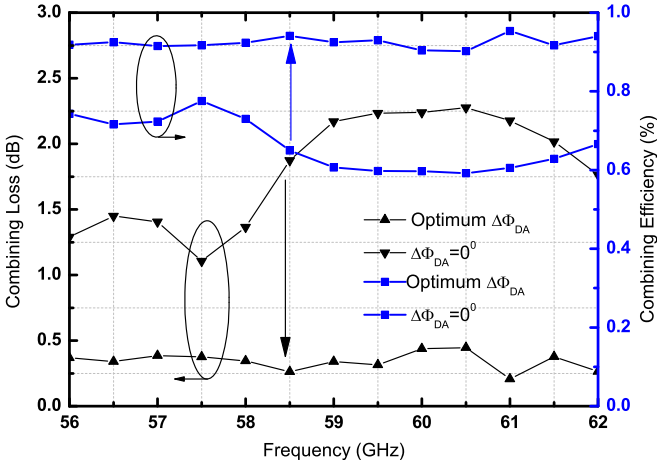

Figure 14. Comparison of the combining loss and efficiency of the power-combined block.

Table 1. The comparison of the proposed power-combined doublers with the single doubler.

Output Freq (GHz)	SM1 (dBm)	SM2 (dBm)	Ideal Com (dBm)	0° $\Delta\Phi_{DA}$ Com (dBm)	Optimum $\Delta\Phi_{DA}$ ($^\circ$)	Optimum Com (dBm)	Optimum CE (%)
56	0.28	0.67	3.49	2.2	20	3.12	91.8
58	−0.14	0.43	3.17	1.8	22	2.82	92.4
60	−1.27	−0.97	1.89	−0.35	38	1.45	90.4
62	0.69	0.81	3.77	2.0	36	3.50	94.1

4. CONCLUSIONS

A 60 GHz power-combined multiplier featuring two mirror fundamental frequency VMs, DAs and doublers has been designed, fabricated and tested. Adjusting the fundamental input VM to compensate the doubler output phase deviation caused by fabrication and assembly errors can increase the output power of the power-combined block by a factor of two compared with a single multiplier without sacrificing the bandwidth. Though the output power of the proposed power-combined block cannot achieve state-of-the-art output power limited by adopted doubler, the topology is an effective approach to enhance the power-handling capabilities despite fabrication and assembly tolerances at the MMW and terahertz solid-state multiplied LO chains.

ACKNOWLEDGMENT

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REFERENCES

1. Schellenberg, J., E. Watkins, M. Micovic, B. Kim, and K. Han, "W-band, 5 W solid-state power amplifier/combiner," *IEEE MTT-S Int. Dig.*, 240–243, May 2010.
2. Lee, C., et al., "A wafer-level diamond bonding process to improve power handling capability of submillimeter-wave Schottky diode frequency multipliers," *IEEE MTT-S Int. Dig.*, 957–960, Jun. 2009.

3. Nosaeva, K., et al., "Multifinger indium phosphide double-heterostructure transistor circuit technology with integrated diamond heat sink layer," *IEEE Trans. Electron Devices*, Vol. 63, No. 5, 1846–1852, May 2016.
4. Schwantuschke, D., P. Brckner, R. Quay, M. Mikulla, and O. Ambacher, "High-gain millimeter-wave AlGaN/GaN transistors," *IEEE Trans. Electron Devices*, Vol. 60, No. 10, 3112–3118, Oct. 2013.
5. Teppati, V., et al., "A W-band on-wafer active load-pull system based on down-conversion techniques," *IEEE Trans. Microw. Theory Tech.*, Vol. 62, No. 1, 148–153, Jan. 2014.
6. Belaid, M. and K. Wu, "Frequency multiplier using waveguide-based spatial power-combining architecture," *IEEE Trans. Microw. Theory Tech.*, Vol. 53, No. 4, 1124–1129, Apr. 2005.
7. Schumann, B., M. Hoft, and R. Judaschke, "A multi-element 150/300 GHz spatial power dividing/combining frequency doubler," *IEEE MTT-S Int. Dig.*, 1539–1542, 2002.
8. Magath, T., M. Hoft, and R. Judaschke, "A two-dimensional quasi-optical power combining oscillator array with external injection locking," *IEEE Trans. Microw. Theory Tech.*, Vol. 52, No. 2, 567–572, Feb. 2004.
9. Kirby, P. L., Y. Li, Q. Xiao, J. L. Hesler, and J. Papapolymerou, "Power combining multiplier using HBV diodes at 260 GHz," *2008 Asia-Pacific Microw. Conf.*, 1–4, Dec. 2008.
10. Maestrini A., et al., "In-phase power combining of submillimeter-wave multipliers," *33rd Int. Conf. on Infrared, Millimeter and Terahertz Waves*, 1–2, 2008.
11. Maestrini, A., et al., "In-phase power-combined frequency triplers at 300 GHz," *IEEE Microw. Wireless Compon. Lett.*, Vol. 18, No. 3, 218–220, Mar. 2008
12. Siles, J. V., et al., "A single-waveguide in-phase power-combined frequency doubler at 190 GHz," *IEEE Microw. Wireless Compon. Lett.*, Vol. 21, No. 6, 332–334, Jun. 2011.
13. Siles, J. V., et al., "A dual-output 550 GHz frequency tripler featuring ultra-compact silicon micromachining packaging and enhanced power-handling capabilities," *2015 Eur. Microw. Conf.*, 845–848, 2015.
14. Chen, Z. and J. Xu, "Design and characterization of a W-band power-combined frequency tripler for high-power and broadband operation," *Progress In Electromagnetics Research* , Vol. 134, 133–150, 2013.
15. Dong, J., Y. Liu, Z. Yang, H. Peng, and T. Yang, "Broadband millimeter-wave power combiner using compact SIW to waveguide transition," *IEEE Microw. Wireless Compon. Lett.*, Vol. 25, No. 9, 567–569, Sept. 2015.
16. Yin, K., K. Zhang, and J. Xu, "Characterization and design of millimeter-wave full-band waveguide-based spatial power divider/combiner," *Progress In Electromagnetics Research C*, Vol. 50, 65–74, 2014.
17. Siles, J. V., L. Choonsup, R. Lin, G. Chattopadhyay, T. Reck., C. Jung-Kubiak, I. Mehdi, and K. B. Cooper, "A high-power 105–120 GHz broadband on-chip power-combined frequency tripler," *IEEE Microw. Wireless Compon. Lett.*, Vol. 25, No. 3, 157–159, Mar. 2015.
18. Hou, Y., L. Li, R. Qian, and X. Sun, "An efficient technique for designing high-performance millimeter-wave vector modulators with low temperature drift," *IEEE Trans. Microw. Theory Tech.*, Vol. 56, No. 12, 3100–3107, Dec. 2008.
19. Han, K., M. Yang, Y. Sun, M. Chen, and X. Sun, "The integration of millimeter-wave active phased array antenna based on vector modulation technology," *IEEE Electr. Design Adv. Package & Syst. Symp.*, 1–4, Dec. 2011.
20. Ding, J., Q. Wang, Y. Zhang, and C. Wang, "A novel five-port waveguide power divider," *IEEE Microw. Wireless Compon. Lett.*, Vol. 24, No. 4, 224–226, Apr. 2014.