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Design of 900 MHz SiGe Power Amplifier with Linearization Bias Circuit

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Abstract—A single stage 900 MHz power amplifier (PA) with linearization bias circuit is designed with HHNEC 0.5 μm BIS500G power SiGe BiCMOS process. It is implemented by single-ended common emitter structure as a class AB power amplifier. The adopted active bias circuit is originally explained by using two virtue current sources, so that the mechanism of the improvement of linearity can be described more clearly. Then the mechanism is applied to guide the design of a power amplifier with an active bias circuit, which shows better linearity than resistor biased power amplifier by simulation. Through further design and measurement, the fabricated single stage power amplifier exhibits output power 1 dB compression point (OP1 dB) of 18.9 dBm, with power added efficiency (PAE) of 26.75% and power gain of 20.9 dB under 3.3 V voltage supply.

1. INTRODUCTION

Recently, the wireless communication system develops rapidly with the tendency of miniaturization and portability. Apart from development of advanced integrated circuit fabrication process, continuous improvement of automatic CAD tools [1–3] also makes a significant contribution to this trend. However, power amplifier is the last module of mobile terminal that has not yet been integrated completely. The reason is that most power amplifiers made by GaAs are expensive, and GaAs technology is incompatible with silicon technology. The CMOS power amplifier suffers from disadvantages such as low breakdown voltage and low output power. Even so, as a power amplifier is also indispensable in many other important applications such as radar system [4], base station [5], etc., researchers turned to SiGe power amplifier [6], since it not only is superior to CMOS power amplifier on frequency response and power gain, but also can be integrated well with CMOS technology while its speed and power performance have been comparable to GaAs technology. So the SiGe power amplifier has attracted much research interest in this field [7–9].

As development of application continuously demands for higher linearity, researchers focus on studying the bias circuit of power amplifier to improve linearity. The traditional bias circuit is simply composed of two series resistors [10]. With the increase of input radio frequency (RF) power, the average direct current (DC) will increase, and base emitter voltage will decrease due to rectification of base emitter diode of power transistor, which will cause gain compression and phase distortion. In order to solve this problem, researchers use an integrated diode linearizer bias circuit [10]. This bias circuit can compensate the variation of base emitter voltage to keep collector current of power transistor steady. But the base voltage of transistor in bias circuit is not as stable as the authors supposed. So a new bias circuit is proposed [11, 12], which adopts two series diodes to keep base voltage of the transistor constant. Some similar bias circuits with the same mechanism apply a capacitor or a reverse biased diode to couple the input RF power to bias circuit [13, 14]. However, the heat produced by large biasing current of power transistor will affect base emitter junction voltage of the transistor in bias circuit. So

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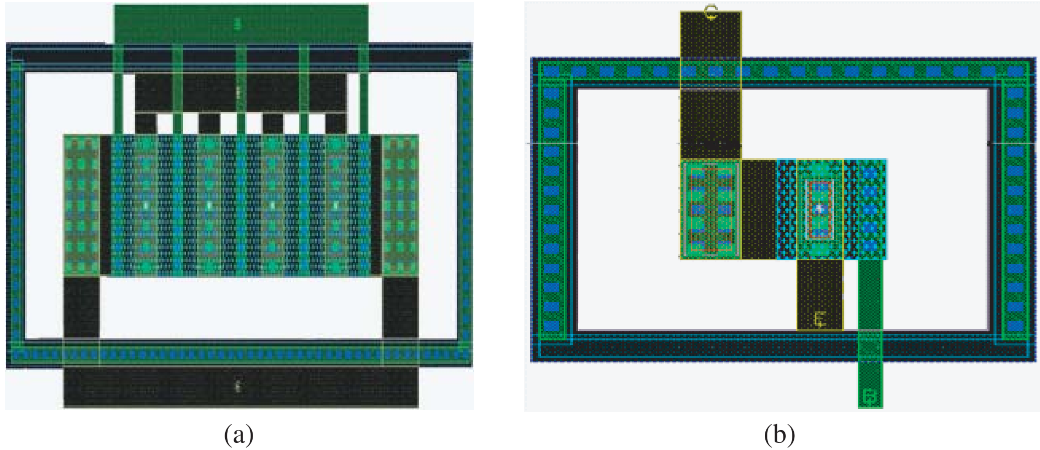
researchers employ adaptive bias control circuit as bias circuit [15, 16], in which the improved current mirror helps to keep the base emitter junction voltage insensitive to temperature. Though these active bias circuits show improvement on linearity, the analysis of their mechanism is not so clearly.

In this paper, an active bias circuit [17] is adopted. In order to obtain a more comprehensive analysis, its operation principle has been explained by employing two virtue current sources with quantitative analysis. With validation of simulation results, it can be known that analysis results can be used to guide the design of an active bias circuit. Then the performance comparison of resistor biased PA and PA with adopted active bias circuit is accomplished through simulation, which shows that the adopted active bias circuit can effectively improve the linearity of PA. Then the paper shows the design and measurement of a 900 MHz single stage power amplifier fabricated by Shanghai Huahong Grace Semiconductor Manufacturing Corporation BIS500G power SiGe technology.

2. ANALYSIS OF BIAS CIRCUIT

The topology of the bias circuit [17] is shown in Fig. 2. T_4 is the power transistor, the model of which is std452_1p2_op. It has four emitter fingers, five base fingers and two collector fingers. All power transistors used in this paper adopt this model. The geometry parameters of this model are listed in Table 1, and Fig. 1(a) shows its structure. As shown in Fig. 1(b), transistors T_1, T_2 and T_3 in the bias circuit adopt the model of std111_p6_op, which has one emitter finger, one base finger and one collector finger. And all transistors of the active bias circuits in this paper adopt this model, the parameters of this model are listed in Table 1.

For the convenience to deduce, it is assumed that power transistors and transistors in the active bias circuit have the same forward current gain h_{FE}. The property of temperature insensitivity is attributed to resistors R_2 and R_3, which can stabilize the base emitter voltage by slowing down the change of



(a) (b)

Figure 1. Layout of transistors. (a) Layout of model std452_1p2_op. (b) Layout of model std111_p6_op.

Table 1. Geometry parameters of adopted model of transistors used in this paper.

	Emitter Finger			**Base Finger**			**Distance between emitter finger and base finger**
	Width (μm)	Length (μm)	Finger space (μm)	Width (μm)	Length (μm)	Finger Space (μm)	Space (μm)
std452_1p2_op	1.2	5	4	0.4	7	4.8	1.8
std111_p6_op	0.6	2.4	–	0.7	4.4	–	0.85

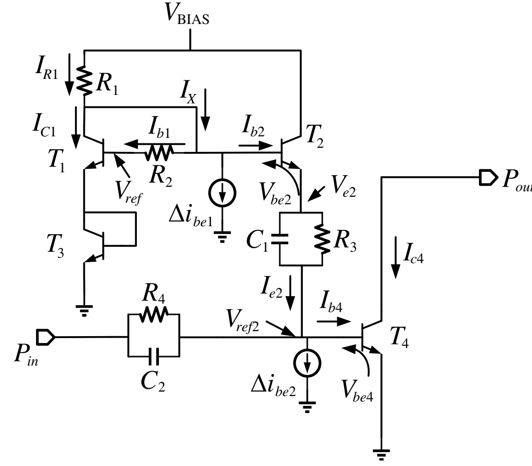


Figure 2. Topology of the power amplifier with adopted bias circuit.

bias current over temperature variation. The decrease of linearity caused by R_3 is compensated by C_1 [18], which can also couple RF signal to the bias circuit. The ratio of resistors can be set according to Eq. (1) [16] where A_E is the emitter area of the transistor in bias circuit. C_2 and R_4 are used as anti-oscillation elements for the PA.

$$\frac{A_E(T_2)}{A_E(T_1)} = \frac{R_2}{(h_{FE}+1)R_3} \tag{1}$$

Two virtual current sources $\triangle i_{be1}$ and $\triangle i_{be2}$ are added to the base of T_2 and T_4, respectively, which indicates the increase of base current in large-signal region [19]. In Fig. 2, the base current will be changed by $\triangle i_{be1}$ with the increase of input RF power which comes from the base emitter junction diode of T_2 [15]. Due to the clamping effect of T_1 and T_3, it can be known that

$$V_{\text{ref}} = 2V_{be1} = 2V_{be3} \tag{2}$$

$$V_{be1} = V_{\text{ref}}/2 = V_T \ln\left(\frac{I_{C1}}{I_S}\right) \tag{3}$$

In Eq. (3), V_T is the thermal voltage, and I_S is the saturation current of T_1. It is inferred from Fig. 2 that:

$$I_X = I_{R1} - I_{C1} \tag{4}$$

$$I_X - I_{b1} - I_{b2} - \triangle i_{be1} = 0 \tag{5}$$

$$I_{c1} = h_{FE} I_{b1} \tag{6}$$

$$I_{e2} = (h_{FE}+1)(I_{b2} + \triangle i_{be2}) \tag{7}$$

$$I_{R1} = \frac{V_{\text{BIAS}} - V_{\text{ref}} - I_{b1}R_2}{R_1} \tag{8}$$

$$V_{be2} = V_{\text{ref}} + I_{b1}R_2 - I_{e2}R_3 - V_{\text{ref2}} \tag{9}$$

Since T_1 and T_2 are identical, their base currents can be assumed as

$$I_{b1} = I_{b2} \tag{10}$$

In order to analyze the relationship between V_{be2} and $\triangle i_{be1}$, by substituting Eqs. (4) and (10) into Eq. (5), then Eq. (5) can be rewritten as

$$I_{b1} = \frac{(I_{R1} - I_{C1} - \triangle i_{be1})}{2} \tag{11}$$

Then substituting Eq. (11) into Eq. (9), V_{be2} is rewritten as

$$V_{be2} = V_{\text{ref}} + \left(\frac{I_{R1} - I_{C1} - \triangle i_{be1}}{2}\right) R_2 - I_{e2}R_3 - V_{\text{ref2}} \tag{12}$$

By substituting Eq. (8) into Eq. (12), V_{be2} can be rewritten as

$$V_{be2} = V_{\text{ref}} + \left(\frac{V_{\text{BIAS}} - V_{\text{ref}} - I_{b1}R_2}{2R_1}\right) R_2 - \frac{I_{C1}R_2}{2} - I_{e2}R_3 - V_{\text{ref2}} - \frac{\triangle i_{be1}R_2}{2} \tag{13}$$

By substituting Eqs. (6) and (7) into Eq. (13), V_{be2} is obtained as

$$V_{be2} = \left(1 - \frac{R_2}{2R_1}\right) V_{\text{ref}} + \frac{R_2}{2R_1}V_{\text{BIAS}} - \frac{I_{b1}R_2^2}{2R_1} - \frac{h_{FE}I_{b1}R_2}{2} - (1+h_{FE})(I_{b1}+\triangle i_{be1})R_3 - V_{\text{ref2}} - \frac{\triangle i_{be1}R_2}{2} \tag{14}$$

By substituting Eqs. (3) and (6) into Eq. (14), V_{be2} can be rewritten as

$$\begin{aligned} V_{be2} \;=\; & \left(1 - \frac{R_2}{2R_1}\right) V_{\text{ref}} + \frac{R_2}{2R_1}V_{\text{BIAS}} - \frac{I_S}{h_{FE}} \exp\left(\frac{V_{\text{ref}}}{2V_T}\right) \left[\frac{R_2^2}{2R_1} + \frac{h_{FE}R_2}{2} + (1+h_{FE})R_3\right] \\ & -(1+h_{FE})\triangle i_{be1}R_3 - V_{\text{ref2}} - \frac{\triangle i_{be1}R_2}{2} \end{aligned} \tag{15}$$

Since T_1 and T_2 have the same emitter area, Eq. (1) can be rewritten as

$$R_2 = (h_{FE} + 1)R_3 \tag{16}$$

By substituting Eq. (16) into Eq. (15), V_{be2} is rewritten as

$$\begin{aligned} V_{be2} \;=\; & \left(1 - \frac{R_2}{2R_1}\right) V_{\text{ref}} + \frac{R_2}{2R_1}V_{\text{BIAS}} - \frac{I_S}{h_{FE}} \exp\left(\frac{V_{\text{ref}}}{2V_T}\right) \left[\frac{R_2R_3(h_{FE}+1)}{2R_1} + \frac{h_{FE}R_2}{2}\right. \\ & \left. + (1+h_{FE})R_3\right] - \triangle i_{be1}R_2 - V_{\text{ref2}} - \frac{\triangle i_{be1}R_2}{2} \end{aligned} \tag{17}$$

The h_{FE} in the third item of Eq. (17) can be canceled, and the inverse of h_{FE} can be ignored. So Eq. (17) can be simplified and rewritten as

$$V_{be2} = \left(1 - \frac{R_2}{2R_1}\right) V_{\text{ref}} + \frac{R_2}{2R_1}V_{\text{BIAS}} - I_S \exp\left(\frac{V_{\text{ref}}}{2V_T}\right) \left[\frac{R_2R_3}{2R_1} + \frac{R_2}{2} + R_3\right] - V_{\text{ref2}} - \frac{3\triangle i_{be1}R_2}{2} \tag{18}$$

As it is known from Eq. (18), the first three items are constant values. On the assumption that V_{ref2} is a constant voltage, V_{be2} will decrease when $\triangle i_{be1}$ increases with the input RF power.

However, due to the clamping and rectification effect of the base emitter diode of power transistor, V_{ref2} also decreases with the increasing input signal power of T_4 [10]. On the assumption that V_{e2} is a fixed voltage, the base current will be changed by $\triangle i_{be2}$ when the input RF power at base terminal of T_4 increases. The mechanism is deduced as follows:

$$\frac{V_{e2} - V_{\text{ref2}}}{R_3} = I_{b4} + \triangle i_{be2} \tag{19}$$

Then V_{ref2} can be expressed as:

$$V_{\text{ref2}} = V_{e2} - I_{b4}R_3 - \triangle i_{be2}R_3 \tag{20}$$

According to Eq. (20), V_{ref2} will decrease when input signal power increases, which is the very reason that linearity of power amplifier degenerates. In fact, V_{ref2} and V_{e2} will change at the same time while the input RF power increases. The variation of V_{be2} can compensate the variation of V_{ref2} by adopting the bias circuit in Fig. 2. Thus the linearity of the power amplifier will be improved. The detailed explanations are made as follows. Now that the emitter terminal of T_4 is connected to ground, the base voltage of T_4 will be decreased by $\triangle i_{be2}R_3$ when V_{ref2} decreases. At the same time, the base terminal voltage of T_2 is fixed by the diode structure of T_1 and T_3 when V_{be2} is reduced, so the emitter terminal voltage of T_2 (V_{e2}) will increase by $\frac{3}{2}\triangle i_{be1}R_2$. Then V_{ref2} can be rewritten as follows:

$$V_{\text{ref2}} = V_{e2} - I_{b4}R_3 + \frac{3}{2}\triangle i_{be1}R_2 - \triangle i_{be2}R_3 \tag{21}$$

Eq. (21) shows that the variation of V_{ref2} is $\frac{3}{2}\triangle i_{be1}R_2 - \triangle i_{be2}R_3$. The variation of V_{ref2} and V_{be2} can be reduced by elaborately keeping the third and fourth items in Eq. (21) partially canceled. It will enhance the stability of quiescent operation point of T_4 and slow down corresponding gain compression. So the linearity of power amplifier can be improved.

3. CIRCUIT DESIGN AND PERFORMANCE COMPARISON

Since Eq. (21) shows relationship of key design parameters of bias circuit to improve the linearity of PA, it will be used to guide PA design with the active bias circuit in Fig. 4. In order to show the advantage of this kind of bias circuit, a resistor biased power amplifier in Fig. 3 has been simulated for comparison. Power cells of both PAs are composed of one power transistor. The emitter area of power transistor is $4 * 1.2\,\mu\text{m}{*}5\,\mu\text{m}$.

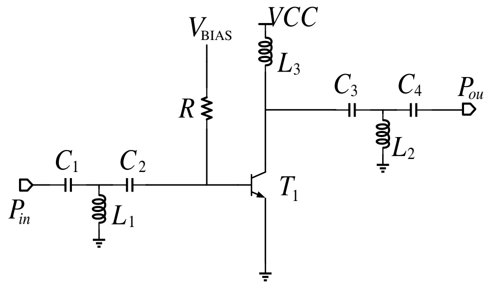


Figure 3. Resistor biased power amplifier.

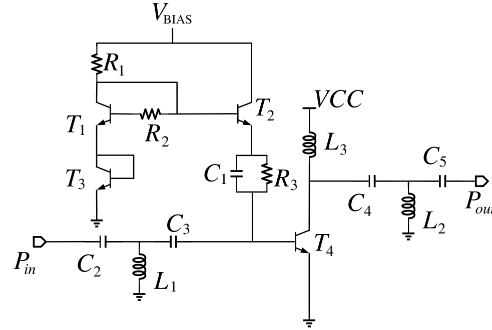


Figure 4. Power amplifier with adopted bias circuit.

The quiescent currents of both power amplifiers are 14.7 mA, and these two power amplifiers have the same topology except for bias network. According to Eq. (21), $\triangle i_{be1}$ and $\triangle i_{be2}$ must be known first, then the variation of base voltage of the power transistor can be calculated and partially canceled. As shown in Fig. 3 and Fig. 4, when RF signal excites the input terminal, the corresponding DC base current and DC base voltage of both power amplifiers are simulated. The comparison results are shown in Fig. 5. It is inferred from Fig. 5 that as the power amplifier operates in class AB mode, the base-emitter voltage decreases, and the base current increases in the resistor biased power amplifier with increase of input RF power. Although it sounds like a contradiction, in fact it is caused by two mechanisms. Firstly, in order to obtain bigger output power, the collector current of power transistor increases when the input power increases. Due to rectification of the base emitter diode of power transistor, the collector DC current increases, so it is the base DC current. Secondly, base voltage of power transistor will decrease as depicted in (20), and it will decrease the base current. These two mechanisms work at the same time, and the phenomenon of them may overlay or offset with each other. Comparing Fig. 5(a) with Fig. 5(b), it can be known that when base emitter voltage of PA with the adopted bias circuit has less variation than resistor biased PA, the corresponding base current shows bigger variation. So it is concluded that the rectification current has bigger influence, and the decrease of base current caused by second mechanism is completely canceled out by the increased rectification current. Thus the base current increases with input RF power.

Design flow of the bias circuit is as follows: $\triangle i_{be2}$ can be obtained by comparing the change of base current versus input power according to simulated results of resistor biased power amplifier. The simulated results of base voltage and base current versus input power are shown in Figs. 5(a) and (b). It is inferred from the simulation that the input power 1 dB gain compression point of resistor biased

Table 2. Comparison of simulated and calculated $\triangle V_{BE}$.

	simulated	**calculated**
$\triangle \mathbf{V_{BE}}$ of resistor biased PA	−5.174 mV	−4.378 mV
$\triangle \mathbf{V_{BE}}$ of PA with adopted bias circuit	3.279 mV	2.896 mV
$\mathbf{V_{BE}}$ stability improvement	36.6%	33.9%

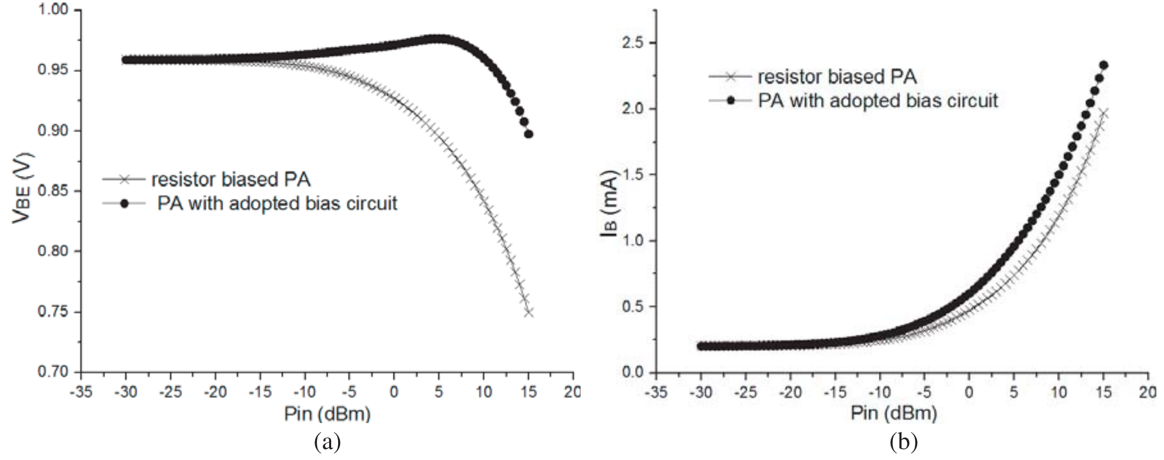


Figure 5. (a) Comparison of simulated DC voltage V_{BE} of power transistor versus input power. (b) Comparison of simulated DC base current I_B of power transistor versus input power.

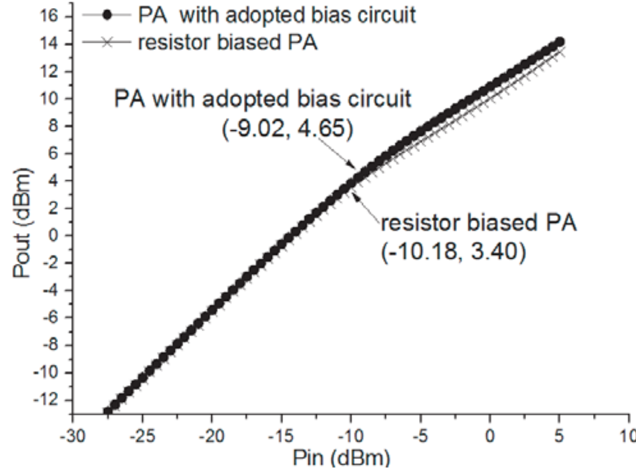


Figure 6. Simulated P1 dB of PA with different bias circuits.

PA is approximately -10 dBm. For alleviating gain compression effectively, the current and voltage variations are obtained when input power is swept from -30 dBm to -10 dBm, and simulated data show that $\triangle i_{\text{be2}}$ is 43.87 μA, and $\triangle V_{BE}$ is -5.174 mV. As for the power amplifier with adopted bias circuit, $\triangle i_{be2}$ is generally $h_{FE}+1$ times of $\triangle i_{be1}$. The simulated results show that the value of h_{FE} is 110. In general, the initial value of the resistor in a bias circuit can be set by simulation. Besides the absolute values of R_2 and R_3, the ratio of R_2 and R_3 can be fine-tuned to get better linearity. Through further simulation, R_3 is set as 100 Ω and R_2 set as 13.1 KΩ. So by substituting all these values into Eqs. (21), the calculated result shows that the voltage vibration amplitude of the PA with adopted bias circuit is effectively reduced, and obvious improvement on the stability of DC base voltage can be obtained. The calculated results have been validated by simulation. The comparison of simulated and calculated results is listed in Table 2. Though the calculated voltage vibration amplitude is reduced from 4.378 mV to 2.896 mV when the adopted bias circuit is applied, the stability of V_{BE} is improved by 33.9%, which basically coincides with simulated result. Because there are some approximations and omissions in calculation, the deviation between simulation and calculation is inevitable. On the whole, this method of calculation offers an effective guidance for active bias circuit design. At last, the comparison of simulated P1 dB of the above two kinds of PA is shown in Fig. 6. It can be known that the PA with adopted bias circuit shows better linearity.

4. DESIGN AND MEASUREMENT OF PA

Based on previous analysis, a single stage high linearity power amplifier with common emitter structure has been designed and fabricated for 900 MHz band by Huahong Grace Semiconductor Manufacturing Corporation BIS500G power SiGe technology. As shown in Fig. 2, the power amplifier designed on-wafer mainly contains power cell and bias circuit which is designed with the method mentioned above. The power cell of PA is composed of ten power transistors, and the total emitter area is 240 μm^2. The PA operates in class AB mode with 3.3 V supply voltage and 80 mA collector biasing current.

With the design method depicted above, a resistor biased power amplifier with the same DC operating point and matching network is simulated. As shown in Fig. 7, the topology is the same as that described in Fig. 2 except for bias circuit. Meanwhile, the comparison of simulated 1 dB gain compression point is shown in Fig. 8. As different bias networks are employed, input impedance and output power of the two PAs are slightly different. However, the adopted bias circuit still shows better performance on improvement of linearity than resistor as shown in Fig. 8.

The on-wafer measurement of the power amplifier is accomplished by the Cascade Microtech device probes and Agilent N5247A vector network analyzer. Calibrations to the probe tips are performed using short-open-load-through (SOLT) method which is available in the Network Analyzer software. When the DC probe touches the corresponding pad tightly, it can offer DC supply voltage to the bias circuit. The input GSG probe offers the input RF signal, and the output GSG probe not only offers supply voltage, but also transmits the output RF signal. A die photograph of the taped out power amplifier is shown in Fig. 9, and the chip area is $1100 * 491\ \mu m^2$, including pads and sealring.

As the layout is designed for on-wafer test with GSG pads, the chip cannot be bonded to the

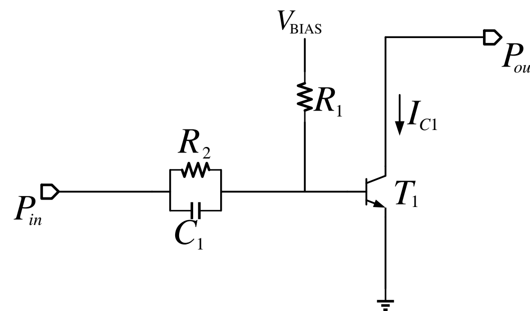


Figure 7. Topology of resistor biased single stage power amplifier.

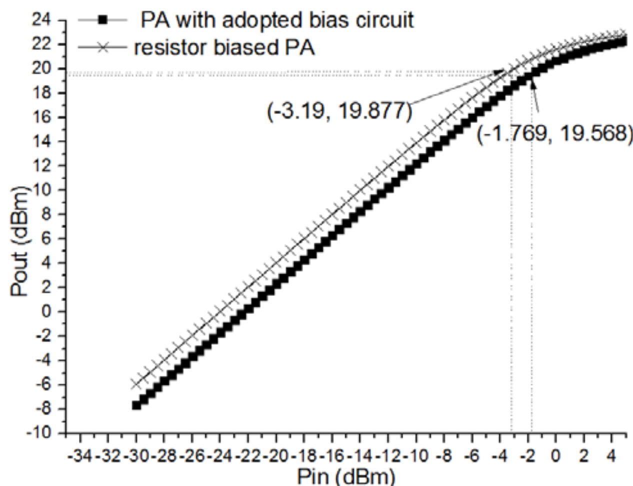


Figure 8. Comparison of simulated P1 dB of PA with different bias circuits.

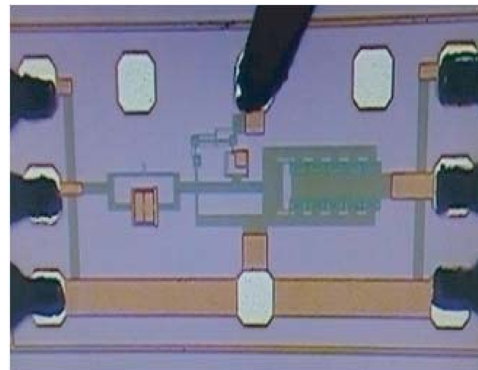


Figure 9. Die photograph of the PA.

Table 3. Comparison of measured performance of PA at different frequencies.

	IP1 dB (dBm)	OP1 dB (dBm)	Gt (dB)	PAE (@P1 dB)
850 MHz	−2	17.657	20.658	20.36%
900 MHz	−1	18.885	20.89	26.75%
950 MHz	−1	17.781	19.90	20.864%

Table 4. Comparison of performance.

Ref.	Tech.	Freq. (GHz)	OP-1 (dBm)	Gain (dB)	PAE(%) (OP-1)	Supply (V)
[**12**]	InGaP/GaAs HBT	5	19.7	22	22.5	3.3
[**20**]	0.35 μm SiGe BiCMOS	0.7	17	22	36	4.2
[**21**]	0.18 μm SiGe BiCMOS	2.4	18.5	–	19	3.3
[**22**]	0.18 μm SiGe BiCMOS	2.4	20	12	–	3.3
This work	0.5 μm SiGe BiCMOS	0.9	18.9	20.9	26.75	3.3

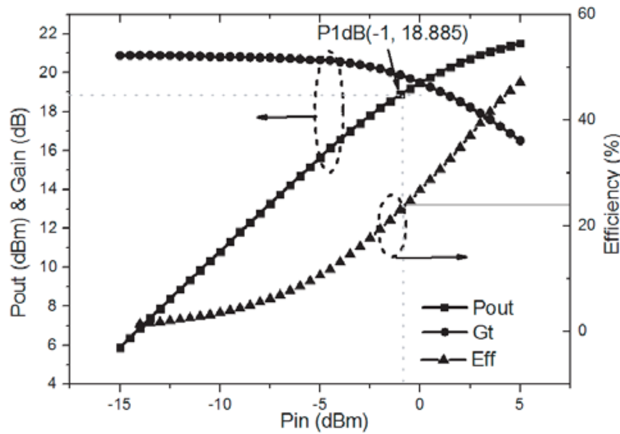


Figure 10. Measured P1 dB, Gain and PAE of the single stage PA.

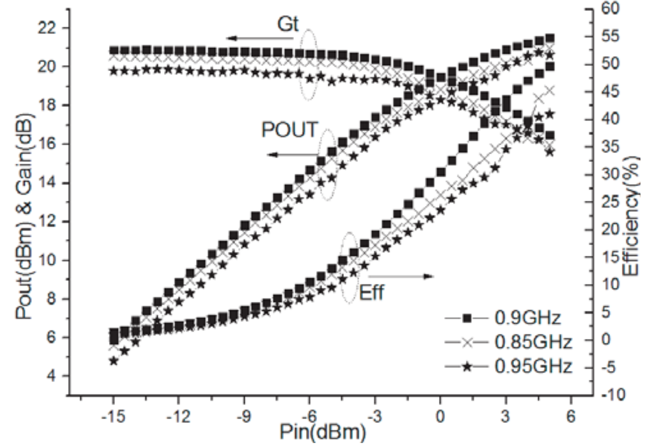


Figure 11. Comparison of measured performance of taped out PA at different frequencies.

printed circuit board for matching and measurement. So the matching networks are completed by the Maury Load-Pull system which is connected to GSG probes. In order to get better performance, both source and load terminals of the Load-Pull system are matched for optimized linearity. The measured performance is shown in Fig. 10, in which the output power 1 dB gain compression point is 18.9 dBm with 26.75% PAE at this point, and power gain of the PA is 20.9 dB. These results are basically consistent with the simulated data in Fig. 8, which shows that the simulated results in this paper are credible. The saturated output power is 21.51 dBm, and the corresponding PAE is 49.617%. In addition to 900 MHz, the performances of 850 MHz and 950 MHz are also measured and shown in Fig. 11 and Table 3, which shows that the performance of PA keeps steady in 100 MHz bandwidth with fixed source and load impedance. At last, Table 4 lists the comparison of published works and this paper [12, 20–22]. As shown in Table 4, the performance of the fabricated SiGe PA is comparable to the GaAs PA, and its linearity is better than other SiGe PAs in the table. This kind of PA can have a broad application prospect in wireless communication systems, such as RFID reader and GSM.

5. CONCLUSION

In this paper, the operation principle of an active bias circuit is analyzed more clearly with two virtue current sources. With the help of simulation, it can be applied to design high linearity power amplifier. Compared with resistor biased PA, the PA with adopted active bias circuit shows better linearity. At last, with the design method of the active bias circuit described in this paper, a single stage class AB PA operating at frequency of 900 MHz is designed and fabricated. Its measured 1 dB gain compression point is 18.9 dBm, and PAE at P1 dB is 26.75%. At the same time, the measured performance can keep steady in 100 MHz bandwidth.

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