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Five Ports Power Divider Designs with Controllable Power Division and Switching Capabilities

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Abstract—Two new 5-port power divider designs capable of controlling the power division ratios between the output ports are proposed. In the first design, the input power is switchable between two pairs of the output ports. This is implemented by terminating the dividers' two open-ended stubs with varactor diodes. In the second design, the power division is controlled by a single varactor diode that terminates one of the dividers two open-ended stubs. With judicious choice of dc bias voltage, it is possible to realize equal as well as unequal power division ratios between the four output ports. High power division ratios was achieved without the necessity of involving transmission lines with high impedances. It is demonstrated that this design is capable of generating amplitude modulated signals. Simulation and measurement results are presented for the designs to show their power division and matching performance.

1. INTRODUCTION

Power dividers are considered as one of the essential components in microwave systems. Numerous designs of microwave power dividers with various features have been developed to cater for new applications and to meet certain design requirements. Frequency agility and power division controllability are examples of features required in some modern power divider designs [1]. To control the power division ratio, a reconfigurable mechanism should be introduced to the power divider design. Such reconfigurability in power dividers can be implemented using MEMS [2, 3], PIN diodes [4–6], RF switches [7], and varactor diodes [8]. In [2], a 5-states power divider, which can be reconfigured using MEMS switches, has been proposed. The divider consists of two hybrid couplers and a reflection-line phase shifter. A ratio of 6:1 is reported for one of the states which are all well performing in terms of matching and isolation. Another MEMS-reconfigurable power divider has been proposed in [3] which is a T junction implemented using composite Right/Left-handed transmission lines. The divider has a dual-band performance and can be switched to achieve the three ratios of 1:1, 2:1, and 3:2 in both bands. Several dual-state 2-way power dividers which can be reconfigured using PIN diodes have been proposed [4–6]. In these dividers, the power division for the first state is always 1:0, whereas the achieved ratio in the second state is 1:1 in [4], 1:3 in [5], and 1:5 in [6]. It is designed to operate in two states; the first with a specific division ratio and the second with the power routed from one output port to another. Single pole double throw RF switches have also been utilized in the design of reconfigurable power dividers. In [7], a 2-way power divider with four modes of operation is constructed through the use of such switches. In [8], varactors have been utilized in a power divider to achieve a power division ratio that can be adjusted based on the biasing voltage.

Reconfigurable power dividers are utilized in many applications, including: reconfigurable feeding networks for antenna arrays [9, 10] and dual-state amplification schemes [11, 12]. In [9], a reconfigurable 1×4 power divider with three states is utilized in an antenna array for beam-forming. A feeding network constituted from a reconfigurable power divider is presented in [10]. Dual-state amplifiers are used in

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wireless communication systems to achieve high average efficiency and hence improve battery life [11]. Such amplifiers require power dividers/combiners with reconfigurable features and good matching in both states of operation. More specifically, the power divider must provide a state of operation where the input power is routed to a specific output port. Reconfigurable power dividers designed for such a scheme are demonstrated in [4–6, 12].

Arbitrary power division ratios can be achieved by properly selecting the characteristic transmission line impedances in some multi-port planar power dividers [13, 14]. However, to realize a different ratio, the divider needs to be redesigned and refabricated. Also, realizing high power division ratios is difficult as the design will involve high characteristic impedances which are difficult to fabricate. Overcoming such an issue can be accomplished by untraditional techniques that involve the use of defected ground structures [15], grooved substrates [16], and electromagnetic band gap patterns [17].

In this paper, two power divider designs with reconfigurable features are analyzed and implemented. These designs are developed from a 5-port power dividing network through the use of varactor diodes. The first design is a switchable 2-way power divider, whereas the second design is a 4-way power divider with a controllable power division ratio. In both designs, the output ports are grouped into two pairs. In the first design, the output power is switchable between the two pairs of output ports by independently biasing two varactor diodes. In the second design, the input power is divided between the two output pairs with a power division ratio that is controlled using a single varactor diode. Various power division ratios are achievable by adjusting the dc bias voltage applied to the varactor diode. In addition, the designs capability to generate amplitude modulated signals is investigated.

In the next section, the theoretical analysis and design configurations of the proposed power dividers will be introduced. Subsequently, the simulation and measurement results will be compared and discussed.

2. THEORETICAL ANALYSIS OF THE PROPOSED POWER DIVIDERS

The circuit scheme of the proposed 5-port power dividers is shown in Fig. 1. The lines joining adjacent ports are all $\lambda/4$ long at the operating frequency. Nodes m and n are connected to open circuited lines that reflect reactive impedances jX_m and jX_n at the respective nodes as shown in Fig. 1. The circuit is symmetrical about the line joining the terminated nodes m and n which dictates that $V_1 = V_2$ and $V_3 = V_4$ (where V_1 to V_4 are the voltages of the output ports 1 to 4, respectively, and V_5 is the input voltage at port 5).

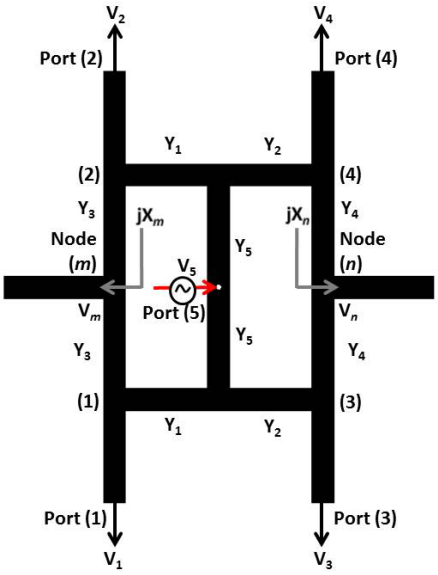

Figure 1. The design configuration of the proposed 5-port power dividers.

Let us assume that the line admittances Y_1 to Y_5 and the reactive loads jX_m and jX_n are chosen so that port 5 is matched. By using the Norton equations at nodes 1, 2, 5, m, and n, the scattering matrix elements are derived in terms of normalized reactances X_m and X_n, as follows:

$$S_{15} = S_{25} = -\frac{\frac{y_1}{2y_5}}{1 + 2j(y_3)^2 X_m} \tag{1}$$

$$S_{35} = S_{45} = -\frac{\frac{y_2}{2y_5}}{1 + 2j(y_4)^2 X_n} \tag{2}$$

Note that all admittances y_i (where $i = 1, \ldots, 5$) are normalized to the ports characteristic admittance Y_o, whereas the reactances X_m and X_n are normalized to the system characteristic impedance Z_o.

For port 5 to be matched, we should have $S_{55} = 0$, or:

$$2\left(|S_{15}|^2 + |S_{35}|^2\right) = 1 \tag{3}$$

Some interesting results that can be obtained for certain combinations of X_m and X_n are discussed next.

2.1. Case 1: One of the Terminated Nodes Is Short Circuited and the Other Is Open Circuited

Assuming that the short circuited node is node m ($X_m = 0$) and that the open circuited one is node n ($X_n = \infty$), Equations (1)–(3) yield to:

$$S_{15} = S_{25} = -\frac{y_1}{2y_5} \tag{4}$$

$$S_{35} = S_{45} = 0 \tag{5}$$

$$y_5 = \frac{y_1}{\sqrt{2}} \tag{6}$$

This means that all the power fed into port 5 is divided equally between ports 1 and 2 only, providing that y_5 satisfies (6).

2.2. Case 2: Both Terminated Nodes Are Short Circuited ($X_m = X_n = 0$)

In this case, Equations (1)–(2) yield:

$$S_{15} = S_{25} = -\frac{y_1}{2y_5} \tag{7}$$

$$S_{35} = S_{45} = -\frac{y_2}{2y_5} \tag{8}$$

Assuming the special case, $y_1 = y_2$, then Eq. (3) yields:

$$y_5 = \sqrt{\frac{y_1^2 + y_2^2}{2}} = y_1 \tag{9}$$

Accordingly, all the input power is divided equally among all output ports providing that relation (9) is satisfied.

2.3. Case 3: One of the Terminated Nodes Is Short Circuited and the Other Is Reactively Loaded

For example, the short circuited node is node m; $X_m = 0$, and the reactively loaded node is node n; $0 \leq |X_n| < \infty$. In this case, the power will be divided into different power division ratios between the two pairs of output ports as given by Eqs. (1) and (2) based on the value of X_n.

In the following sections, we present simulation and measurement results of the power dividers which are designed based on the aforementioned theoretical cases.

3. RESULTS AND DISCUSSION

In this section, two power divider designs based on the circuit shown in Fig. 1 are presented. In these designs, the reactances X_m and/or X_n are implemented using a transmission line connected to a varactor diode. This is possible since the varactor diode is in essence a variable reactance. The first design is based on case 1 of Section 2.1, whereas the second design is based on case 3 of Section 2.3. The design frequency of the proposed designs is chosen to be 5 GHz. The characteristic impedances of the lines connecting the adjacent ports in Fig. 1 (Z_1, Z_2, Z_3, and Z_4) are all 50, where $Z_i = 1/Y_i$. The value of the impedance Z_5 is set according to the conditions discussed in the previous section. Both designs are implemented on a Rogers Duroid 5880 substrate with dielectric constant of 2.2 and thickness of 0.787 mm. The designs were simulated using Advanced Design System (ADS) package, and then a prototype of each design was fabricated to verify the design concepts. The details of each design along with the simulation and measurement results are presented next.

3.1. Switchable 2-Way Power Divider Design

In this design, the configuration shown in Fig. 1 is developed to be a switchable power divider with two switching states where the input power can be switched between the output ports pairs (1, 2) or (3, 4). This is an implementation of case 1 discussed in Section 2.1 where all the power fed to port 5 is equally divided between a pair of output ports (1, 2) or (3, 4) depending on the terminations of nodes m and n. When nodes m and n are short- and open-circuited, respectively, the input power is divided between the output ports pair (1, 2) which is labeled as *switching state* A. On the other hand, when nodes m and n are open- and short-circuited, respectively, the input power is divided between the output ports pair (3, 4) which is labeled as *switching state* B. Therefore, 2-way switchable power division is possible by controlling the terminations (short or open) of nodes m and n. Meanwhile, it is required to satisfy $y_1 = y_2 = \sqrt{2}y_5$ for port 5 to be matched.

To implement this two-way switchable power divider, each of nodes m and n is connected to a transmission line terminated with a varactor diode. The lines connected to nodes m and n are both of the same length L_{s1} and characteristic impedance Z_{stub} ($Z_{\text{stub}} = Z_3 = Z_4$). Each of these varactor-terminated lines is equivalent to an open stub with an effective length L_{eff} which is controlled by the value of junction capacitance C_j of the varactor. To realize a short circuit termination, the value of C_j is set so that $L_{eff} = \lambda/4 + k\lambda/2$ (k is an integer), whereas to realize an open circuit termination, C_j is set so that $L_{eff} = k\lambda/2$ (k is an integer).

The configuration of the proposed design is shown in Fig. 2, whereas a photograph of the fabricated design is shown in Fig. 3. In this configuration, two varactors (SMV2019 manufactured by Skyworks)

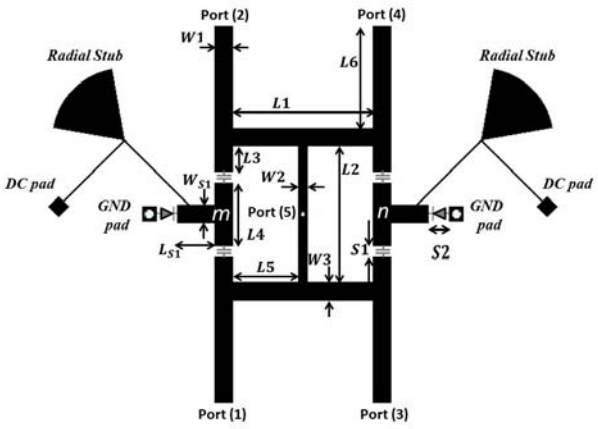

Figure 2. Configuration of the switchable 2-way power divider.

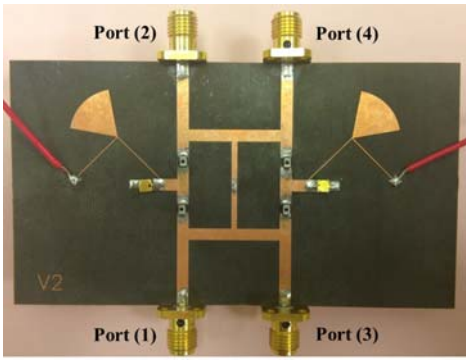

Figure 3. Photograph of the fabricated switchable 2-way power divider.

Table 1. Dimensions of the switchable 2-way power divider.

Symbol	Value (mm)	Symbol	Value (mm)
L_1	18.6	L_{S1}	5
L_2	18	$W2$	1.2
L_3	3.39	$W1$, $W3$	2.42
L_4	8.42	W_{S1}	2.42
L_5	8.7	$S1$	1.4
L_6	13.58	$S2$	2.64

Table 2. Summary of the switching states.

	State A	State B
Output Ports Pair	(1, 2)	(3, 4)
Node m Termination	Short	Open
Node n Termination	Open	Short
Left Varactor Bias	20 V	0 V
Left Varactor C_j	0.16 pF	2.25 pF
Right Varactor Bias	0 V	20 V
Left Varactor C_j	2.25 pF	0.16 pF

are incorporated in the blank spaces $S2$. Also, four 39 pF capacitors (0805 ACCU-P manufactured by AVX) are placed at the blank spaces $S1$ to block the dc power from reaching the RF ports of the circuit and to isolate the dc bias voltages applied to the varactor diodes from each other. It is worth mentioning that the blocking capacitors were not placed in the stubs, and this is to avoid an increase in the electrical length of the stubs, which results in a narrower bandwidth. Each varactor diode is biased independently using a bias circuit as shown in Fig. 2. The optimized dimensions of the design are listed in Table 1. It should be noted that the circuit (excluding the bias circuits) is symmetrical about the horizontal and vertical axes passing through port 5.

To realize switching state A, node m is short-circuited while node n is open-circuited, and this is achieved by biasing the varactors so that C_j of the left and right varactors are set to 0.16 pF (corresponding to the maximum reverse bias of 20 V) and 2.25 pF (corresponding to a DC bias of 0 V), respectively. In state B, the terminations of nodes m and n are interchanged. This is achieved by simply interchanging the bias voltages of the two varactors. Summary of the two switching states is presented in Table 2. It is to be mentioned that the varactors are simulated using their series R-L-C equivalent circuit. The capacitance in this equivalent circuit is the junction capacitance, whereas the inductance and resistance represent the the packaging effect of the varactor diode lumped with the effects of packaging and the grounding via. The values of the inductance and resistance used in the simulation for both varactors are 1 nH and 4.8 Ω, respectively. The simulation and measurement results of both switching states are shown in Fig. 4. It can be observed that the simulation and measurement results are in good agreement.

The results of state A where the input power is divided equally only between ports 1 and 2 with $|S_{15}| = |S_{25}|$ are shown in Fig. 4(a). It can be seen that $|S_{15}| = -3.47$ dB at the operating frequency of 5 GHz which indicates a loss of approximately 0.4 dB (due to the resistance of the varactors and the losses associated with the transmission lines). Plots of $|S_{25}|$ and $|S_{45}|$ are not shown because they are identical to that of $|S_{15}|$ and $|S_{35}|$, respectively. The response of $|S_{55}|$, which is shown in Fig. 4(c), indicates good matching performance. The operating range for which both $|S_{35}|$ and $|S_{55}|$ are less than -10 dB is between 4.47 GHz and 5.52 GHz which is more than 1 GHz of bandwidth. In this frequency range, $|S_{15}|$ and $|S_{25}|$ vary within 1 dB. If we consider the maximum allowable reflection coefficient to

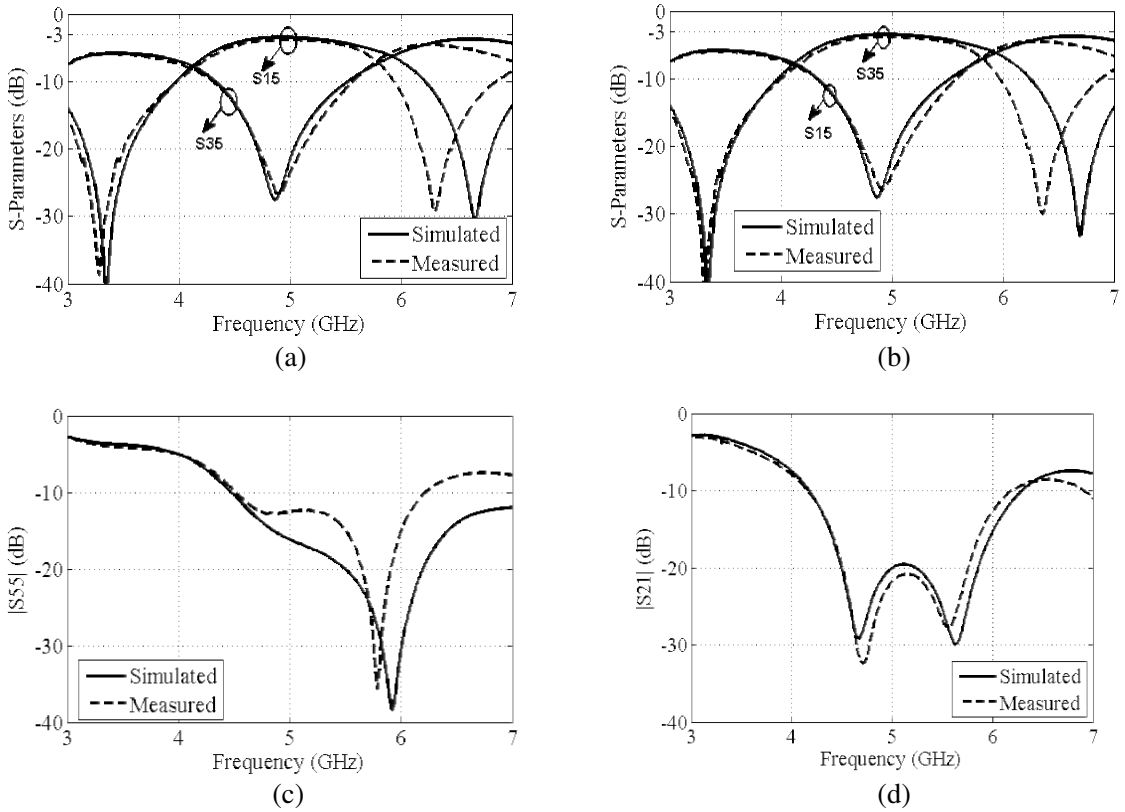

Figure 4. (a) Measurement vs. simulation results for $|S_{15}|$ and $|S_{35}|$ (State A). (b) Measurement vs. simulation results for $|S_{15}|$ and $|S_{35}|$ (State B). (c) Measurement vs. simulation results for $|S_{55}|$ (identical for both states). (d) Measurement vs. simulation results for $|S_{21}|$ (State A).

be -12 dB, then the operating range will be limited to the range 4.7 GHz up to 5.52 GHz. The isolation between ports 1 and 2 is demonstrated for state A by the plot of $|S_{21}|$ in Fig. 4(d). It can be observed that $|S_{21}|$ is below -20 dB over the bandwidth 4.5–5.85 GHz.

As expected, similar results are observed for state B where the results shown in Fig. 4(b) are almost the same as in state A with the output ports being the pair (3, 4) instead of (1, 2). Good matching is also achieved in state B with the plot of its $|S_{55}|$ being identical to that shown in Fig. 4(c) for state A.

As can be seen from Fig. 4, there is a good agreement between simulated and measured results, except at frequencies above 6 GHz where a shift in the frequency response is noticed.

3.2. Controllable 4-Way Power Divider of Various Division Ratios

In this design, the configuration shown in Fig. 1 is used as a 4-way power divider where the input power is divided between the output ports pairs (1, 2) and (3, 4) with different power division ratios. The proposed design is shown in Fig. 5, and it is an implementation of case 3 discussed in Section 2.3, where the line admittances are given by Equations (1)–(3) with $X_m = 0$ (node m is shorted). In this case, node m is short-circuited, whereas node n is terminated with a reactive load. By varying the reactance X_n of the load, different power division ratios between the output pairs (1, 2) and (3, 4) can be attained. The two terminations are practically implemented in the proposed design by connecting node m to a quarter wavelength open stub (effectively short circuiting node m at the design frequency) and attaching a varactor-terminated transmission line to node n. As discussed in the previous design, the varactor-terminated line is equivalent to an open stub with an effective length which is controlled by the value of C_j of the varactor. Let C_{oc} and C_{sc} denote the values of C_j which make the varactor-terminated line equivalent to open and short circuit terminations, respectively. When the value of C_j

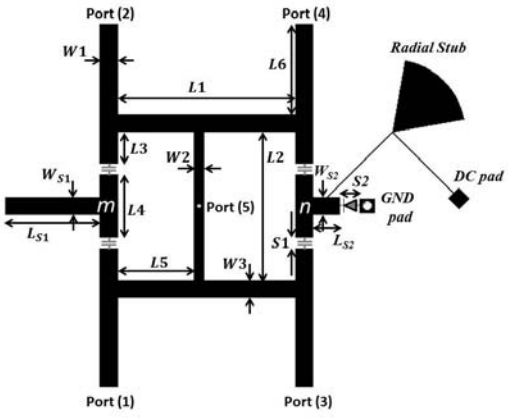

Figure 5. Configuration of the controllable 4-way power divider.

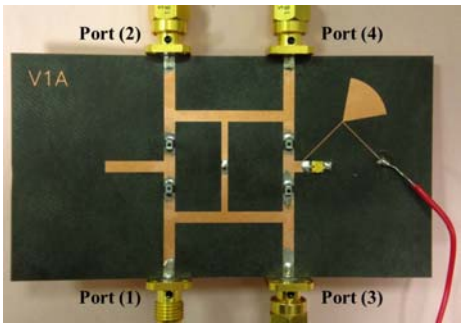

Figure 6. Photograph of the fabricated layout of the controllable 4-way power divider.

Table 3. Dimensions of the controllable 4-way power divider.

Symbol	Value (mm)	Symbol	Value (mm)
L_1	23.4	L_{S1}	12.5
L_2	19.5	L_{S2}	3.5
L_3	4.14	$W2$	1.4
L_4	8.42	$W1$, $W3$	2.42
L_5	10	W_{S1}	2.42
L_6	11.83	W_{S2}	2.42
$S1$	1.4	$S2$	2.64

Table 4. Simulation and measurement results of the controllable 4-way power divider at 5 GHz.

C_j (pF)	$S_{15} = S_{25}$		$S_{35} = S_{45}$		S_{55}	
	Sim. (dB)	**Meas. (dB)**	**Sim. (dB)**	**Meas. (dB)**	**Sim. (dB)**	**Meas. (dB)**
0.16	−6.336	−6.965	−6.545	−6.574	−11.74	−10.02
0.26	−6.861	−6.942	−6.274	−6.600	−11.77	−10.06
0.38	−5.624	−5.895	−7.761	−7.666	−13.25	−11.45
0.46	−4.806	−5.079	−9.347	−9.108	−14.57	−13.19
0.71	−3.740	−3.896	−14.27	−14.89	−17.53	−20.61
0.99	−3.440	−3.681	−18.58	−19.28	−18.65	−28.85
2.25	−3.257	−3.606	−30.24	−26	−19.08	−27.93

of the varactor is in the range $C_{sc} \leq C_j \leq C_{oc}$, then, the input reactance X_n of the varactor terminated line can take any value from that of a short circuit to that of an open circuit (i.e., $0 \leq X_n < \infty$). Therefore, the power division between the output pairs (1, 2) and (3, 4) is controlled by the value of C_j. The output power in this case is gradually steered towards the pair (1, 2) starting from equal division between the two pairs when $C_j = C_{sc}$ (Section 2.2) until the output power is totally steered to the pair (1, 2) when $C_j = C_{oc}$ (Section 2.1).

The varactor used in this design is also the SMV2019 manufactured by Skyworks, and it is placed in the space labeled $S2$. The varactor is biased using the radial stub circuit as shown in Fig. 5. Four 39 pF dc blocking capacitors (0805 ACCU-P manufactured by AVX) are incorporated in the design, and they are placed in the spaces labeled $S1$. The two capacitors on the left (near the quarter wavelength open stub) are placed only to maintain design symmetry. The optimized line dimensions of the design are listed in Table 3, whereas a photo of the fabricated design is shown in Fig. 6.

In Figs. 7(a)–(c), the simulation and measurement results of the design configuration shown in Fig. 5 are plotted for three selected values of C_j. These values lie in the range between $C_{sc} = 0.16$ pF corresponding to the maximum reverse bias of 20 V and $C_{oc} = 2.25$ pF corresponding to a dc bias of 0 V. It can be observed from the plots shown in Figs. 7(a) and (b) that at the operating frequency of 5 GHz, the input power is divided between the output ports pairs in ratios that depend on the value

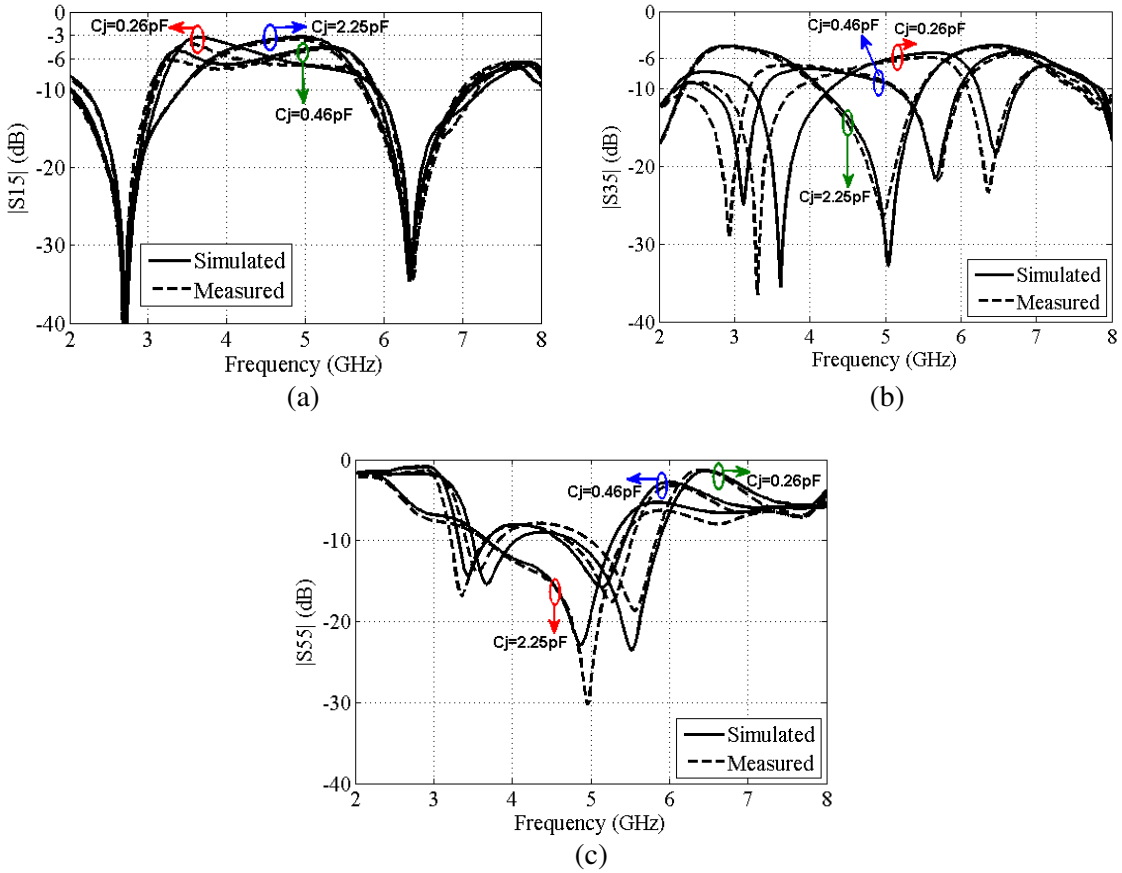

Figure 7. (a) Measurement vs. simulation results of $|S_{15}|$. (b) Measurement vs. simulation results of $|S_{35}|$. (c) Measurement vs. simulation results of $|S_{55}|$.

Table 5. Capacitance ranges of the used C_j values in Fig. 8.

Freq. Range (GHz)	C_j Range (pF)
4.4–4.7	0.71–2.25
4.712–4.844	0.46–2.25
4.856–4.988	0.38–2.25
5–5.4	0.16–2.25

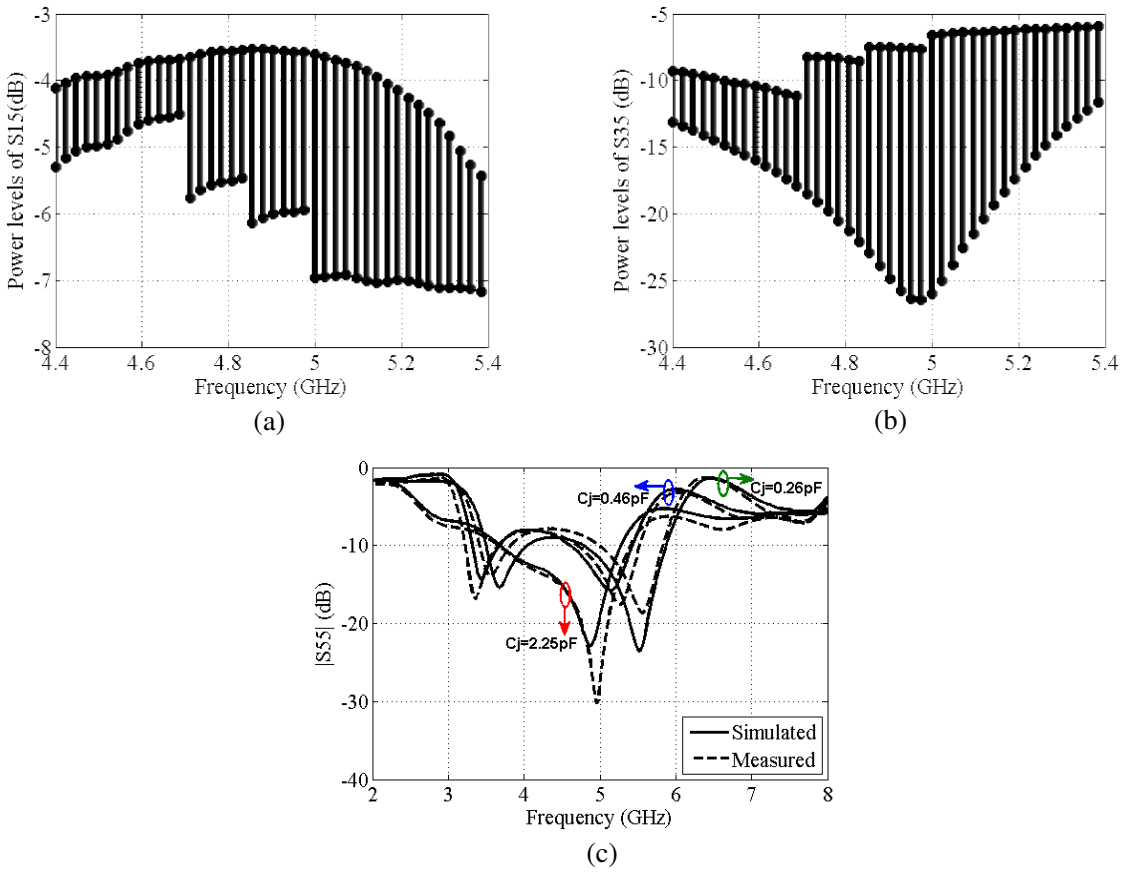

Figure 8. Available power levels while adjusting C_j value within the acceptable capacitance ranges. (a) S_{15}. (b) S_{35}. (c) S_{55}.

of C_j. The power division ratios at the design frequency are listed in Table 4 for different values of C_j. It is observed from Table 4 that while increasing C_j from 0.16 pF to 2.25 pF, the power level of S_{15} increases from -6.96 dB to -3.61 dB and the power level of S_{35} decreases from -6.57 dB to -26 dB. It can be seen from Fig. 7(c) that having a good input matching at frequencies other than 5 GHz is dependent on the value of C_j. For example when $C_j = 0.26$ pF, matching occurs in the frequency range 4.6 to 5.8 GHz while for $= 2.25$ pF the matching occurs in the range from 3.6 to 5.5 GHz.

Alternatively, the range of values of C_j that results in good matching ($|S_{55}| \leq -10$ dB) are listed in Table 5 for specific bandwidths in the frequency range between 4.4–5.4 GHz. For these ranges of C_j, the measured magnitude levels of S_{15}, S_{35}, and S_{55} of the fabricated design are plotted in Fig. 8 at the four different frequency ranges given in Table 5. This figure gives the range of achievable power level at ports pairs (1, 2) and (3, 4), as well as the matching level range for each frequency within the bandwidth of 1 GHz (4.4–5.4 GHz).

It should be pointed out that this design is capable of achieving high power division ratios without the necessity of involving high transmission line impedances, which is a major advantage. The challenge of designing power dividers with high power division ratio, which requires high impedance transmission lines and is a drawback due to fabrication limitation, was tackled previously by using a defected ground structure [15], grooved substrate [16], or electromagnetic band gap pattern [17]. In such designs, the power divider becomes more complicated. One more concern that arises is that the fabricated designs can only cater for a certain power division ratio since the division ratio is determined by the line impedances which cannot be readjusted after fabrication.

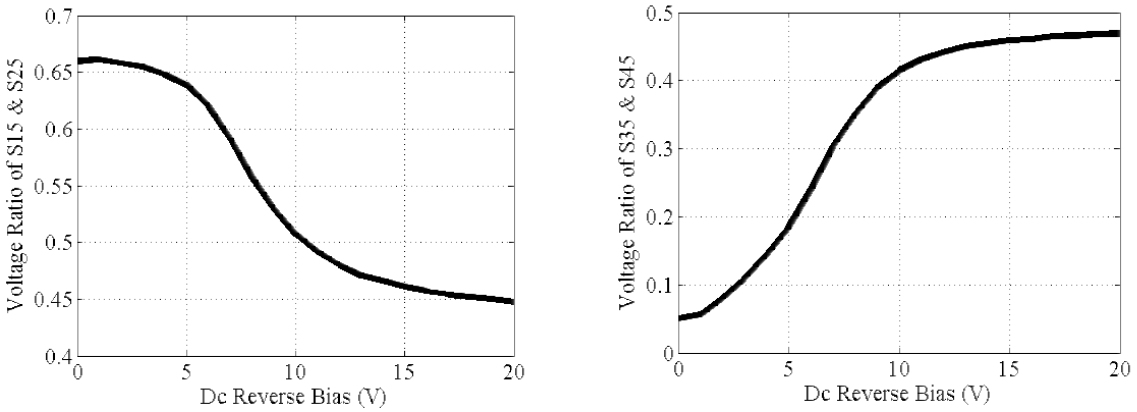

Figure 9. Measured voltage ratios vs. the applied DC reverse bias voltages at 5 GHz for the controllable 4-way power divider. (a) Voltage ratios of S_{15} and S_{25}. (b) Voltage ratios of S_{35} and S_{45}.

3.2.1. Application as Amplitude Modulator

In this section, we explore the possibility of using the proposed design in Fig. 5 as an amplitude modulator. To this end, the linearity of S_{15}, and S_{35} are investigated versus the applied bias voltage. Thus, the voltage ratios versus the applied reverse bias voltage of the varactor diode are plotted in Fig. 9. It is observed from Fig. 9 that reasonable linearity is achieved for the voltage ratios of the four outputs when applying dc reverse bias voltages in the range between 5 V to 10 V, which implies that the proposed design can be used as a linear amplitude modulator.

4. CONCLUSION

Two new 5-port power divider designs for controllable power division ratios have been presented. The power division control in both designs is implemented using varactor diodes. The first design utilizes two varactors to switch the input power into two selected output ports. This is achieved by biasing the two varactors so that one of the varactor-terminated lines is equivalent to a short circuit while the other is equivalent to an open circuit. In the second design, the power division ratios are controlled through the use of a single varactor. For this design, equal and unequal power division ratios are realized depending on the value of the DC bias voltage. High power division ratios were realized without the need to use transmission lines with high impedances or to redesign and refabricate. This feature is an advantage over many previous designs that had to resort to untraditional techniques to realize the high impedance transmission line associated with the design of power divider with high power division ratio. Measurement results of both designs were found to be consistent with the simulation results. Also, it was demonstrated that the single varactor design was capable of generating amplitude modulated signals.

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