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Novel Broadband Equalizer Optimization Technique for High-Speed Digital System Designs

Shaowu Huang[1, *] and Beomtaek Lee[2]

Abstract—In this paper, a novel broadband equalizer optimization technique is introduced for high-speed digital system designs. Through effectively compensating both conductor loss and dielectric loss, this technique provides a new solution to find optimal equalizer for high-speed signaling over printed circuit board (PCB) with continuous time linear equalizer (CTLE) as an application. The coefficients of CTLE are quickly identified through searching the minimum of the variation of total transfer functions over the low-mid frequency range. Channel simulations with different server interfaces of 12 Gbps and 25 Gbps are performed, respectively. Simulation results are presented to validate the technique.

1. INTRODUCTION

In modern digital systems, equalizers are needed to mitigate the inter-symbol interference (ISI) caused by the frequency dependent channel loss associated with printed circuit boards or copper cables [1–23]. As data rate approach higher and higher, which is the trend in industry, it is important to develop fast and effective equalizer optimization techniques. There are many high speed differential input/output (I/O) interfaces in the market for 25 Gbps and higher transfer rate such as 25 Gbps Ethernet, Infiniband EDR (25 Gbps), 28 Gbps Fiber Channel (32GFC), etc., and faster I/O interfaces such as OIF CEI-56G are under development, where the channel loss compensation becomes critical in high speed link circuit designs and platform designs.

In PCBs/packages/copper cables, the conductor loss is proportional to square root of the frequency ($\sqrt{f}$), and the dielectric loss is proportional to the frequency (f). Compensation of both conductor loss and dielectric loss is critical for achieving better recovery of transmit signal distorted by the frequency dependent loss in PCB design and applications.

In this paper, it is demonstrated that, (1) the different behaviors of the conductor loss and dielectric loss of PCB is one key factor determining the performance of equalizers in high speed signaling; (2) the performance of equalizers are sensitive to the variation of total transfer function at the low-mid band frequency range, which was also shown in the literature. In the proposed technique, the optimized settings are obtained through calculating the variation of total transfer function (S_{21} or S_{dd21}) including channel loss, equalizers, and other contributions such as on-chip pad response (C_{pad}) over the low-mid frequency range. The technique is targeted for compute system designs with PCB channels. It provides a novel and effective way to find optimal CTLE for compensating both conductor loss and dielectric loss over broadband frequency spectrum. This leads to improvement in high speed signaling performance, and/or efficiency in the design of equalizers with satisfied required performance.

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* Corresponding author: Shaowu Huang (shaowu.huang@intel.com).
[1] Intel Corporation, Dupont, WA 98327, USA. [2] Intel Corporation, Santa Clara, CA 95054 , USA.

2. METHODOLOGY

2.1. Physical Basis of the Proposed Technique

Through compensating both conductor loss and dielectric loss, this technique achieves best optimized CTLE for high speed signaling. Note that.

i) The distortion of signal due to the conductor loss and dielectric loss is most sensitive at the low-mid frequency range of [0 GHz, f_cut] for PCB channel. The cutoff frequency f_cut varies depending on the stack-up, and it is around 1 GHz to 1.5 GHz for most PCB layout.

ii) If the total transfer function can be designed to be "flat" enough over the low-mid frequency of [0 GHz, f_cut], the equalizer should be the best optimized in compensating both conductor loss and dielectric loss. Channel equalization over cutoff frequency are achieved with DFE (decision feedback equalizer) and/or increased CTLE bandwidth (higher frequency poles).

iii) By searching the minimum of the variation of total transfer function, which gives most "flat" total transfer function, the corresponding equalizers including CTLE can be best optimized.

iv) This provides a simple but powerful frequency-domain technique for designing broadband equalizers for PCB applications.

v) This paper discusses only the PCB applications. However, this idea can be extended to including package and copper cable application, which also has conductor loss and dielectric loss. This technique can be also extended to any other communication where the channel has two distinguishable losses (e.g., conductor loss vs. dielectric loss).

2.2. Implementation of the Proposed Technique

A simple implementation is described below on how to apply the technique in searching the CTLE optimized settings.

2.2.1. Determine the Variation of Transfer Function

The key step is to calculate the variation of total transfer function (S_{21}) including channel loss, equalizers, and other contributions such as on-chip pad response (C_pad).

Finding optimal equalization is like a minimization problem. The objective function can be defined in many ways. For example, either S_{21} variation over mean or standard deviation on frequency domain can be defined as the objective function.

2.2.2. Simple Methods to Calculate the Variation of Transfer Function

The standard deviation can be simply obtained through the integral of the square of the total S_{21}, such as

$$\sigma_{S_{21}} = \sqrt{\int_0^{f_\text{cut}} \left|S_{21_\text{total}}(f) - S_{21_\text{total}}\,(0\,\text{GHz})\right|^2 df} \tag{1}$$

where $S_{21_\text{total}}(f)$ is in dB scale. An alternative is to calculate the mean deviation, which can be simply obtained through the integral of the total S_{21}, such as

$$MD_{S_{21}} = \sqrt{\int_0^{f_\text{cut}} \left|S_{21_\text{total}}(f) - S_{21_\text{total}}\,(0\,\text{GHz})\right| df} \tag{2}$$

2.3. Applications of the Proposed Technique

There are various applications of the proposed equalizer optimization technique as different equalizers are used in real circuit design such as Tx FFE (feed forward equalizer), Rx FFE, Rx CTLE, Rx DFE (decision feedback equalizer), etc. This paper is focused on the application to CTLE. However, the proposed technique can be extended to other types of equalizers.

2.3.1. Procedure

First, find the optimized CTLE setting without TxFFE and DFE. The order and frequencies of poles can be picked as higher as possible from the available range of practical design parameters (circuit complexity, area, cost, etc.). With the chosen poles, the zeros are tuned and optimized accordingly. Note, the poles can be determined by the availability of hardware implementation. Higher order and/or higher frequency of poles will give larger Rx bandwidth and gain if the zeros are optimized accordingly. However, this leads to more complexities and higher cost in hardware implementation as well. Then, search optimal TxFFE and/or adaptively optimized DFE with the fixed optimized CTLE setting.

2.3.2. Complexity

Circuit design for this implementation can be simplest and lowest cost. In this paper the simulation result was shown with above method. As said above, the technique can be applied to find optimal CTLE per each Tx FFE setting for the best equalizer performance.

2.4. Advantages of the Proposed Technique

2.4.1. Problems with Conventional CTLE Design

Conventional CTLE usually uses brute force search over a sweep table for pole, zero and gain to determine the optimized settings in time domain. There are several disadvantages.

i) Due to restriction in complexity and cost of hardware implementation (e.g., power and area), the sweep table often only covers a small set of all possible zeros and poles. This is a restriction for conventional CTLE.

ii) For given sweep table, the brute force search and other optimization algorithms often rely on full channel margining to determine optimized settings. Since full channel margining is usually time-consuming in simulations. This consists of another restriction for conventional CTLE in practical design and applications.

iii) It is an iterative procedure to design optimal CTLE setting ranges (pole, zero and gain) and, thus, time-consuming.

2.4.2. Advantages of CTLE Design Using Proposed Technique

This technique computes optimal CTLE setting (pole, zero and gain) very efficiently and accurately on frequency domain without parameter sweeping or channel margin simulations.

i) This technique provides a simple but powerful tool to circuit engineers and signal integrity engineers for circuit and platform designs.

ii) Using this technique, the optimized CTLE can be directly found out without complicated sweeping procedure. The table of CTLE setting can be smaller, or even can be completely discarded. This leads to reduction in complexity and cost of hardware implementation for CTLE.

iii) Using this technique, the search of optimized setting doesn't require the channel margining. It gives faster optimization procedure than that in conventional CTLE design. This results in improved robustness of CTLE.

iv) The improved effectiveness of CTLE can provide solution space for the designs of other equalizers. For example, using this technique, the Tx FFE and Rx DFE can be less aggressive in tap settings. This can result in cost reduction in circuit and platform designs.

v) The improved effectiveness of CTLE can also help to eliminate the need of Tx FFE. Since Tx FFE causes the loss of energy, it is desired to remove the Tx FFE. Combining this technique with Rx DFE and without Tx FFE can be one feasible solution for high speed signaling.

3. SIMULATION RESULTS AND DISCUSSIONS

In this section, simulations are done to test the performance of proposed technique for CTLE application. Three different orders (1st, 2nd, and 3rd) of CTLE are compared. Two different high speed channels with data rates 12 Gbps and 25 Gbps are compared.

3.1. Case 1: 12 Gbps Channel

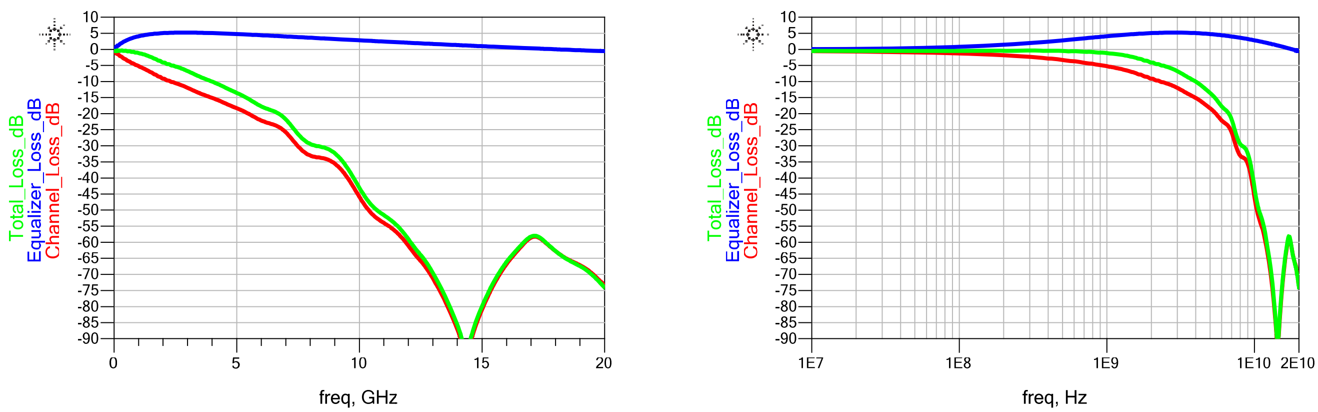
In the simulation, 1st order CTLE is used to determine the z_0 (zero point) with fixed p_0 (pole 0) and p_1 (pole 1). Pole 1 is pre-set as $s = 2 * \pi * f = 40$, with frequency $f = 6.37$ GHz. The standard deviation is computed to determine the minimum of the variation.

A high speed server channel is used in simulation with two via stubs of length = 81 mils at the transfer rate of 12 Gbps. For given $p_1 = 6.37$ GHz ($s = 40$), $p_0 = 2.86$ GHz ($s = 18$), the variation (standard deviation) is calculated for varying z_0 from 0.1 to 10, and it is found that $z_0 = 0.67$ GHz ($s = 4.2$) gives minimum variation. The cut off frequency is 1.25 GHz in the calculation. Then, the optimized z_0 is 0.67 GHz for given $p_1 = 6.37$ GHz and $p_0 = 2.86$ GHz. In this case the stub resonance is, at 14.5 GHz, far away from the low-mid band of (0 GHz, 1.25 GHz).

In Figure 1, the transfer functions in terms of S_{21} are compared for the proposed 1st order CTLE ($p_1 = 6.37$ GHz, $p_0 = 2.86$ GHz, $z_0 = 0.67$ GHz). Results clearly show that, the optimized value give "flat" total transfer function over frequency range [0, 1.25 GHz].

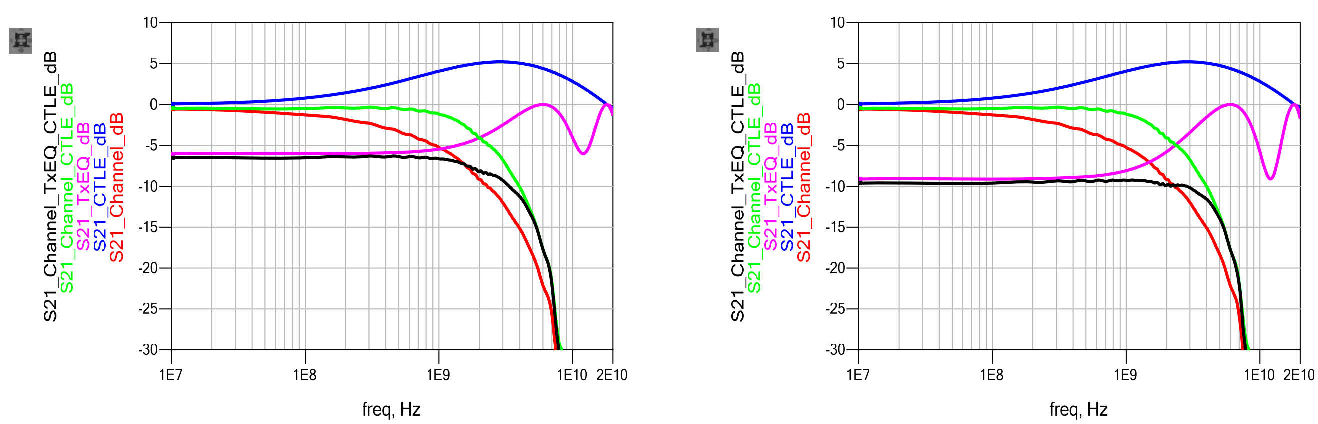
In Figure 2, the S_{21} are compared for the case with a 3 tap Tx FFE. Figure 2(a) shows with 6 dB Tx FFE, the optimized proposed 1st order CTLE is almost the same. Figures 2(b), (c), and (d) show that, the more the Tx FFE increases, the more the CTLE change is needed accordingly to keep the total transfer function "flat" over the low-mid frequency range.

In Figure 3, the eye diagrams are compared over no equalization, CTLE, Rx FFE and Rx DFE; (a) no equalization, (b) 1st order CTLE, (c) 12 tap Rx FFE, (d) 6 tap Rx DFE, (e) 1st order CTLE and 6 tap Rx DFE, and (f) 12 tap Rx FFE and 6 tap Rx DFE. In Table 1, the eye height and eye

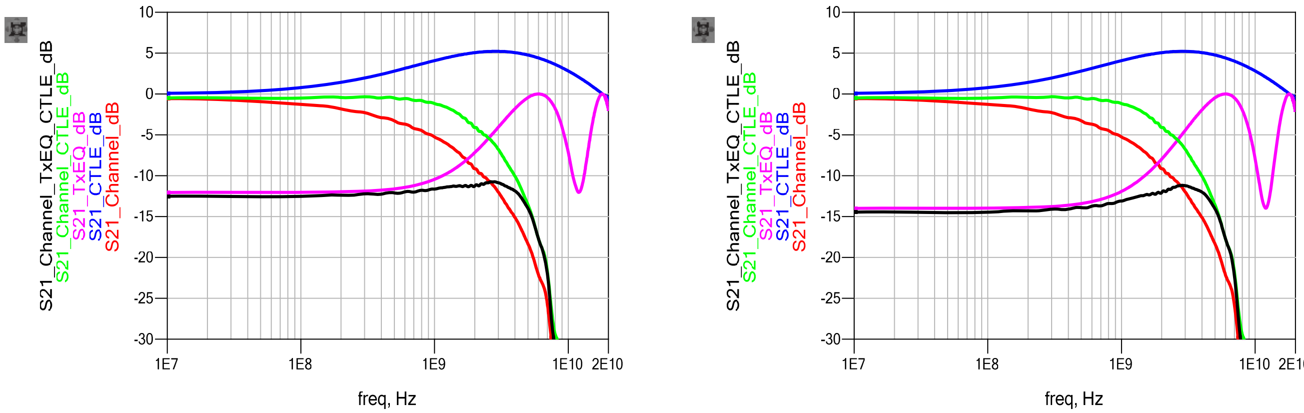


(a) (b)

Figure 1. S_{21} for the channel with 81 mil via stubs: Red — Channel; Blue — 1st order proposed CTLE; Green — Total. (a) S_{21} in log-log scale, (b) S_{21} in linear-log scale.



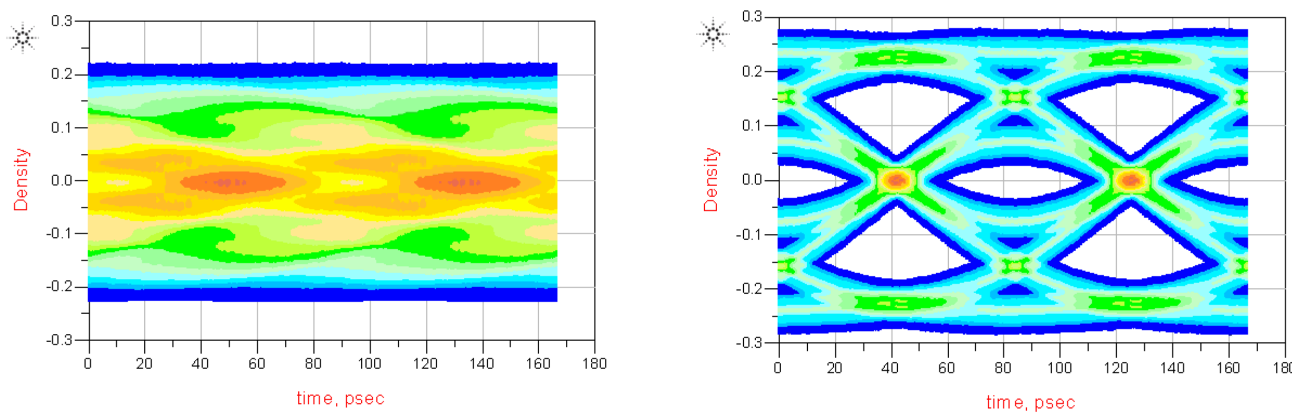
(a) (b)



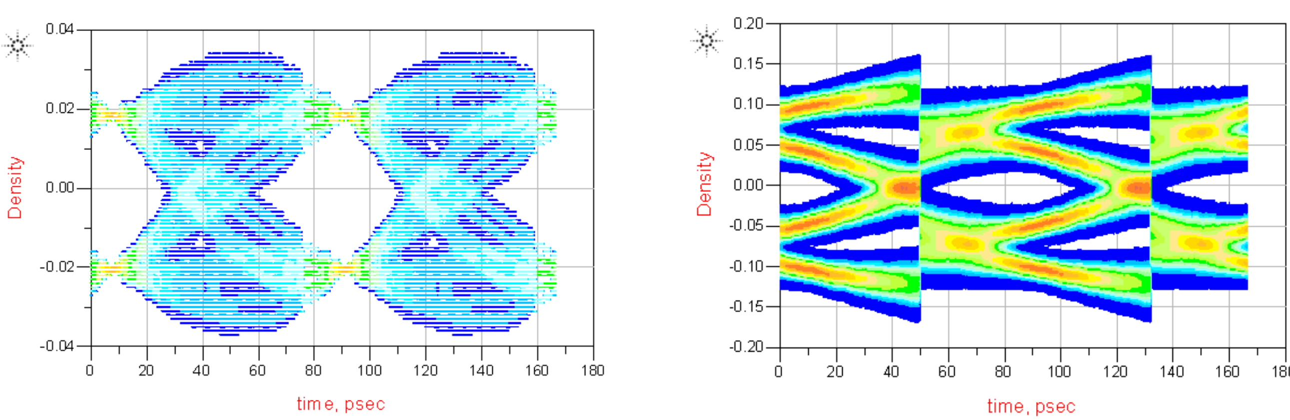
(c) (d)

Figure 2. S_{21} for the channel with 20 mil via stubs: Red — Channel; Blue — CTLE; Green — Channel + CTLE; Magenta — TxEQ; Black — Channel + CTLE + TxEQ. (a) 6 dB TxEQ: Precursor $= -0.125$, post-cursor $= -0.125$, (b) 9 dB TxEQ: Precursor $= -0.15$, post-cursor $= -0.175$, (c) 12 dB TxEQ: Precursor $= -0.175$, post-cursor $= -0.2$, (d) 15 dB TxEQ: Precursor $= -0.2$, post-cursor $= -0.2$.

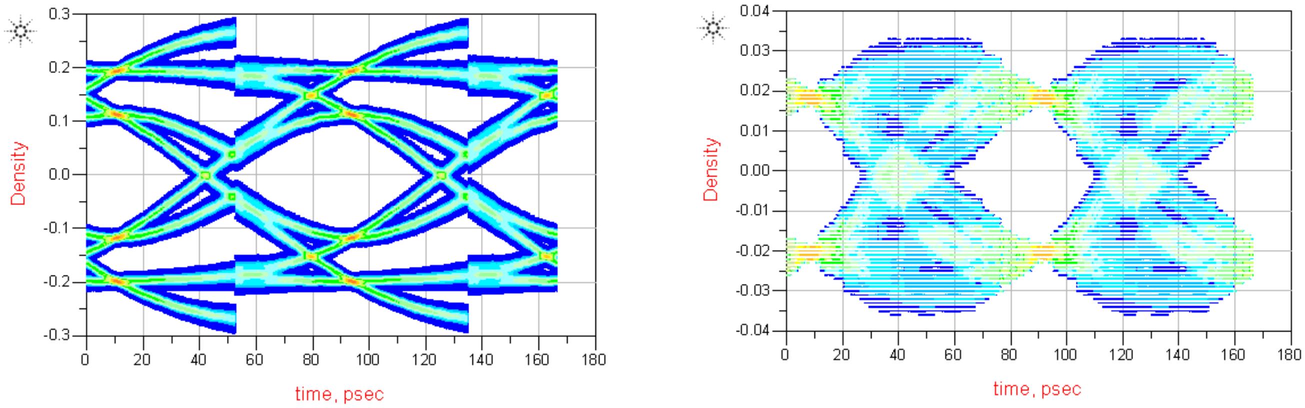
width are summarized and compared for the diagrams in Figures 3(a)–(f). Results show that with no equalization the eye is completely close. The 1st order proposed CTLE is more effective than 6-tap adaptively optimized Rx DFE or 12-tap adaptively optimized Rx FFE. Combining proposed CTLE and DFE gives the best equalization for the channel in simulation.



(a) (b)



(c) (d)

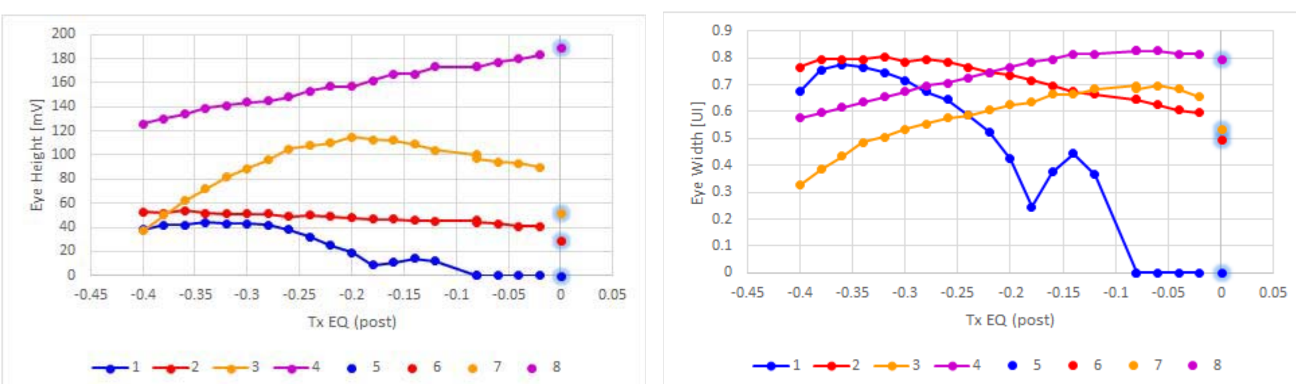


(e) (f)

Figure 3. Comparison of eye diagrams among Rx CTLE, Rx FFE, and Rx DFE. (a) No equalization, (b) 1st order proposed CTLE, (c) 12 tap optimized Rx FFE, (d) 6 tap optimized DFE, (e) 1st order proposed CTLE + 6 taps optimized DFE, (f) 12 tap Optimized Rx FFE + 6 tap optimized DFE.

Table 1. Summary for Figure 3: Comparison of eye height/width.

12 Gbps	No eq	CTLE	Rx FFE	Rx DFE	Rx CTLE + DFE	Rx FFE + DFE
EH [mV]	0	52	36	29	189	34
EW [UI]	0	0.535	0.615	0.495	0.795	0.615



(a) (b)

Figure 4. Comparison among Tx FFE, CTLE, DFE and combinations. (a) Eye height, (b) eye width.

Next, a 3 tap brute force Tx FFE search is added. In Figure 4, the eye height and eye width are compared among 1st order proposed CTLE and 6 tap Rx DFE with the 3-tap brute force Tx FFE. Both pre-cursor and post-cursor are swept over $[-0.4, -0.02]$ to find optimal Tx FFE settings. Results are summarized in Table 2. Results show that the proposed CTLE also works well with Tx FFE. Combination of CTLE, Tx FFE, and Rx DFE can give best EW. However, the combination of CTLE and Rx DFE without Tx FFE gives the largest EH, because there is no signal amplitude attenuation caused by the Tx FFE. Again, this indicates that, this technique combined with DFE can be used to eliminate or minimize the need of Tx FFE for the channel in simulation.

Table 2. Summary for Figure 4: Comparison of eye height/width.

Color	Index	Equalization	EH [mV]	EW [UI]
Blue line	1	Tx FFE	44	0.775
Red line	2	Tx FFE + Rx DFE	54	0.805
Orange line	3	Tx FFE + Rx CTLE	115	0.695
Purple line	4	Tx FFE + Rx CTLE + Rx DFE	183	0.825
Blue dot	5	No equalization	0	0
Red dot	6	Rx DFE	29	0.495
Orange dot	7	Rx CTLE	52	0.535
Purple dot	8	Rx CTLE + Rx DFE	189	0.795

3.2. Case 2: 25 GT/s Channel

In this case, a high speed server channel is used in simulation with the transfer rate of 25 Gbps.

3.2.1. 2nd Order CTLE with 2nd Pole $p_2 = 9.55$ GHz

In the simulation, 2nd order CTLE is used to determine the z_1 and z_0 (zero points) with fixed p_0 (pole 0), p_1 (pole 1) and p_2 (pole 2). Pole 2 is pre-set as $s = 2 * \pi * f = 60$, with frequency $f = 9.55$ GHz. The standard deviation is computed to determine the minimum of the variation.

For given $p_2 = 9.55$ GHz ($s = 60$), $p_1 = 8.75$ GHz ($s = 55$), $p_0 = 7.96$ GHz ($s = 50$), the mean variation is calculated for varying z_1 and z_0, and it is found that $z_1 = 2.57$ GHz and $z_0 = 0.95$ GHz gives minimum variation. The cut off frequency is 2 GHz in the calculation. In this case the Nyquist frequency is at 12.5 GHz, far away from the low-mid band of (0 GHz, 2 GHz).

In Figure 5, the transfer functions in terms of S_{21} are compared for the proposed 2nd order CTLE ($p_2 = 9.55$ GHz, $p_1 = 8.75$ GHz, $p_0 = 7.96$ GHz, $z_1 = 2.57$ GHz, $z_0 = 1.27$ GHz). Results clearly show that, the optimized value give "flat" total transfer function over frequency range [0, 2 GHz].

In Figure 6, the eye diagrams are compared over no equalization, CTLE, Rx FFE and Rx DFE; (a) no equalization, (b) 2nd order CTLE, (c) 12 tap Rx FFE, (d) 6 tap Rx DFE, (e) 2nd order CTLE and 6 tap Rx DFE, and (f) 12 tap Rx FFE and 6 tap Rx DFE. In Table 3, the eye height and eye width are summarized and compared for the diagrams in Figures 6(a)–(f). Results show that with no equalization or DFE the eye is completely close. The 2nd order proposed CTLE is more effective

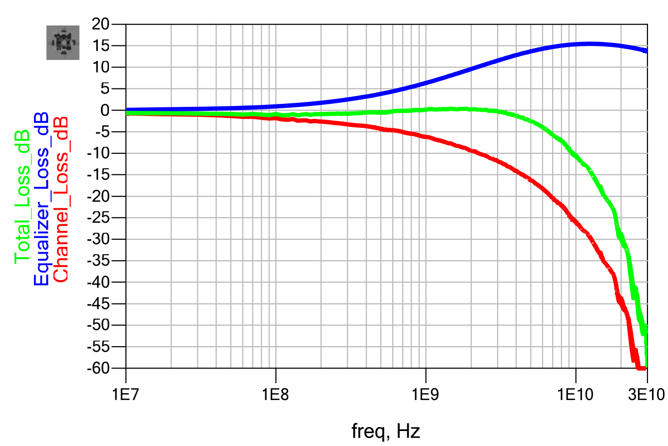


Figure 5. S_{21} for the channel in log-log scale: Red — Channel; Blue — 2nd order proposed CTLE; Green — Channel with optimal CTLE.

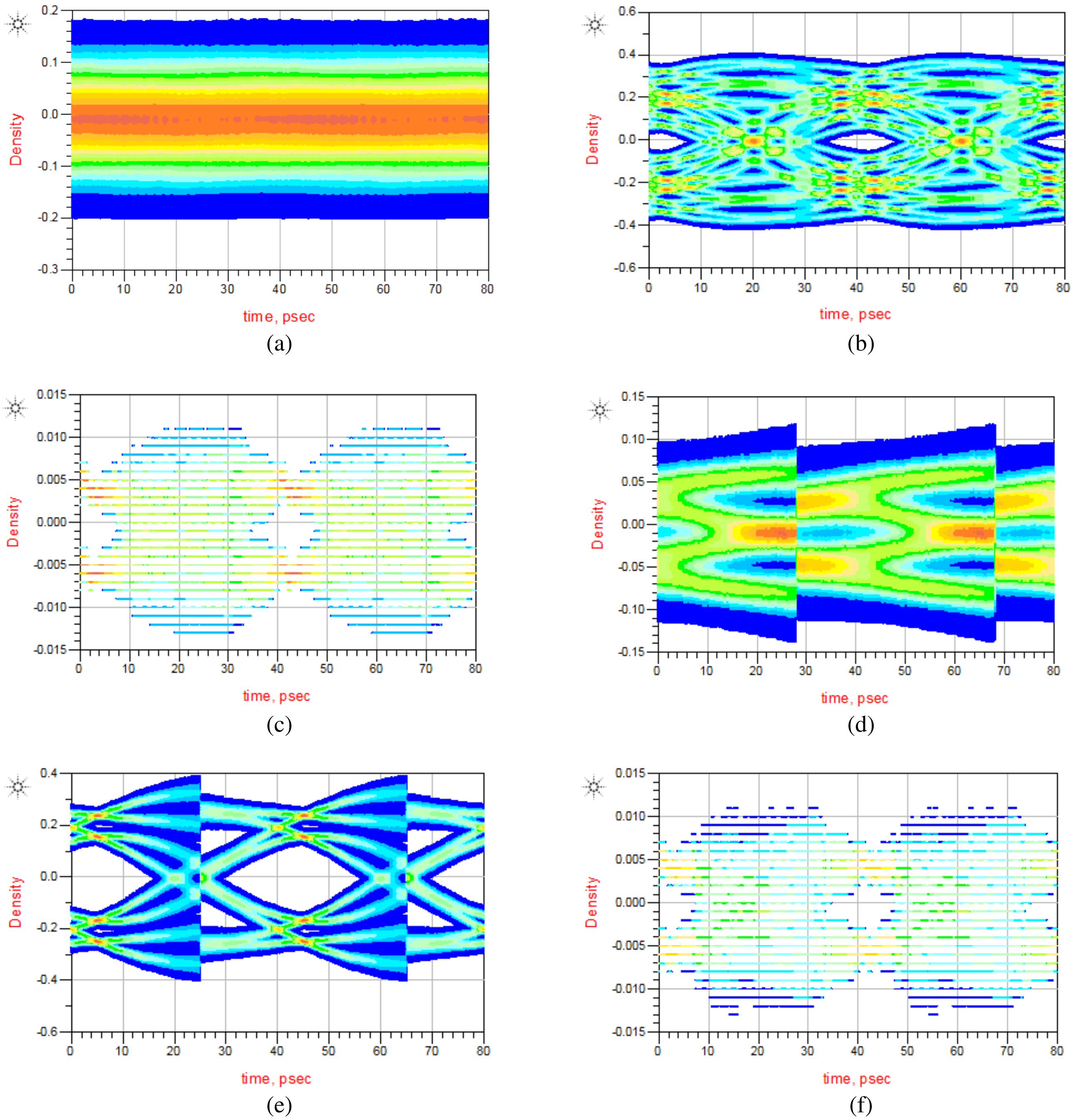


Figure 6. Comparison of eye diagrams among Rx CTLE, Rx FFE, and Rx DFE. (a) No equalization, (b) 2nd order proposed CTLE, (c) 12 tap optimized Rx FFE, (d) 6 tap optimized DFE, (e) 2nd order proposed CTLE + 6 taps optimized DFE, (f) 12 tap Optimized Rx FFE + 6 tap optimized DFE.

than 6-tap adaptively optimized Rx DFE or 12-tap adaptively optimized Rx FFE. Combining proposed CTLE and DFE gives the best equalization for the channel in simulation.

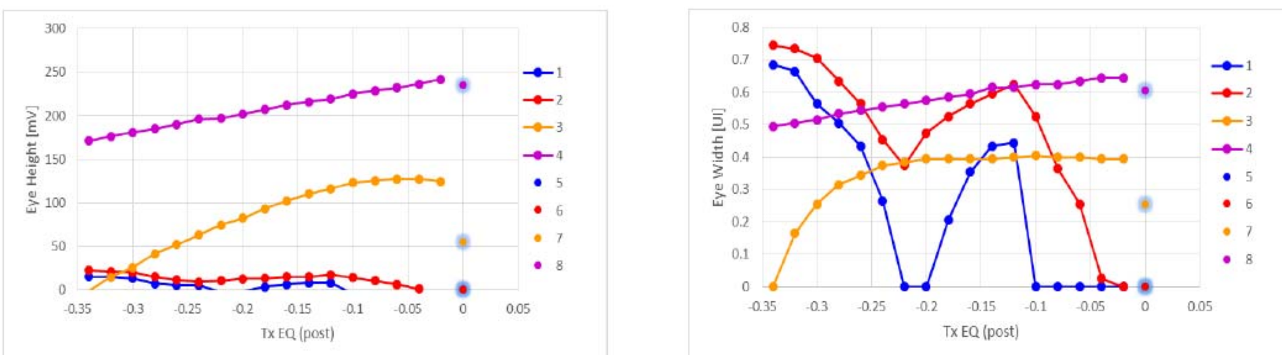
Next, a 3 tap brute force Tx FFE search is added. In Figure 7, the eye height and eye width are compared among 2nd order proposed CTLE and 6 tap Rx DFE with the 3-tap brute force Tx FFE. The pre-cursor are swept over $[-0.4, -0.02]$ and the post-cursor are swept over $[-0.34, -0.02]$ to find optimal Tx FFE settings. Results are summarized in Table 4. Results show that the proposed CTLE

Table 3. Summary for Figure 6: Comparison of eye height/width.

25 Gbps	No eq	CTLE	Rx FFE	Rx DFE	Rx CTLE + DFE	Rx FFE + DFE
EH [mV]	0	55	6	0	235	5
EW [UI]	0	0.255	0.315	0	0.605	0.345

Table 4. Summary for Figure 7: Comparison of eye height/width.

Color	Index	Equalization	EH [mV]	EW [UI]
Blue line	1	Tx FFE	15	0.685
Red line	2	Tx FFE + Rx DFE	22	0.745
Orange line	3	Tx FFE + Rx CTLE	127	0.405
Purple line	4	Tx FFE + Rx CTLE + Rx DFE	242	0.645
Blue dot	5	No equalization	0	0
Red dot	6	Rx DFE	0	0
Orange dot	7	Rx CTLE	55	0.255
Purple dot	8	Rx CTLE + Rx DFE	235	0.605



(a) (b)

Figure 7. Comparison among Tx FFE, CTLE, DFE and combinations. (a) Eye height, (b) eye width.

also works well with Tx FFE. Combination of CTLE, Tx FFE, and Rx DFE can give best eye opening as EW*EH. The eye opening of combination of CTLE and DFE without Tx FFE is almost as good as the best. It indicates that, the technique combined with DFE can be used to eliminate or minimize the need of Tx FFE for the channel in simulation.

3.2.2. 2nd Order CTLE with 2nd Pole $p_2 = 12.7$ *GHz*

Next, it still uses 2nd order CTLE but increase the frequencies of the poles. For given $p_2 = 12.7$ GHz ($s = 80$), $p_1 = 11.1$ GHz ($s = 70$), $p_0 = 9.55$ GHz ($s = 60$), the mean variation is calculated for varying z_1 and z_0, and it is found that $z_1 = 2.76$ GHz and $z_0 = 0.95$ GHz gives minimum variation. The cut off frequency is 2 GHz in the calculation.

In Figure 8, the transfer functions in terms of S_{21} are compared for the proposed 2nd order CTLE ($p_2 = 12.7$ GHz, $p_1 = 11.1$ GHz, $p_0 = 9.55$ GHz, $z_1 = 2.76$ GHz, $z_0 = 0.95$ GHz). Results clearly show that, the optimized value give "flat" total transfer function over frequency range [0, 2 GHz].

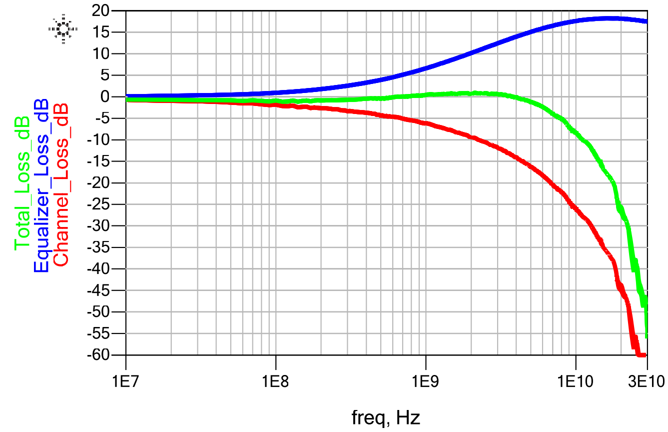


Figure 8. S_{21} for the channel in log-log scale: Red — Channel; Blue — 2nd order proposed CTLE; Green — Channel with optimal CTLE.

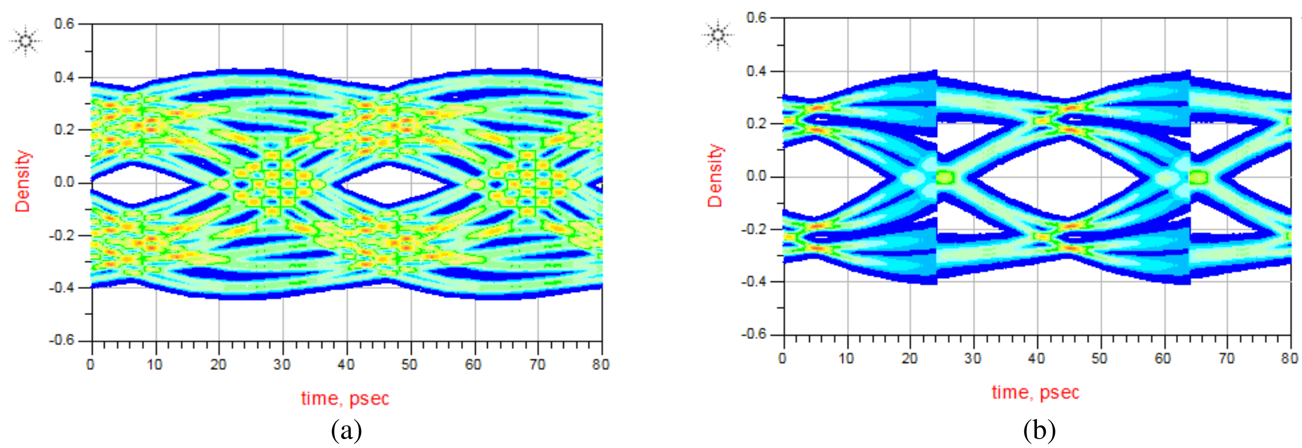


Figure 9. Comparison of eye diagrams among Rx CTLE and Rx DFE. (a) 2nd order proposed CTLE, (b) 2nd order proposed CTLE + 6 taps optimized DFE.

Table 5. Summary for Figure 9: Comparison of eye height/width.

25 Gbps	CTLE	Rx CTLE + DFE
EH [mV]	117	269
EW [UI]	0.355	0.605

In Figure 9, the eye diagrams are compared over CTLE and Rx DFE. Note, the cases with no equalization or Rx FFE are same as those in Figure 6. In Table 5, the eye height and eye width are summarized and compared for the diagrams in Figures 9(a)–(b). The 2nd order proposed CTLE is more effective than 6-tap adaptively optimized Rx DFE or 12-tap adaptively optimized Rx FFE. Combining proposed CTLE and DFE gives the best equalization for the channel in simulation.

Eye height and eye width results in Table 5 are better than those in Table 3 with CTLE and CTLE with DFE. CTLE pole frequencies used in Table 5 are higher than those used in Table 3, and it moves the peak frequency close to Nyquist frequency (12.5 GHz). It can viewed as increasing the receiver bandwidth. Thus, it improves receiver margins of eye height and eye width in Table 5 comparing to those in Table 3.

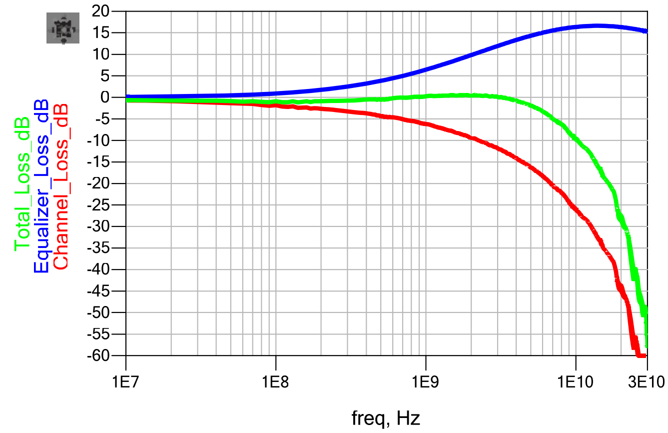


Figure 10. S_{21} for the channel in log-log scale: Red — Channel; Blue — 3rd order proposed CTLE; Green — Channel with optimal CTLE.

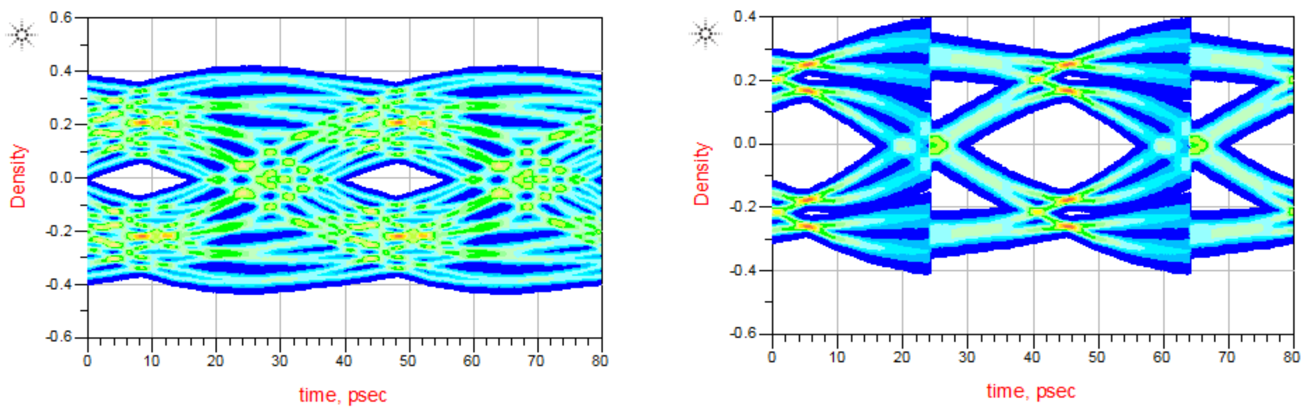


Figure 11. Comparison of eye diagrams among Rx CTLE, Rx FFE, and Rx DFE. (a) 3rd order proposed CTLE, (b) 3rd order proposed CTLE + 6 taps optimized DFE.

3.2.3. 3rd Order CTLE with 3rd Pole $p_3 = 9.55$ GHz

Next, it uses 3rd order CTLE with lower frequencies of the poles. For given $p_3 = 9.55$ GHz ($s = 60$), $p_2 = 8.75$ GHz ($s = 55$), $p_1 = 7.96$ GHz ($s = 50$), $p_0 = 7.16$ GHz ($s = 45$), and $z_2 = 4.8$ GHz ($s = 30$), the mean variation is calculated for varying z_1 and z_0, and it is found that $z_1 = 2.9$ GHz and $z_0 = 0.95$ GHz gives minimum variation. The cut off frequency is 2 GHz in the calculation.

In Figure 10, the transfer functions in terms of S_{21} are compared for the proposed 3rd order CTLE. Results clearly show that, the optimized value give "flat" total transfer function over frequency range [0, 2 GHz].

In Figure 11, the eye diagrams are compared. In Table 6, the eye height and eye width are summarized and compared for the diagrams in Figures 10(a)–(b). Results show the3rd order proposed CTLE is more effective than 6-tap adaptively optimized Rx DFE or 12-tap adaptively optimized Rx FFE. Combining proposed CTLE and DFE gives the best equalization for the channel in simulation.

CTLE pole frequencies used in Table 3 and Table 6 are the same except one more pole is added in cases of Table 6 for CTLE and CTLE with DFE. Eye height and eye width results in Table 6 are better than those in Table 3 with CTLE and CTLE with DFE. The receiver margins of eye height and eye width are improved by adding a pole in Table 6 comparing to those in Table 3, but the gain is not as much as increasing the receiver bandwidth as shown in Table 5. Table 7 compares above three cases of CTLE implementations. Again, it shows the importance of CTLE design and receiver bandwidth for

Table 6. Summary for Figure 11: Comparison of eye height/width.

25 Gbps	CTLE	Rx CTLE + DFE
EH [mV]	94	253
EW [UI]	0.305	0.585

Table 7. Summary for Figure 6 (CTLE, RX CTLE + DFE), 9 and 11: Comparison of eye height/width.

25 Gbps	CTLE			Rx CTLE + DFE		
Case	3.2.1	3.2.2	3.2.3	3.2.1	3.2.2	3.2.3
CTLE	2nd	2nd	3rd	2nd	2nd	3rd
highest f_p [GHz]	9.55	12.7	9.55	9.55	12.7	9.55
EH [mV]	55	117	94	235	269	253
EW [UI]	0.255	0.355	0.305	0.605	0.605	0.585

both without and with DFE. Higher order CTLE and higher receiver bandwidth improve eye opening at the receiver.

4. CONCLUSIONS

In this paper, a novel broadband equalizer optimization technique is proposed to best compensate both dielectric loss and conductor loss for PCB design and applications. The applications to find the optimized CTLE in frequency domain is investigated. The coefficients of the CTLE are determined via searching the minimum variations of total transfer functions. The technique is implemented for 1st, 2nd, and 3rd order CTLEs, respectively. Simulations are performed with 12 Gbps and 25 Gbps channels to verify the method. Results show the method provides an effective and fast optimization solution for determine the CTLE coefficients.

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