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Analytical Modeling and Analysis of Through Silicon Vias (TSVs) in High Speed Three-Dimensional System Integration

Md Amimul Ehsan[1], Zhen Zhou[2], and Yang Yi[1, *]

Abstract—This paper gives a comprehensive study on the modeling and design challenges of Through Silicon Vias (TSVs) in high speed three-dimensional (3D) system integration. To investigate the propagation characteristics incurred by operations within the ultra-broad band frequency range, we propose an equivalent circuit model which accounts for rough sidewall effect and high frequency effect. A closed-form expression for TSV metal oxide semiconductor (MOS) capacitance in both depletion and accumulation regions is proposed. The coupling of TSV arrays and near and far field effect on crosstalk analysis are performed using 3D Electro-Magnetic (EM) field solver. Based on the TSV circuit model, we optimize the TSVs' architecture and manufacturing process parameters and develop effective design guidelines for TSVs, which could be used to resolve the signal integrity issues arising at high frequency data transmission in 3D Integrated Circuits (ICs).

1. INTRODUCTION

Three-dimensional integrated circuits (3D ICs) have become an inordinately propitious technology. The advantages gained by vertically stacking with multiple dies are: (1) a reduction in form factor, (2) high system speed, (3) high interconnect densities, (4) a decrease in overall wire length, and (5) reduced power consumption [1–3]. To analyze the electrical performance of 3D ICs, it is crucial to model and design the Through Silicon Vias (TSVs) accurately and efficiently because of their critical roles in the overall communication architecture [4]. TSVs are most commonly fabricated by high aspect ratio deep silicon etchinglined with a dielectric to provide electrical isolation; and super conformed filled with copper. Unlike the conventional interconnects, TSVs are essentially metal insulator semiconductor (MIS) devices [5] wherein the dielectric layer (typically SiO_2) is deposited to isolate the conductive metals from the substrate [6]. From the design standpoint, as related to parasitic extraction, TSVs can be incorporated as a separate cell (within conventional design tools) that demands proper analytical modeling and characterization. The ultimate goal is clear and straightforward: low-cost, high-yield process technologies, and successful attainments require concise optimizations of the TSV electrical design process, which demands a comprehensive consideration of complex TSV electrical modeling and analysis [7].

Metal oxide semiconductor (MOS) effect is an important phenomenon in TSV based 3D ICs which could overcome the misestimation that occurs in determining the cylindrical capacitance. When TSVs are operated in the low frequency range, the MOS effect in TSVs can be quite satisfactorily modeled as MOS capacitances [8]; whereas, when TSVs are operated in the ultra-broad band frequency range, the electrical behavior is considerably altered and deviated into a domain of scarcely imaginable complexity. High speed switching can dynamically bias the TSV-MIS interface and result in regions of electronic accumulation or depletion; the capacitance becomes a nonlinear function of signal bias. In 3D ICs, the

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* Corresponding author: Yang Yi (yyi@ku.edu).

[1] Department of Electrical Engineering and Computer Science, University of Kansas, Lawrence, KS 66045, USA. [2] Intel Corp. Research Lab on Photonic Technology, 3600 Juliette Ln, Santa Clara, CA 95054, USA.

MOS capacitance plays a significant role to decrease the total capacitance due to biased substrate and thus it reduces the leakage current into the silicon material [2].

Most of the TSV modeling approaches focus on the radio frequency (RF) applications with operation frequency of several GHz or even lower, whereas the TSV technology specifically for millimeter wave range (mmW)/THz applications is seldom reported. The mmW communication has emerged as an enabling technology to resolve the spectrum shortage issue due to significant growth of mobile data traffic [9–11]. There are some outstanding challenges due to electro-magnetic (EM) effects that are associated with the mmW technology such as impedance mismatching, signal reflections, crosstalk, and radiation [12, 13]. It is therefore a prudent consideration to address the critical issues which influence the properties of the TSVs in ultra-high and extremely-high frequency range [7]. These challenges can be addressed by properly modeling and designing the TSVs considering those effects in emerging and attractive 3D integration approach. A cross sectional view of an mmW transceiver module in 3D silicon interposer technology is shown in Figure 1. One of the most important issues is the sidewall roughness which induces a significant quantity of leakage current within the TSVs [14]. The effect of sidewall roughness must be considered within the mmW frequency range, since the root mean square (rms) height of the sidewall roughness features become comparable to the skin depth.

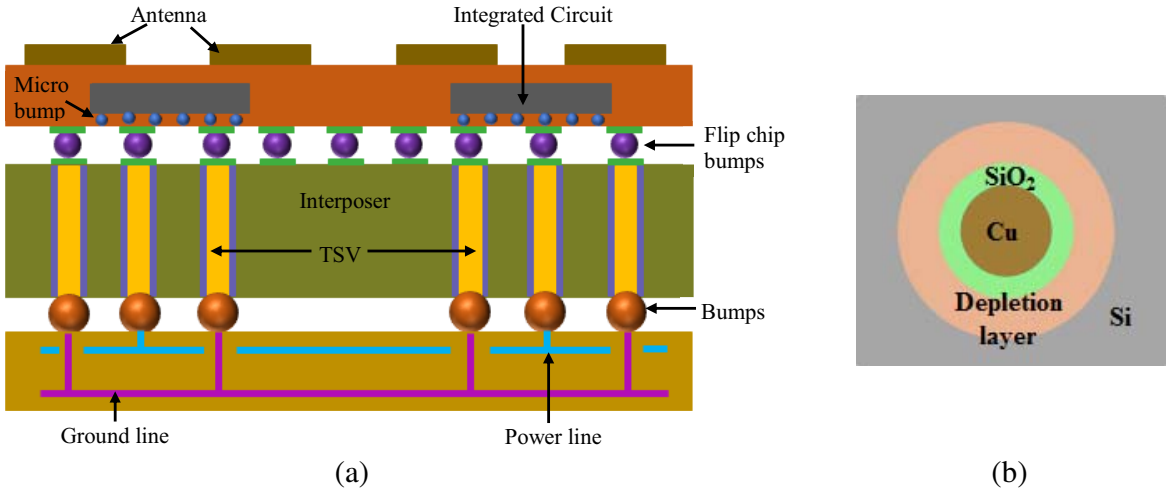

Figure 1. (a) 3D structure of an mmW transceiver module, and (b) cross sectional view of TSV.

Heretofore, a considerable amount of research work on TSV modeling and analysis have been performed to address the impact of TSVs on high speed signals, to analyze the TSV crosstalk, to study the TSV resistance, as well as to apply the full-chip extraction and optimization [15–22]. Reasonably comprehensive TSV models have been constructed which characterized resistance, inductance, capacitance, and conductance. These modeling methodologies can be categorized into three discrete classes; depending on the type of electromagnetic technique used: full-wave modeling, quasi-static modeling, and analytical modeling [15]. These three modes correspond to different silicon resistivity levels; (1) a slow wave, low frequency mode, where the electrical field is as if "screened" by the silicon substrate, and the magnetic field penetrates somewhat into the substrate; (2) a quasi-transverse electromagnetic mode, wherein both electrical and magnetic fields penetrate deeply into the substrate; and: (3) a very high frequency skin effect mode, where the characteristic dimension of the silicon skin depth is smaller than the TSV spacing.

This paper proposes a closed-form analytic expression for TSV capacitance which accounts for both depletion and accumulation effects. Furthermore, we introduce a rough sidewall TSV model to account for the propagation characteristics within the ultra-broad band frequency range. Our endeavor culminates with an equivalent circuit model that accurately captures all the parasitic elements of various TSVs arrangements. The proposed circuit model accounts for high frequency skin effects, eddy currents in the substrate, MOS effects, and sidewall roughness effects. The model's compactness and compatibility with Simulation Program with Integrated Circuit Emphasis (SPICE) simulators allows

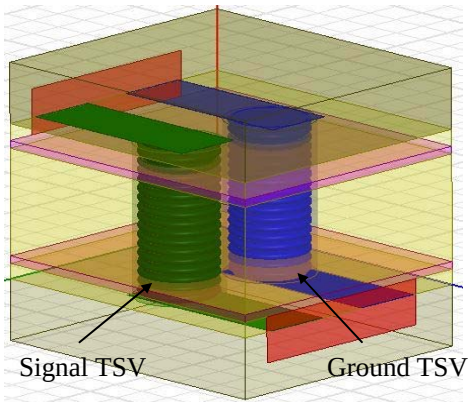

Figure 2. TSV pair with sidewall roughness.

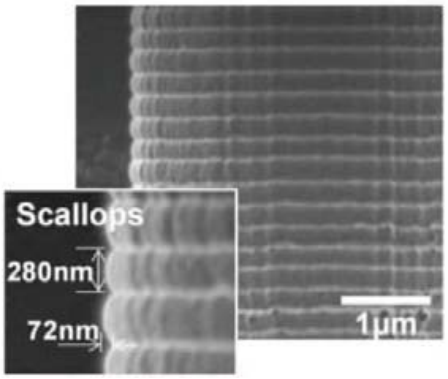

Figure 3. SEM image of TSV with sidewall roughness using Bosch etching [14].

the electrical modeling of various TSVs arrangements without the need for computationally expensive field solvers, which significantly reduces the simulation running time. We also focused on the coupling and cross talk analysis between the TSV interconnections which is critical in signal integrity. Based on the proposed TSV model, we optimize the TSVs' architecture and manufacturing process parameters and develop effective design guidelines for TSVs which could be used to resolve the signal integrity issues arising at high speed data transmission in 3D ICs.

2. MODELING AND SIMULATION OF TSV IN ULTRA-HIGH FREQUENCY

Electromagnetic models of differential and complex multi-TSVs are proposed to extract electrical parasitics and obtain analytic equations for lumped model analysis in the frequency domain [16–18]. Numerical, analytical, and measurement based methods have been extensively applied to extract the TSV parameters and validate EM simulations. High frequency analytical efforts have generated TSV models that include parametric studies of skin and proximity effects towards a comprehension of propagation characteristics [15, 19]. The impacts of differing TSV geometries and structures upon signal integrity can be quantified and the performance of the TSVs can be optimized by using coaxial configuration.

To model the TSVs, analytical expressions of RLGC parameters are required; these are obtained from the transmission line theory [23], and simply extended into the high frequency range [15, 24]. Analytical expressions of frequency dependent RLGC incorporated within the model account for differing geometric parameters, dielectric materials, electromagnetic permeability, and the effects of lossy substrate materials. The skin effect is the critical model factor, because as operating frequency increases, current accumulates at the sidewall. As a consequence, the skin depth decreases; which causes the effective resistance and inductances of TSV to increase by reducing the effective cross-section of the conductor. These frequency dependent additional resistance and inductances are added to the RL parameters of transmission line to get the TSV resistance and inductance. The results of certain previous work [7] relate this skin effect can be modeled as an additional resistance, $R_0(f)$ and inductance, $L_0(f)$, according to:

$$R_0(f) = \frac{hf\mu_0}{2r\sqrt{\pi f\mu_0\sigma_{Cu}} - 1} \tag{1}$$

where h is the height of TSV, r is the radius of TSV, f is the operating frequency in GHz, μ_0 is the permeability of the free space, and σ_{Cu} is the conductivity of the conductor.

$$L_0(f) = \frac{\mu_0 h}{2\pi} \ln\left(1 + \frac{2.84h}{\pi r}\right) + \frac{R_0(f)}{2\pi f} \tag{2}$$

The effect of conductor surface roughness is more significant at mmW frequency due to skin effect. In our study, we examined the impact of surface roughness by the creating the TSV structures with and

without surface roughness. The TSV surface roughness is illustrated in Figure 2 where a signal TSV is paired with a ground TSV. Also, an experimental study is performed by T. Nakamura et al. [14] to measure the leakage current due to the surface roughness at high frequency. In this experiment, the rough surface TSV shown in Figure 3 is created during a process of "Bosch etching".

The roughness of the conductor surface have significant effects on signal integrity and it is important to model the rough surface for proper analysis. The rough surface is characterized by the correlation length l, rms height of roughness Δx, and the correlation function. Using the spectral density or the Fourier transformation of the correlation functions, the roughness profile can be generated [25];

$$W(k_x) = \frac{1}{2\pi}\int_{-\infty}^{\infty} e^{jk_x x}(\Delta x)^2 C(x)dx \tag{3}$$

where Δx is the height of sidewall roughness and $(\Delta x)^2 C(x)$ the correlation function.

Due to the existence of the conductor surface roughness of TSV, an increased resistance is appeared. For the proper modeling of TSV, it has to be taken into account the impact of roughness. A Gaussian distribution function is necessary to approximate the binomial distribution of events;

$$g(x) = \frac{1}{\sqrt{2\pi\sigma_g^2}} e^{\frac{-(x-a)^2}{2\sigma_g^2}} \tag{4}$$

Then applying the continuous Gaussian distribution function and modification of the resistance due to skin effect, the following additional resistance is obtained:

$$R_s(f) = \frac{a(h-a)}{\sigma_g^3\sqrt{2\pi}} e^{\frac{-(h-a)^2}{2\sigma_g^2}} \frac{k_c}{\sigma_{cu}\pi\left[(r+\Delta x)^2 - r^2\right]} \tag{5}$$

where $k_c = f(f_\theta)$ is angular spatial frequency, σ_g^2 the variance, and a the mean value of the number of events, and the probability of any integer.

The schematic diagram of rough surface TSV is shown in Figure 4 where the geometric parameters are indicated. The complete equivalent circuit model of TSV shown in Figure 5 is obtained by combining all the high frequency RLGC elements that associated with the charge and current density distribution and accounts the sidewall roughness as well.

This analytical model includes the parasitic elements that represent the loss, as well as the inductive and capacitive coupling in conductor and insulating sidewall. The accuracy of this analytical model of TSV is verified through the 3D field simulation based model by means of scattering parameters (S-parameters).

Simulated results with and without rough sidewall and analytical results with rough sidewall is shown in Table 1 and Table 2 from 10 GHz to 100 GHz. The S-parameters of the TSV pair in 3D ICs studied for this work are calculated with the equivalent circuits illustrated in Figure 5, and are

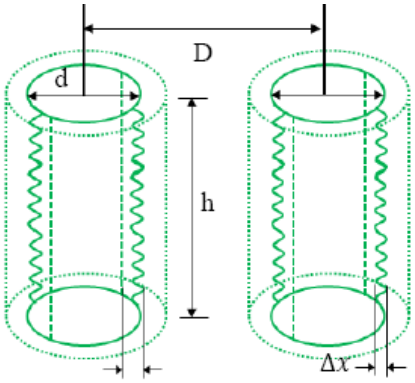

Figure 4. Rough sidewall TSV.

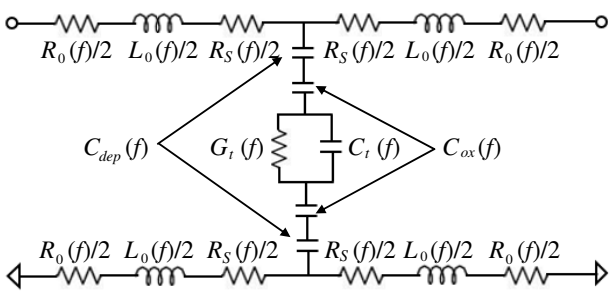

Figure 5. Equivalent circuit model of TSV.

Table 1. Analysis of S parameter (magnitude) with and without rough sidewall in TSV.

Frequency (GHz)		10	20	30	40	50	60	70	80	90	100
S_{11} (dB)	Model	−22.91	−19.73	−17.35	−17.71	−17.48	−17.28	−17.04	−16.77	−16.57	−16.43
	Simulation	−22.35	−20.75	−19.56	−18.90	−18.47	−18.00	−17.46	−16.97	−16.62	−16.41
	Sim. w/o roughness	−24.30	−22.08	−21.10	−20.65	−20.28	−19.96	−19.55	−18.92	−18.57	−18.39
S_{12} (dB)	Model	−0.573	−0.805	−0.906	−0.936	−0.945	−0.954	−0.955	−0.954	−0.953	−0.952
	Simulation	−0.621	−0.796	−0.865	−0.892	−0.900	−0.909	−0.917	−0.923	−0.928	−0.929
	Sim. w/o roughness	−0.596	−0.750	−0.814	−0.837	−0.846	−0.855	−0.863	−0.870	−0.874	−0.876

Table 2. Analysis of S parameter (phase) with and without rough sidewall in TSV.

Frequency (GHz)		10	20	30	40	50	60	70	80	90	100
S_{11} (dB)	Model	−68.93	−92.58	−115.5	−127.8	−139.7	−146.3	−152.3	−156.1	−162.0	−163.2
	Simulation	−88.29	−112.3	−127.5	−138.4	−146.5	−152.8	−157.8	−161.9	−165.0	−167.7
	Sim. w/o roughness	−89.44	−113.5	−130.1	−140.3	−147.9	−153.6	−158.6	−162.4	−167.1	−168.9
S_{12} (dB)	Model	−17.37	−29.81	−40.35	−49.78	−58.41	−66.37	−73.73	−80.56	−88.09	−93.85
	Simulation	−19.06	−36.03	−49.97	−61.37	−70.91	−79.25	−86.81	−93.91	−100.7	−107.3
	Sim. w/o roughness	−19.01	−35.08	−49.24	−60.32	−70.01	−78.17	−85.52	−91.98	−99.70	−105.9

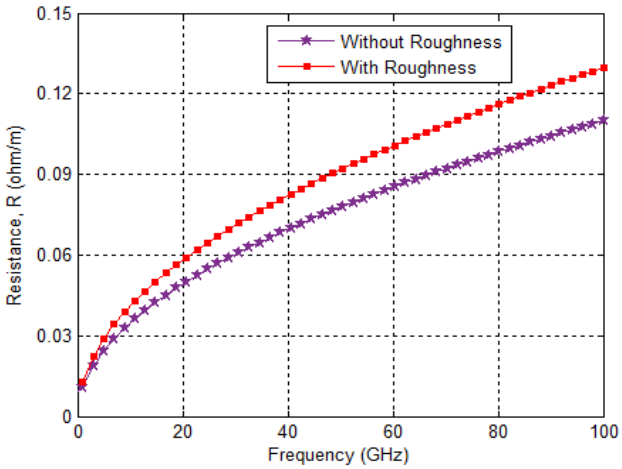

Figure 6. Comparison of TSV pair resistances with and without surface roughness.

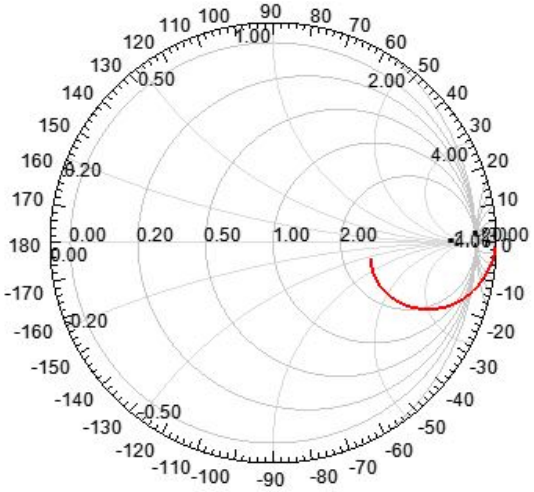

Figure 7. HFSS S parameter (S_{11}).

compared to their HFSS (high frequency structure simulator) [26] simulated values. As demonstrated in Table 1 and Table 2, it has been found that there is a close correlation and good agreement between the values of simulated results and the analytical models.

At low frequency as 10 GHz, S parameter value is the same between the rough and smooth sidewall TSV but after that it varies due to the loss mechanism in rough sidewall. As a validation of the proposed model Figure 6 is plotted and it provides the comparison of resistances of TSV pair with and without surface roughness. Figure 7 shows the representation of the measured S_{11} parameter.

Parametric study is being performed and simulation is carried to assess the quantitative influence of physical and geometric parameters of TSV on the impedance and consequently on loss properties. The impact of TSV physical parameters to its electrical response can also be better understood by technology tuning. The insertion and return loss can be set as perform merit matrices to assess the impact of the TSV physical parameters.

To optimize the performance and capture the enhancement of the TSV model, the parameters, i.e., thickness of SiO_2, pitch, and length of the via are investigated independently. The thinnest oxide liner has the highest return loss because a significant amount of reflected wave propagates in Si, which is not an insulator and hence experiences more loss. Whereas, the insertion loss improves for the shorter length of TSV. Therefore, the losses can be minimized by using higher resistivity silicon, thinner oxide line and shorter TSV length.

3. MODELING OF TSVS WITH VOLTAGE DEPENDENT AND NONLINEAR CAPACITANCE

New basis functions are introduced to capture the effect of TSV oxide liner that could simulate a large number of TSVs with less computation time [22]. The full wave analysis methods are accurate, but will be computationally intensive due to the large number and multi-scale dimensions (oxide thickness and aspect ratio) of TSVs in the 3D mmW ICs. Another bottleneck of the full wave methods is that it is difficult to be compatible with SPICE simulators. The equivalent circuit methods with lumped Resistance (R), inductance (L), conductance (G), and capacitance (C) elements could be a good alternative and can provide good compatibility with SPICE simulators. Most of the TSV modeling approaches in equivalent methods focus on the RF applications with operation frequency of several GHz or even lower, whereas the TSV technology specifically for mmW/THz applications is seldom reported. The challenges in modeling TSV in 3D mmW integrated circuits comes from the need of accurate broadband model capturing high frequency effect, frequency-dependent losses, coupling, and mismatch.

As mentioned in previous sections, TSVs have been mostly modeled assuming that the TSV MIS interface is not biased and the silicon substrate is a lossy, low conductive medium. Ignoring the semiconductor properties of the substrate and the resulting MOS capacitance introduce significant inaccuracies in the TSV modeling. Refs. [27–30] studied the impact of a bias voltage on TSV characteristics (mostly capacitance) theoretically and experimentally. However, these analyses only consider the static biasing and hence they are only applicable for the small and low-speed signal application. Ref. [31] rigorously modeled the full-wave, both small and large signal wave propagation in a MIS micro strip structure. It requires solving both the full Maxwell equations and Boltzmann transport equation at the same time. Even though the TSVs are small in size and there is no need to consider wave propagation, the Boltzmann equation still needs to be solved simultaneously to consider the carrier accumulation and depletion. Furthermore, it is very difficult to apply the proposed TSV models to the channel simulations. Therefore, we propose a computationally efficient circuit model of the TSVs with the consideration of non-linear and voltage dependent capacitance.

Since the high speed signals can dynamically bias the TSV MIS interface and drive the TSV MIS into the accumulation or depletion regions, the TSV capacitance is expected to be nonlinear and dependent on the biasing of the TSVs with respect to the substrate. When the TSV MIS is in accumulation region, the electrical field is confined in the SiO_2 liner and the TSV capacitance is equal to the SiO_2 liner capacitance; when TSV MIS is in depletion region, the electrical field can penetrate into the substrate and the TSV capacitance is equal to the SiO_2 liner capacitance in series with the depletion region capacitance. The TSV MIS interface is biased statically. In a p-type substrate, the majority carriers are positively charged holes. A flat band voltage (V_{FB}) can be defined for MIS interface and it corresponds to the voltage that induces zero net charge in silicon:

$$V_{FB} = \varphi_m - \varphi_{Si} - Q_S/C_{ox} \tag{6}$$

where φ_m and φ_{Si} are the work functions of TSV metal and silicon; Q_S is space charge. C_{ox} is silicon liner capacitance and expressed as,

$$C_{SiO_2} = 2\pi\varepsilon_o \frac{\varepsilon_{ox}}{\ln\left(\frac{r}{r_{ox}}\right)} \tag{7}$$

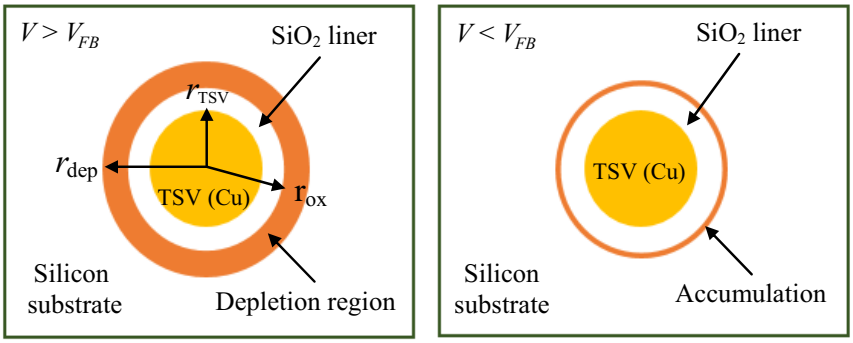

Figure 8. Accumulation and depletion of TSV MIS.

When a voltage V is applied to a TSV, if $V < V_{FB}$, the positively charged holes in silicon are dragged to Si-SiO_2 interface, and an accumulation layer is formed; if $V > V_{FB}$, holes are pushed away and a depletion region is formed (as shown in Figure 8). V_{FB} depends on material properties as well as fabrication processes (doping, etc.). Note that the similar results could be applied to n-type substrate cases. When the TSV MIS is in accumulation region, the electrical field is confined in the SiO_2 liner and the TSV capacitance is equal to C_{ox}. When TSV MIS is in depletion region, the electrical field can penetrate into the substrate, and the TSV capacitance is equal to C_{ox} in series with C_{dep}. (C_{ox} is the capacitance of the SiO_2 liner, C_{dep} is the capacitance of the depletion region). Accordingly, an analytical formula for depletion capacitance is introduced for the large signal and nonlinear capacitance [18].

$$C_{dep} = 2\pi\varepsilon_S h / \ln\left[\left(r_{ox} + w_{dep}\right)/r_{ox}\right], \tag{8}$$

where h is the TSV height, ε_s the dielectric constant of Si, and r_{ox} the radius of a TSV with SiO_2 liner.

The depletion width w_{dep} can be calculated by solving the Poisson's equations of scalar potential in the depletion region and a Laplace's equation in the SiO_2 liner. The depletion width w_{dep} is expressed as;

$$w_{dep} = 2\varepsilon_S \left(-t_{ox} + \sqrt{t_{ox}^2 + 3\varepsilon_{ox}^2 \left(V - V_{FB}\right) \Big/ \left(qN_a\varepsilon_S\right)} \right) \Big/ 3\varepsilon_{ox}, \tag{9}$$

where t_{ox} is the SiO_2 liner thickness, V_{FB} the flat band voltage, V is supply voltage, ε_{ox} the dielectric constant of the SiO_2 liner, and N_a the silicon doping concentration.

We verified the proposed analytical formula by comparing it with the C-V curve obtained from static simulation and measurement with a static bias. The TSV capacitance $C_{\mathrm{TSV}}(V(t))$ is much higher than the capacitance obtained assuming small signal analysis and non-biasing condition [15].

To obtain a faster signal response and lower signal distortion,the TSV process and geometry parameters ought to be tune to achieve minimum TSV capacitance in the desired operating voltage region. Table 3 shows the horizontal eye opening (UI) and vertical eye opening (mv) of the chip level TSV at accumulation region (high Cap.), depletion region (medium Cap.), and deep depletion region (low Cap.). Figure 9 shows the eye diagrams of interposer TSVs without and with optimized depletion capacitance when the signal data rate at 30 Gbps.

As shown in the Figure 9, the eye diagram of interposer TSV is closed when its data rate reaches 30 Gbps. As jitter closes the eye horizontally and noise closes the eye vertically, the sampling area gets squeezed, increasing the chance to sample incorrectly and get bit errors. This could be a very serious performance issue for TSV in silicon interposer, especially for mmW applications. The optimized depletion capacitance is achieved by biasing the TSV into the deep depletion region with low work function metal for p-type Si. Compared with the eye diagram shown in Figure 9, we find the performance of interposer TSV significantly improved. As shown in both Table 3 and Figure 9, optimizing the parameters of TSVs architecture and manufacturing process to obtain the minimum depletion capacitance could drastically enhance the TSV electrical performance across wide frequency range. Our study helps in developing design guidelines for TSVs in 3D ICs.

Table 3. Horizontal & vertical eye opening.

Data Rate (Gbps)	Horizontal Eye Opening (UI)			Vertical Eye Opening (mv)		
	High Cap.	Medium Cap.	Low Cap.	High Cap.	Medium Cap.	Low Cap.
10	0.9	0.95	0.96	94	96	100
15	0.85	0.93	0.94	81	84	87
25	0.82	0.875	0.9	70	74	76

4. COUPLING AND CROSSTALK ANALYSIS OF TSV ARRAYS

Coupling and cross talk are another important issues in large TSV arrays; such impacts can be analyzed in both time and frequency domain through eye margin analysis [20, 21], which present the electrical modeling, analysis, and measurement of TSV coupling capacitance without considering the MOS capacitance effect. However, considering the MOS capacitance effect [8, 18] has an influential dominance on determining the TSV mutual capacitance.

An important effect which requires special attention is the coupling effect in rough surface TSVs. Consider a numerous amount of closely spaced I/O TSVs co-existing with various mixtures of signal and ground TSVs in high speed circuits and systems [6, 32]; we simulate the coupling of 4 rough surface TSV pairs arranged in linear configuration with ground and signal TSV in HFSS, as shown in Figure 10.

The electric and magnetic fields for the TSV arrangement presented in Figure 10 are demonstrated in Figures 11 and 12. As a MIS structure, the TSV produces electric and magnetic fields induced by current and voltage near the copper conductor which has near field characteristic. Both the electric and magnetic fields are plotted at 100 GHz.

The capacitive coupling which is dominated in the TSV structure between the TSVs depend on the permittivity of the oxide, the TSV geometry, the arrangement of surrounding TSVs, and body contacts places. The coupling in the case of nearest adjacent TSVs with respect to the central TSV in a TSV array is higher than the coupling with the TSVs in the diagonal direction. The TSV coupling capacitance and inductance increase as the space between the TSVs decreases. As demonstrated in Figure 13, S_1 has the strongest coupling to S_2, compared to couplings to other signal TSVs. The coupling can be reduced by adding the ground TSV and making the TSV pairs fully surrounded by ground vias; following proper design consideration.

Also the crosstalk between those two adjacent TSVs is obtained. The crosstalk is the outcome

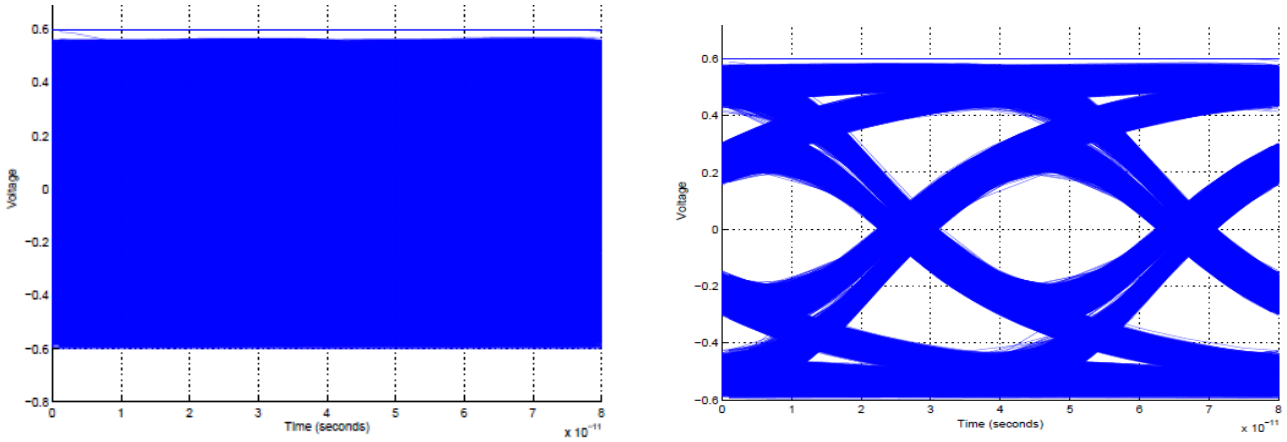

Figure 9. (a) Eye diagram of interposer TSV, (b) eye diagram of interposer TSV with optimized depletion capacitance.

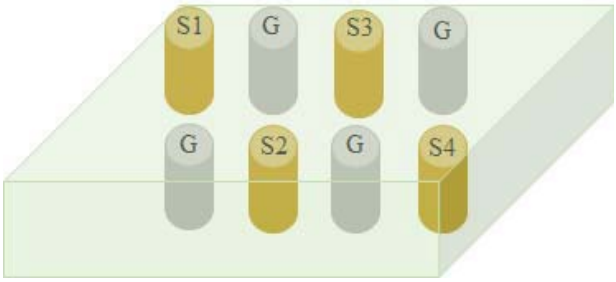

Figure 10. Different TSV configurations for coupling analysis.

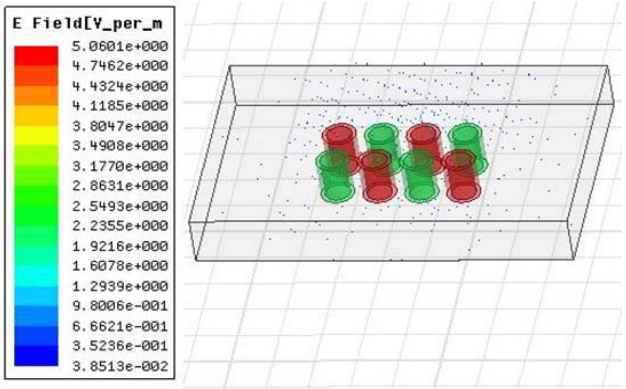

Figure 11. E field distributions of 4 TSV.

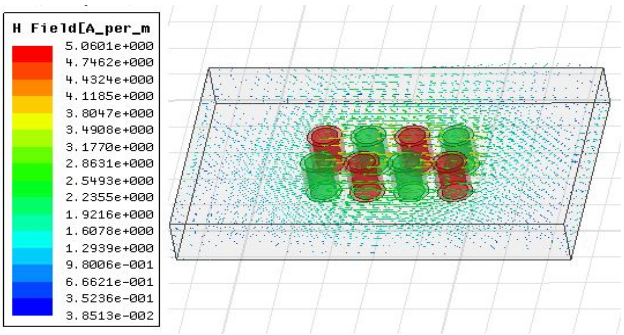

Figure 12. H field distribution of 4 TSV.

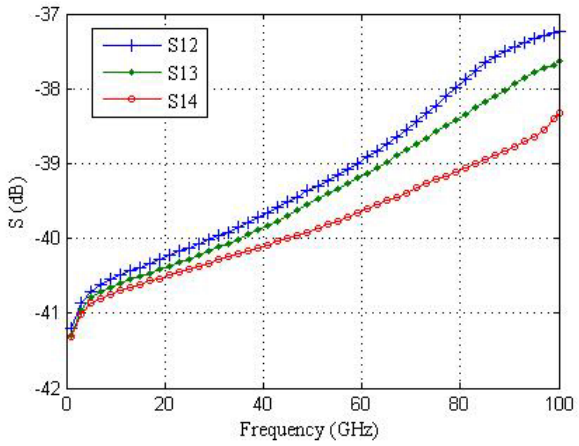

Figure 13. Coupling S parameters in different TSV pairs.

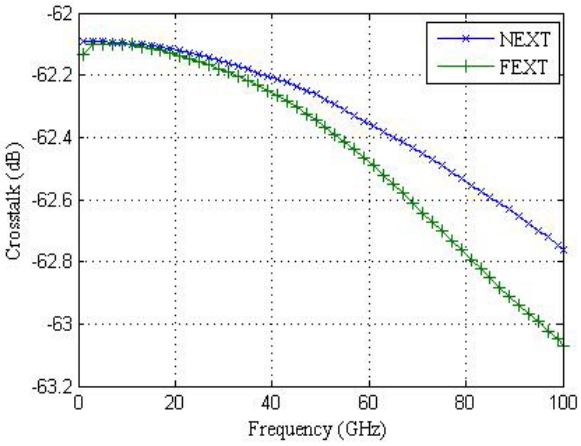

Figure 14. Signal-ground near and far end crosstalk of between two TSV pairs.

of capacitive coupling due to the conductivity of Si substrate and thin SiO_2 that introduces a large capacitance. Both the simulation results, near end crosstalk (NEXT) and the far end crosstalk (FEXT) are shown in Figure 14. At a frequency beyond 10 GHz, higher NEXT than FEXT is observed. The sharp slope in FEXT at very low frequency is for the slow wave propagation. For the Maxwell-Wagner effect, the velocity of propagation of slow wave mode is much slower and it increases the effective permittivity at lower frequencies. Also, NEXT behaves differently than FEXT at lower frequencies can be explained by the fact of ground planes that provides a shieling effect.

5. CONCLUSION

Analytical modeling and 3D electromagnetic field simulation for TSVs have been performed, and the challenges associated with electrical design have been analyzed. A rough sidewall TSV is modeled that captured the impact of conductor sidewall roughness in high speed 3D interconnects. The proposed model is analytically calculated and validated by comparing the S-parameters predicted by both the model and the HFSS simulation up to 100 GHz in both magnitude and phase. From this study, it is found that the effect of TSV sidewall roughness becomes a very important factor when modeling TSVs in the extremely high frequency band. MOS effect and high frequency effect are investigated in mmW/THz frequency range. The impact of the voltage dependent and nonlinear capacitance on the performance of high speed differential signals is analyzed with the data of eye diagram approach. The coupling of TSV arrays under high speed operations using 3D EM field solver is performed and the near and far field effect on crosstalk analysis is observed. Parametric study is performed for the assessment of quantitative influence on loss properties of TSV and the impact of the frequency, pitch, dielectric, and TSV length is observed on the overall performance.

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